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Proposed Fast Electronics for EPICS

los alamos
scientific laboratory
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Proposed Fast Electronics for EPICS

by

Henry A. Thiessen

PROPOSED FAST ELECTRONICS FOR EPICS

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ABSTRACT

A block diagram has been prepared for the fast electronics for EPICS including beam monitors. The system should prove to be adequate for the first few experiments with the exception that no provision has been made for a differential Cherenkov counter. The comments and criticism of users during the summer of 1972 have been incorporated.

I. DETECTOR COMPLEMENT

I have assumed that the standard detectors for the spectrometer consist of four helical proportional chambers, two scintillators, one lucite Cherenkov counter, and one gas Cherenkov counter. In addition, provision is made for four veto scintillation counters (for use as pole-tip veto counters in as-yet-to-be-defined locations) and a scintillation counter which can be installed near the first proportional chamber when better particle identification is required at the expense of momentum resolution. These detectors will be located roughly as shown below in Fig. 1 (the particles travel from left to right).

In addition, I have assumed that we will have two 3-counter telescopes and two ion chambers for use as beam monitors.

II. DETECTION PROBLEMS

A. Counting Rates

For a total cross section of 1 barn (assumed isotropic), a beam intensity of $5 \times 10^8 \pi^+/\text{sec}$, a solid angle of 15 msr, and a 100 mgm/cm² carbon target, we expect an instantaneous counting rate in the first detector of

$$C = 5 \times 10^8 \times \frac{6 \times 10^{23}}{12} \times .1 \times \frac{10^{-24}}{4\pi} \times .015 \\ \times 16 = 0.5 \times 10^5 \text{ counts/sec.}$$

In the above calculation, no effect of the low momentum cutoff of the triplet has been considered, hence the rate obtained should be considered to be an upper limit.

Fig. 1.

B. Pion-Muon Separation

The problem of separation of pions and muons is difficult in the energy region of pions and muons of EPICS. The resolution of the spectrometer and consistency checks such as projection to the target, etc., will eliminate a substantial number of muon counts. The remaining muon counts will give a smooth background under our spectra. Stroot, et al., found this background to be a problem only at small scattering angles. A design study for a differential Cherenkov counter capable of separating pions and muons is under way. I have made no provision for such a counter in the initial block diagram since a complete design is not available and funding is not assured.

C. Electrons

Electrons (and positrons) are easily eliminated with a threshold Cherenkov counter containing a gas such as freon or propane at a pressure slightly above 1 atmosphere. I have provided for one such counter in the block diagram (Fig. 1).

D. Protons

Protons will be the most numerous background in many experiments. The $(\pi, 2p)$ reaction has a large total cross section and results in roughly isotropic protons of all energies. Protons can be separated from pions by range, dE/dx , and by time-of-flight in the 128-417 MeV/c region. Some relevant data appears in the table below.

We note that below about 250 MeV/c, the protons will not have sufficient range to penetrate the scintillation counters. Over the remainder of the energy region, the helical chambers may have sufficient time resolution to separate protons and

pions. dE/dx will give more reliable separation, however, there will be an efficiency problem because of the long tail of the Landau distribution. With a discriminator threshold at $3.5 \times$ minimum, 2-3% of the pions will give pulses larger than threshold. If we use two counters and require that the threshold be exceeded in both counters before the event is classified as a proton, then the inefficiency can be reduced to negligible proportions. If any protons remain, they may easily be rejected by time-of-flight.

E. Lucite Cherenkov Counter

There may be occasions when a lucite or other threshold counter will be useful for separating pions from protons. At a few specific momenta, it may be possible to separate pions and muons with such a counter as well. Provision has been made for such a counter.

F. Accidentals

There may be a significant number of accidental extra tracks in the first helical proportional chamber. The simplest way to handle this problem is to read all events into the computer and classify events with additional y wires fired as accidentals. Since many accidentals will be thrown out because of failure to retrace to the target or an incorrect momentum measurement, it is likely that a correction should be made for the number of events lost due to additional tracks in the chamber and that no correction should be made for extra accidental triggers. In making this correction, we must keep alert for events in which two or more adjacent wires have an avalanche due to delta rays or other causes (see Charpak's review article). Thus, the readout system

TABLE I

T_{π} MeV	P MeV/c	$1/c\beta$ ns/m	dL/dx min	T_p MeV	Range gm/cm ²	$1/c\beta$ ns/m	dL/dx min	$\frac{dL/dx_p}{dL/dx_{\pi}}$	$\Delta\tau$ (7m) ns
50	128.3	4.9	1.60	8.7	0.1	24.6	18.9	11.8	--
100	194.7	4.1	1.20	20.0	0.4	16.4	11.0	9.1	--
150	253.7	3.8	1.08	33.7	1.1	12.8	7.6	7.0	63
200	309.6	3.7	1.03	49.8	2.2	10.7	5.7	5.5	49
250	363.7	3.6	1.01	68.0	3.9	9.2	4.5	4.9	39
300	416.9	3.5	1.00	88.4	6.2	8.2	3.8	3.7	35

must record the number of adjacent wires struck as well as recording any additional hits.

Accidental vetoes of good events (by the pole tip counters) may be significant. In order to correct for this possibility, the number of events in coincidence with veto counter pulses and the number of events with a coincidence with a delayed veto counter pulse will be recorded.

G. Dead Time Monitoring

There will be a significant dead time (20-50 μ sec) each time an event is read into the computer. In addition, there will be a built-in dead time ($\sim$ 1200 ns) for each event in each helical chamber in order to prevent pile-up effects in the chambers. The readout for each chamber will include a busy signal which is a logical one during this dead time. However, a fast output (SOR) which is the "OR" of all the high voltage wire signals will be provided which is never insensitive. The SOR and busy signals can be used to monitor the number of events lost during the dead time. There will still be a small dead time associated with each wire. However since most wires are not affected by an event, the remaining dead time should be between one and two orders of magnitude smaller than the monitored dead time.

III. ELECTRONICS BLOCK DIAGRAM (See Fig. 2)

A. General

Scalars are provided at many points in the logic. In addition to scaling rates needed for computing cross sections, these scalars serve three purposes: 1) they provide confidence (and the possibility of a post-mortem check) that all circuits are operational; 2) they provide for rapid location of failures; and 3) they provide permanent checks on the validity of the data. Although the number of NIM modules is somewhat larger than the bare minimum required and the number of scalars is a lot larger, we feel that the extra circuits are justified for several reasons. First, the large number of users who have been allotted only short running time means that education and debugging time must be minimized. Second, the large number of possible running conditions needed to cover all experiments proposed means that permanent checks must be set up for effects which can cause problems in one experiment and not in another. Finally, the additional scalars are likely to cost on the order of \$100/

channel since they can largely be 10 MHz units which means that they are relatively inexpensive.

B. Operation of Helical Chamber Fast Output ("SOR") and Busy Output ("BUSY")

The anode wires of the helical proportional chambers will be used to provide a fast output for use in the trigger electronics. As noted earlier, we will use the proportional chamber to monitor its own accidentals, and pile-up rejection and dead time circuits will also be required.

These circuits will operate as follows. The first anode pulse will generate a fixed duration output pulse "SOR" (100 ns, but can be changed by changing R or C). During this fixed time, any additional anode pulse will set a flip-flop to indicate its presence, but will not cause an additional SOR pulse nor will it lengthen the SOR pulse. The memory flip-flops will be desensitized and a busy output signal will appear at the trailing edge of the SOR pulse. The BUSY signal will be 1200 ns long unless a readout trigger is received, in which case it will last until the computer readout cycle is complete. The SOR signal will not be gated by busy, and anode pulses received during the time that busy is a logical 1 will update the busy timer and also will cause an additional 100 ns SOR pulse to appear. The above logic will be constructed for each helical chamber, and the OR of the busy signals from all chambers will be provided as well. This logic should be sufficient to prevent pile-up effects, should allow monitoring of accidentals by recording extra hits in the chambers, and should allow monitoring of events rejected during the major dead time. Note that since the memory flip-flops are sensitive during the 100 ns SOR pulse, this time is not a dead time of the system.

C. Veto Counters

The veto counters will be used entirely by recording the output in the computer via the EG&G C212 input register. Since the effect of these counters depends on the computer programs for event reconstruction, this method allows maximum flexibility in the use of veto counter information.

D. Trigger Selection

An "OR" circuit has been provided to allow the user the ability to trigger the readout on π , p, e or any combination of these. If cable lengths are properly chosen, it should be possible to change the trigger without otherwise affecting the logic.

EPICS, PROPOSED FAST ELECTRONICS BLOCK DIAGRAM, 1 AUG. 72

Fig. 2.

By making use of the ratio of triggers to inputs to the trigger selector, it is possible to obtain the dead time losses for events of interest.

E. Time-of-flight and Pulse Height Data

All useful pulse height data are recorded by the LRS 2248 (Octal ADC). All scintillator and Cherenkov counter pulse heights can be monitored with this one unit. A particular advantage of the method chosen for using the veto counter information is that the pulse height distribution in each veto counter can be recorded to keep track of the performance of these counters.

Two important times are measured by the LRS 2226 Quad TDC. The choice of logic and output pulse lengths (together with proper overall timing) should guarantee that the leading edge of the event signal carries the timing information of the S2 counter, if one and only one of the four inputs to the trigger selector circuit is used. This should be adequate for a start pulse for the HC-1 to S2 time spectrum. The S3-S2 delay measurement can be done better and care will be required whenever these data are needed. The remaining times are recorded only for monitoring purposes. They can be used as an independent check on the helical chamber time resolution and may also indicate malfunctions of the helical chambers.

F. Timing Considerations

The electronics should be set up to be 100% efficient for all π 's and for protons of range greater than $\sim 1 \text{ gm/cm}^2$. The choice of 100 ns for the basic resolving time of the helical chambers is based on 63 ns maximum time difference between pions and protons, and 35 ns for resolving time of the chambers. The gate time for pulse height measurements at the focal plane of the spectrometer can be somewhat shorter since the start of the gate will be derived from the S2 pulse. The veto counter time resolution should be 50 ns or greater in order to guarantee that events scattered from the pole tips, etc., can be vetoed independent of the type of particle involved.

One additional problem was discovered when laying out the block diagram (Fig. 2). Since a slow coincidence between S1L-S2L and Chamber Coinc is desired, the possibility exists that two or more S1L-S2L pulses can occur during a single chamber coincidence pulse. Since this would confuse the

later circuits, a dead time of 100 ns was built into the S1L-S2L circuits. Since this dead time occurs only on doubles, it probably will not be significant compared with the helical chamber dead times which occur on singles. A 100 MHz scaler is set up to monitor this loss. However, it should be used with caution since the helical chambers will record two tracks in many of the cases in which an event would be lost. We must not count these losses twice.

G. Test Pulse

A test pulse is provided as part of the helical chamber interface. Under the control of the computer it is possible to inject a pulse into any amplifier input. This will be used both as a check for circuit failure and as a calibration for the helix delays. In order to provide for a trigger to start the TDC's with the test pulse, an OR circuit has been provided to allow triggering on either the test pulse or event. Scalers are provided to keep track of the total number of each type of pulse which triggers the readout system.

H. Timing of Helical Chamber Stop Pulses

The taps on the helix will be 2.0 cm apart. With a delay/unit length of 17 ns/cm, the maximum delay between the anode pulse and the last stop pulse will be 51 ns. Since the TDC's will start with a time related to the S2 scintillator pulse, we must allow 63 ns for the time-of-flight difference between pions and protons plus 35 ns for chamber resolving time. In order to allow some margin for time difference between amplifiers, we will need to use a full scale range of ~ 200 ns. This means that the range of the TDC's will have to be modified from the LRS standard. With 208 ns full scale, we will still have 0.4 ns resolution which is good enough to get 0.25 mm resolution on each chamber. We will need nine bits to record raw data, however only eight bits will be needed for the three time differences which are used to calculate position.

I. S3 Option

It may prove important to use the S3 circuit in the trigger in order to reduce accidentals in the first chamber. A 4-input and circuit (LRS 364) has been provided so that this can be accomplished without otherwise changing the logic. It may be necessary to use S3 to reduce the muon contamination when we operate without a differential Cherenkov counter.

J. Not Yet Considered

We have not yet considered a method of starting and stopping runs in synchronism with the accelerator pulses. Nor have we considered the circuitry necessary for generating the beam gate during a run or during manual operation.

IV. EQUIPMENT LIST

In Table II we have included an equipment list of all the NIM, CAMAC, and test electronics for EPICS. Also included is a request for equipment from LEEP submitted August 21, 1972.

TABLE II
EPICS Electronics Equipment List
August 21, 1972

I. Test Equipment

2	Tektronix 454A scopes	3320	6640
1	Phillips PM5770 pulser	1400	1400
1	PHA (existing)	nc	nc
1	Quad Delay Box	600	600
1	DVM (existing)	nc	nc

II. Fast Logic - NIM

5	EG&G T121/NL Discr.	690	3450
4	LRS 364 Dual 4-fold	595	2380
3	LRC 322 Quad 2-fold	695	2085
1	LRS 128 Dual fanout	400	400
1	NIM Bin (2 others on hand)	570	570

III. CAMAC

1	EG&G C212	520	520
4	LRS 2226A Quad TDC	1320	5280
1	LRS 2248 Octal ADC	1950	1950
2	LRS 2550B Quad 100 MHz Scaler	870	1740
8	Cheap scalers	200	1600
1	CAMAC crates	2995	2995
1	Scaler Display System	5000	5000

IV. Slow Logic

2	Ortec 439 Current Digitizer	960	1920
1	TAC (existing)	nc	nc
1	Lin Gate & Stretcher (existing)	nc	nc

V. High Voltage & Distribution

2	3kV PMT supplies	395	790
4	5-channel PMT distribution	250	1000
2	5kV MWPC supplies	619	1238
2	6-channel MWPC distribution	250	500
TOTAL			42058

TABLE II (continued)

EPICS Equipment Pool Request
Revised August 21, 1972
Request Form for Electronics from LEEP

<u>Type</u>	<u>Typical Model</u>	<u>Cost</u>	<u>No. Req'd</u>
I. Test Equipment			
150 MHz Portable Scope	Tektronix 454	\$3320	2
500 MHz Scope, plugins	Tektronix 7000 series	5850	
100 MHz Pulsar (see also Sec. II BNC 8020)	Phillips PM-5770	1400	1
1-1000V, 5-1/2 digit DVM	Dana 5330/700	2070	1 (existing HP acceptable)
10 kV Power Supply, 10 mA	Fluke 410B	950	
256 Channel PHA	Northern Sci: NS-633	2860	1 (existing 4096 channel pre- ferred)
Electrometer (see also Sec. IV Ortec 439)	Cary 401	2350	
Dual 100 MHz Nixie Scaler	Jorway 800	2160	
Other (specify)	Quad Delay Box		1
II. Fast Logic - NIM			
70 MHz Octal Disc (100 mV)	EG&G T108	795	
150 MHz Quad Disc (50 mV)	EG&G T121/NL	690	5
150 MHz Quad Disc (100 mV)	LRS 321B	695	
200 MHz Dual Disc	CRN 154	675	
100 MHz Quad Zero-x Disc	EG&G T140/NL	760	
Other (specify)			
Dual 4-fold Coinc	LRS 364	595	4
Dual f-fold Coinc	LRS 365	795	
Quad 2-fold Coinc	LRS 322	695	3
Other (specify)			
Dual 4-fold Logic OR	EG&G OR102/NL	340	
Dual 5-fold Logic Fanout	EG&G F108/NL	340	
Dual 8-fold Linear Fanin	LRS 127L	400	
Dual 8-fold Linear Fanout	LRS 128L	400	1
Other (specify)			
Dual Linear Amplifier	LRS 133B	495	
Other (specify)			
Delay and Gate	EG&G GD150	725	
Gate Generator	EG&G GG200	635	
Other (specify)			
Pulse Generator	BNC 8020	850	
NIM Bin (2 amps±12V, 1 amp±24V)		570	1
Other (specify)			

TABLE II (continued)

III. CAMAC

Coincidence Buffer	EG&G C212	\$ 520	1
Disc/Coin/Latch	Jorway 64	1595	
Other (specify)			
Output Register (TTL)	Jorway 40	495	
Output Register (NIM)	Jorway 41	395	
Input Register (TTL)	Jorway 60	595	
Input Register (NIM)	Jorway 61	450	
Priority Interrupt Register	Jorway 64	550	
Other (specify)			
Quad Time to digital	LRS 2226A	1320	4
Octal 8-bit ADC	LRS 2248	1950	1
12-bit ADC	Jorway 30	775	
Other (specify)			
Quad, 100 MHz, 24-bit scaler	LRS 2550B	870	2
10 MHz, 24-bit scaler, 30 channels			8
CAMAC Crate with Power supply and Type A Controller		2995	2
Digital-to-Analog Converter			
Other (specify)			
Franch Driver	LAMPF-MBD		1
Computer	PDP-11/20		
Stand-alone Readout System			
Other (specify)	PDP-11/45, etc.		1
	Scaler Display System		1

IV. Slow Logic - NIM

Detector Bias Supply	TC 908	880	
Slow Logic Unit	TC 404	640	
FET Preamp	TC 161A	500	
Preamp Power Supply	TC 920	295	
Active Filter Linear Amp.	TC 203	570	
Linear Gate	TC 303	500	
Delay and Gate Gen.	TC 410	265	
Timing SCA	TC 445	750	
Ref. Pulser	TC 813	200	
Timing Pickoff Control	ORT 403A	255	
Current Digitizer	ORT 439	960	2
			(Prefer MP-3 design)
Sum Invert Amplifier	CAN 1465	180	
Const. Frac. Timing Disc	ORT 463	550	
Timing Filter Amp.	ORT 454	345	
Fast Coinc	CAN 1441	450	
Delay Amp.	ORT 427A	390	
Others	Existing TAC		1
	Existing Linear Gate and Stretcher		1