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Problems Associated with Pulse Charged Capacitor Banks*

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Pulse charging of capacitor banks is not a new technique. There are, however, two distinct areas in which pulse charging should be considered, namely:

- 1) Capacitor banks which are designed to be charged in a time which is too short to be convenient using a conventional D.C. power supply directly.
- 2) Capacitors which are charged, due to failures in the circuit, to voltages which may be considerably higher than the system is designed to handle.

Pulse charged banks have been used at Los Alamos for several years on such machines as Scylla I, II, and III and Columbus II to reduce insulation requirements, switch pre-fire problems, and improve capacitor life. Each of these machines was operated in the 100 KV region and each was charged with a five stage Marx circuit.

If one ignores circuit resistance, Fig. 1g, then when SW_1 is closed, V_1 and V_2 should be 180° out of phase and oscillate about the quiescent voltage V_q where

$$V_q = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2} \quad (1)$$

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If $C_1 = C_2$ and the initial charge on V_2 , $V_{2_0} = 0$, then $V_q = 0.5V_1$, Fig. 1a, and $V_2 \text{ max} = V_1 = 2V_q$. If V_{2_0} has any value other than zero, then

$$V_2 \text{ max} = 2V_q - V_{2_0}. \quad (2)$$

For instance let $C_1 = C_2$ and $V_{2_0} = -V_{1_0}$, Fig. 1d, then $V_q = 0$ and $V_2 \text{ max} = 2V_q - V_{2_0} = V_{1_0}$. It can be shown, Fig. 1b, that as C_1 approaches infinity V_q approaches V_{1_0} and $V_2 \text{ max}$ approaches $2V_{1_0}$ provided $V_{2_0} = 0$. From Fig. 1d, e, and f it becomes apparent that when $V_{2_0} = -V_{1_0}$, V_q approaches V_{1_0} as C_1 approaches infinity and $V_2 \text{ max}$ approaches $3V_{1_0}$. In all cases, however, $V_2 \text{ max} = V_q - V_{2_0}$.

The maximum energy stored in L_1 is the difference between the initial energy stored in C_1 and C_2 and the energy stored in C_1 and C_2 at V_q or

$$V_{L_1} = \left(\frac{1}{2} C_1 V_1^2 + \frac{1}{2} C_2 V_2^2 \right) - \frac{1}{2} \frac{(C_1 V_1 - C_2 V_2)^2}{C_1 + C_2}$$

$$V_{L_1} = \frac{1}{2} \frac{C_1 C_2 (V_1 - V_2)^2}{C_1 + C_2} \text{ joules.} \quad (3)$$

The maximum energy stored in L_1 increases as the difference between V_{1_0} and V_{2_0} increases. In designing pulse charging circuits one must take into account the magnetic forces implied by the energy stored in the inductor L_1 and build the inductor to mechanically withstand these forces.

One can rearrange the circuit, Fig. 2, such that the load capacitor, C_2 , has a D.C. ground to the hot terminal. From a safety point of view, such a system is attractive because C_2 is effectively short circuited except for the very short time it takes to charge C_2 and discharge it into a load. For effective operation L_2 should be much larger than L_1 so that very little current will flow through L_2 . In practice, if the charging period is.

one-tenth that of the circuit C_1 , L_2 , SW_1 , no problems should be encountered. In operation C_1 is charged to V_0 , when the switch is closed V_1 goes from zero to $-V_0$ and V_2 starts to charge. V_2 max will approach $-V_0$. Note that the input voltage was V_0 and C_2 is charged to $-V_0$. If one assumes the initial conditions to be those voltages which appear the instant after closing the switch, then formula (2) gives a very good approximation of V_2 max.

In machines using pulse charged capacitor banks the load capacitors, C_2 , Fig. 1g and Fig. 2, are discharged into the machine load in a time which is short compared to the charge time.

If one wishes to charge C_2 to a higher voltage than the initial charge on C_1 , then C_1 can be increased in capacity, Fig. 1b. As stated earlier V_2 can approach twice the initial charge of V_1 . However, when C_1 is larger than C_2 , a charge remains on C_1 when C_2 is charged to its maximum. This charge will be fed through L_1 , and the load into which C_2 is discharged. The time constant of this circuit will be long compared to the normal period of the machine (C_2 and its associated load), being dominated by C_1 and L_1 .

If more voltage is needed than is convenient with single stage systems, Fig. 1g and Fig. 2, Marx circuits can be used. Fig. 3 shows a typical two stage grounded Marx circuit. The resistors can be replaced with inductors on the ground side of the circuit if one wishes to keep a low resistance D.C. ground on the hot terminal of the load capacitor. Here at Los Alamos five stage grounded Marx circuits have been used with inductive isolation (inductors replacing the resistors shown), on a $\frac{1}{4}$ Mj bank using spark gap switching. The effective series capacity of the Marx should, of course, equal the load capacity in which case V_2 max = $-V_0 n$ where n = number of stages. Fig. 4 shows a conventional two stage Marx circuit. Note that V_2 max = nV_0 .

Practical Marx circuits have been built at Los Alamos with the following parameters:

Output voltage -- up to 120 KV into a matched load

Number of stages -- up to 10

Types of switches -- size A ignitrons; 3 and 4 element spark gaps

Isolation between stages -- resistors and inductors.

At Los Alamos, we have also encountered capacitors which have been inadvertently pulse charged due to circuit misbehavior. This problem occurs in modular systems where each module is independently switched into a common load, Fig. 5.

C_1 through C_{10} represent modules of one or more capacitors in parallel. L_1 through L_{10} represent the inductance of each module and consist of inductance of the switch, capacitor(s) and cables. L_{load} is the load inductance. For purposes of discussion let C_1 through C_{10} be 10 μ f each, L_1 through L_{10} 0.1 μ h each, L_{load} 1.2 μ h, and the initial charge V_0 on each module +10 KV. If one closes SW_1 through SW_9 but leaves SW_{10} open, a voltage will appear across L_{load} which is equal to V_0 less the drop across the parallel inductances L_1 through L_9 . The wave shape will be a cosine wave with a period determined by C_1 through C_9 , L_1 through L_9 and L_{load} . At $\frac{1}{2}$ period the voltage will be $-V_0 - V_{L_1}$ through $-V_{L_9}$. If the source inductance L_1 through L_9 is small compared to L_{load} as in the example shown, then V_{load} max will approach $-V_0$, and the voltage on C_{10} is $+V_0$. If SW_{10} closes, then a voltage equal to $2V_0$ will be applied across L_{10} and the voltage on C_{10} may approach $3V_0$, Fig. 5f.

This type of pulse charging is not uncommon and the results are often dramatic. The time required to charge C_{10} is determined primarily by C_{10} and L_{10} . Thus, the charge time may be short compared to the normal discharge time. The current through L_{10} may be much larger than normal, resulting in cable failure due to magnetic forces larger than the cable can handle.

These forces are proportional to I^2 , so large increases in current become a real problem. Capacitor failure is probably the most usual problem resulting from this type of pulse charging. The corona in capacitors increases as a function of both voltage and frequency. The peak to peak voltage across C_{10} approaches $4V_0$ and the frequency is, of course, higher than the normal discharge frequency, therefore capacitor failure is almost assured.

The best way to overcome this problem is to use switches which can be relied upon to fire at the proper time or not fire at all. If, for example, SW_1 through SW_{10} had all closed at the same time, no problem would have occurred, or if SW_1 through SW_9 had closed but SW_{10} had not closed at all, no problem would have occurred either.

In practice this type of pulse charging has occurred in systems using ignitron or spark gap switching. Improved switches have increased the chances of successful operation, but one should keep the problem in mind when designing modular systems.

Fig. 1

Fig.2

Fig. 3

Fig. 4

Fig. 5