ALPHECHON: EVALUATION OF A
DEVELOPMENTAL VIDEO STORAGE TUBE

MASTER

by

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PREFACE

The Alphechon is a developmental storage tube made by RCA, Lancaster, Pa., as Type C22017A. It was designed for non-destructive, continuous read-out of information presented as a message on a standard TV frame, with the purpose of providing real time, moderate resolution video storage. It was decided to construct a video storage system about the Alphechon, and evaluate its performance for possible use in the On Line Fourier Transform (OLFT) system.

Circuit schematics for a TV frame storage system were provided by RCA with the data sheet for the Alphechon. These circuits were constructed and were found to be lacking in stability, ease of adjustment, and video resolution. The author then constructed a more complex system which eliminated many of the shortcomings and problems of the RCA system, so that the performance of the Alphechon alone could be judged. Improvements ranged from minimizing the number of power supplies required by the system, to the use of feedback in the circuits driving various elements of the Alphechon. Drift of the adjustments was minimized, more parameters affecting the operation of the Alphechon were made adjustable, and the bandpass of the video processing circuits was increased. Additionally, the system was made compact, and considerably more rugged and portable than the first system.

Despite all these changes, several problems were encountered within the Alphechon tube itself. The focus of a stored TV frame varied due to the non-planarity of the Alphechon Target element, and limited resolution to 250 lines at the center of the stored TV frame. The read-out duration was one minutes. Arcing inside the Alphechon tube often destroyed a stored TV frame.

It was decided that the Alphechon was too limited in its performance to be of use. Recently, more advanced versions of a storage tube have been developed and marketed by various companies. The circuitry developed for the Alphechon will be useful for the evaluation of these new types.

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1. INTRODUCTION

In the OLFT (1) system there is a need for a TV frame storage device to provide video input and also to store a transformed or filtered TV frame. The storage device is required to hold a single TV frame, and instantly provide continuous read-out in the form of a complete, composite video signal for at least several minutes. The most obvious device for this would be a video disc. The primary reason one could not be used was its cost.

In mid-1968 RCA released specifications (2) on a new development video storage tube, the Alphechon. It is a secondary emission storage tube intended for storage and non-destructive read-out of a TV frame. Its major intended market would be graphic computer display terminals. Claimed resolution was 500 lines; claimed read-out time was greater than two minutes. Also, due to the storage mechanism of the Alphechon, selective erasure and rewriting of fractions of a stored image was a possibility. Additionally, the Alphechon is inexpensive and its structure is quite similar to that of a vidicon so standard deflection systems could be employed. Thus, the Alphechon had a fair potential for information display systems, and unknown potential for the OLFT system.

It was decided to construct a video storage system about the Alphechon, and evaluate its performance. Circuits for a TV frame storage system were provided by RCA with the data sheet for the Alphechon. This provided a basis for a first evaluation system. Problems with the RCA design led to the design and construction of a second system by the author. After a discussion of the physical operation of the Alphechon tube, these two systems will be described, and then the performance of the Alphechon will be discussed.

2. OPERATION OF THE ALPHECHON

The Alphechon is constructed almost identically to a vidicon. The most apparent external difference between the Alphechon in Figure 1 and a vidicon is the second base on one end of the Alphechon where light would have entered the vidicon. The electron optics are essentially unchanged. An electron beam is formed through an orifice in the Intensity Grid G1, enveloping the Cathode. The beam is focused electrostatically by G2, G3, and G4. It is also focused magnetically by a solenoid surrounding the Alphechon tube. The axial magnetic field from this solenoid causes the electron beam to spiral down the tube through one turn of a helix, and form an image of the G1 orifice on the Target. Since the Target is a high impedance material, the electron flux reflected from the Target is collected primarily by G4. Because the electron optics of the Alphechon and the vidicon are so similar, a standard vidicon deflection system could be used.

The major internal difference between the Alphechon and the vidicon is the Target. The Alphechon Target is a plastic coated screen mesh. It is drawn taut on a frame supported by the rear base assembly. Electrically, the Target is a conductive plane covered by a high impedance material.

Images are stored on the Target by secondary electron generation. Figure 2 represents the typical relation between the ratio of the number of secondary electrons (n_s) to the total number of primary electrons (n_i), and the energy of the electron beam. This energy is actually the potential difference between the Cathode and the Target. The three regions of interest in Figure 2 are labeled A, B, and C. Operation of the Alphechon at any Target potential other than the origin, V_p , or V_s generates stored charge on the screen. If the charge is stored by operation in regions B or C, it will

Figure 1. The Alphechon

Figure 2. Typical Secondary Electron Characteristics

be imbedded in the Target material, and low electron densities will not seriously erode the magnitude of the charge. Operation of the Alphechon in region A only generates a surface charge which follows the electron beam, and is not permanently stored.

The amount of charge stored, for a fixed electron beam intensity, depends entirely upon the Target potential. For example, operation of the Alphechon Target potential at V_3 will result in a stored charge at a potential that is $V_3 - V_s$ below the Target potential, and negative charge is stored. Operation at V_2 will store charge at a potential that is $V_s - V_2$ above the Target potential, and positive charge is stored.

A TV frame is written into the Alphechon Target by operation in region B. This minimizes the heat dissipated on the Target, and lowers the voltage swing required of the Target voltage driver. The magnitude of the stored charge can be modulated as the Target is scanned either by modulating the electron beam intensity through G1, or by modulating the Cathode potential, which is equivalent to modulating the Target potential.

Once an image has been written onto the Target, it is read-out by operation of the Alphechon Target potential in region A. The electron beam intensity is low. No charge is stored, and due to the high impedance of the Target material, the stored charge remains unchanged for several minutes. If the average Target potential is V_1 , the spot on the Target which the beam impacts will be held at a potential that is V_1 with respect to ground. The Target mesh is connected to a high impedance video amplifier. As the Target is scanned, the written charge pattern will cause the mesh voltage to fluctuate. This signal, when amplified, provides the reconstruction of the stored TV frame.

Erasure of the stored charge is accomplished by operation of the Target potential in region A also. The Alphechon is driven into saturated beam current by holding the Intensity Grid at the Cathode potential. The high electron density which this generates on the Target causes rapid erosion of the stored charge through the high impedance Target material. The Target potential must be low to preclude damage of the Target from heat.

Many of the physical parameters of the Alphechon tube affect its operation in Write, Read, or Erase Mode. The conductivity of the Target material influences the effectiveness of erasure and the length of read-out time. This conductivity is compromised for these. The Target mesh must be planar to avoid any change in the focus as the Target is scanned. Heating of the Target during continuous operation can cause the Target to flex, causing the focus to drift.

Since variation of the Cathode voltage affects both the energy and the current of the electron beam, the density of the stored charge is much more sensitive to modulation of the Cathode than modulation of G1. Also, the lower impedance of the Cathode affords a higher bandwidth from a driver with fixed parasitics. For these reasons, the Cathode, rather than G1 is modulated in Write Mode.

3. SYSTEM DESIGN

3.1 Alphechon 1

With the release of developmental data, RCA also presented a set of typical circuits (2). These were constructed in order to evaluate the performance of the Alphechon and were found to have many shortcomings. Several sections of the RCA design dissipated a great amount of heat, causing voltage adjustments to drift. Also several of the voltage adjustments interacted, making adjustment and alignment of the system an iterative process. Several parameters affecting the performance of the Alphechon tube were not adjustable. Others were not independently adjustable for each of the Read, Write, and Erase Modes.

The RCA system drifted so severely that performance could not be guaranteed for longer than five minutes. The lack of independent adjustments made operation of the system very tedious. It was concluded that this first Alphechon system did not provide an adequate means of measuring the performance of the Alphechon. The system did demonstrate shortcomings which a new system should avoid. Such a system should incorporate the following features:

1. All voltage adjustments should be completely independent.
2. All voltage adjustments should be independently adjustable for Read, Write, and Erase Modes.
3. Additional parameters should be made adjustable. These include the driven impedance connected to the Target in Read Mode, and bias on the Accelerator Grid G2.
4. All adjustments should be stable. Long term drift should be limited to 2%.

5. The number of power supplies should be minimized.

6. All video circuits should have a minimum bandwidth of 4.5 MHz.

3.2 Alphechon 2

The system for a frame freeze system built around the Alphechon is shown in Figure 3. With this system, very few parameters affecting the storage tube's operation are fixed. It was decided to modulate the Cathode voltage rather than the Intensity Grid voltage in Write Mode. Also, Erase Mode lasts for one TV frame. More frames could be required should erasure not be complete in one frame.

The Cohu deflection system (3) was selected to eliminate unnecessary complication of the design of the system. The Cohu system was intended for closed circuit TV cameras using a vidicon. The full system for a camera consists of at least four circuit boards. The names and functions of these boards are:

SYNC generation of standard synchronizing waveforms for a 525 line interlace TV system.

DEFL generation of driving voltage for the vertical deflection coil, and input to the HORZ horizontal driver board.

HORZ located near the deflection coil, drives the horizontal deflection coil.

VIDEO amplifies the video from a vidicon Target, mixing in synchronization waveforms to form a complete, composite video signal.

The Cohu system also allowed the use of a Cohu camera for video input to the Alphechon, since the two deflection systems are compatible.

In addition to the deflection coils enveloping the Alphechon tube in Figure 3 are the Alignment Coils and the Focus Coil. Both are driven from

Figure 3. System Block Diagram

current sources. There are five main power supplies plus an adjustable bias supply driving the Accelerator Grid G2. The bias supply was provided to extend the focus range, if necessary.

The "Erase/Write/Read Gate Generator" produces a sequence of signals causing the various voltage drivers to switch levels. These are logic signals; they are not amplified by the drivers. The actual operating voltages applied to the tube elements are determined inside each driver. The Erase/Write/Read sequence (a refresh cycle), shown in Figure 4, is initiated by an external signal, a push button, or an internal clock with a period adjustable from a second to two minutes. This sequence is synchronized with the vertical drive pulses from the deflection system.

Video from the "Target Driver/Video Amplifier" in Figure 3 is referred to as raw video. It is mixed with synchronization signals by the "Processing Amplifier," which is actually the Cohu Video Amplifier supplied with the Cohu deflection system. This amplifier also blanks the video in Erase and Write Modes.

The circuits which form the core of the Alphechon system in Figure 3 are the "Cathode Driver," the "G1 (Intensity) Driver," the "G3 (Focus) Driver," and the "Target Driver/Video Amplifier". In Figure 4, a summary of the approximate, required waveforms is presented. All are switched dc voltages with two exceptions: The Cathode in Write Mode, and the Target in Read Mode. In Write Mode the Cathode is driven by at most 75 Vpp of input video derived from a 1 Vpp input signal. In Read Mode, the Target is connected to a high input impedance video amplifier and an adjustable dc bias. Some experimentation was performed in an attempt to optimize the input impedance of this amplifier, yielding 100 k as a non-critical, optimum value.

Figure 4. Element Voltage Summary

To ensure the required stability, these circuits were designed using the Erase/Write/Read signals as logic signals. That is, these signals are not amplified by the drivers; they switch trimpots into and out of the driver circuits. The adjustment of these trimpots determines the output levels of the drivers.

Within most of the drivers, feedback from the output was used to reduce noise, drift, and enhance stability. Feedback also improves the switching speed of the drivers. The use of servo design techniques allows the drivers to have low output impedance without the expenditure of large amounts of power, further reducing drift and easing power supply requirements.

Feedback was not used in the Target Driver, however, since a very high impedance (the Target) is being driven. Feedback also does not appear in the Cathode Driver, since the required bandwidth of 4.5 MHz would cause severe instability problems.

4. CIRCUITS

4.1 G3 Driver

The Focus Grid (G3) driver provides a voltage adjustable from 200 to 450 volts with a stability of 1 volt. In Erase Mode, it has to deliver about 50 μ A. In other Modes it is relatively unloaded. Switching of voltage levels between Erase, Write, and Read Modes should be completed within one vertical blanking time.

Figure 5 is the schematic of the driver. This approach to switching the voltage adjustment is typical of all the system drivers. The E, W, and R lines are raised to 5 volts sequentially, as shown in Figure 4. Thus, only one of the trimpots is switched into the TR4 emitter circuit at a time. TR4 is a common base current follower; its collector is a current source, adjusted by whichever trimpot is switched on. The linearity of the TR4 current follower is limited only by the alpha linearity of the transistor. Its collector current is divided between the 200 k and the 2 M resistors, providing reasonable operating current for TR4 and minimizing the current required in the feedback path of the TR5-TR6 circuit. These transistors form a high gain amplifier. Current through the 2 M input resistor is matched by that through the 3.9 M feedback path.

The circuit is insensitive to any instability in the 200 volt supply since TR4 appears as a current source. The feedback tends to eliminate drift due to the 500 volt supply or to changes in the driven load. Worst case switching time from 200 volts in one Mode to 450 volts in the next, via passive pull-up through the 220 k resistor, is 20 μ s. Focus voltages differ typically by a maximum of 30 volts, for which the switching time becomes about 2 μ s. The amplifier of TR5 and TR6 minimizes temperature drift,

Figure 5. G3 Driver

since the ΔV_{be} of each tend to track one another and cancel, minimizing the input threshold drift at the base of TR5. The .001 μ F capacitor reduces high frequency noise generated by the video signals in Write Mode.

4.2 G1 Driver

The Intensity Grid (G1) driver provides a voltage adjustable from 0 to -200 volts with a stability of 1%. The Intensity Grid impedance is fairly high so that parasitics are the only challenge to switching times. The driver must supply about -50 μ A in Erase Mode. Since voltage swings are typically 160 volts (see Figure 4), the driver's output impedance during switching must be lower than that required by the Focus driver. This requires that the output be both active pull-up and active pull-down. A quasi-symmetric voltage driver is used.

The input to the driver is generated by switching current source references, as in the Focus Grid driver. In this case (Figure 6), however, a negative going current is required since the driver supplies a negative voltage. The Erase, Write, and Read signals alternately switch off TR4, TR5, and TR6. TR7 buffers the reference voltage that supplies the trimpots. Current is supplied to the driver through the two 6.8 k resistors and 100 k trimpot of the transistor which is switched off. TR8, TR9, TR10, and TR11 form a high gain amplifier with input at 0 volts and output swing from -200 volts to 0 volts. The 190 volt zener diode protects the collector junction of TR9. Feedback comes through the 330 k resistor on the output of the quasi-symmetric driver formed by TR10 and TR11. A "keep alive" resistor removes oscillation due to the crossover distortion of the driver. The .0068 μ F capacitor helps stabilize the driver and keeps the output impedance low at high frequencies. The circuit of TR8 and TR9 reduces temperature drift of the output due to V_{be} drift of TR8. The emitter of TR10 is held

Figure 6. G1 Driver

0.7 volts above -200 volts to enhance switching time, which is near $5\mu\text{s}$ for large voltage swings.

4.3 Target Driver

The Target driver provides from 15 volts to 200 volts in Erase and Write Modes. In Read Mode, however, the Target must drive a high impedance video amplifier. The output from the Target is typically $\pm \frac{1}{2}\mu\text{A}$ with 10 pF of parasitic capacitance. It is essential that the low impedance voltage driver be completely isolated from the Target in Read Mode. Also, the amplifier must be protected from the large voltage swings on the Target in Erase and Write Modes, and recover moderately fast.

The Target driver is shown in Figure 7. TR1 and TR2 switch trim-pots which act as current sources as in the other drivers. TR3, switched on in Read Mode, connects a 6.8 k resistor into the TR4 emitter circuit, which saturates TR4.

In Erase or Write Mode, TR4 is a common base current follower, and the Target voltage appears on its collector. Buffered by TR5, this voltage forward biases D1. Since the Target is a very high impedance, a load must be provided to keep TR5 and D1 active during down-going voltage swings. For this, in Erase or Write Mode, TR7 is on; TR8 becomes a current source and $3/4\text{ mA}$ flows through D2, keeping D1 and TR5 active.

In Read Mode, TR4 is saturated, holding the anode of D1 at 10 volts. Simultaneously, TR8 is off, allowing the Cathode of D2 to rise to 200 volts. Thus, the junction of D1 and D2 is connected to two reverse biased diodes, the Target, a bias source, and the input to the video amplifier. The 100K resistor connects the Target to a bias supply, adjustable from 15 volts to 50 volts. It also determines the operating impedance that loads the Target in Read Mode. This adjustment is the Read Mode Target

Figure 7. Target Driver

voltage. The video signal from the Target, dropped across the 100 k resistor, is coupled through a .005 μ F capacitor to the FET input stage of the video amplifier. The gate of TR10 is protected in Erase and Write Modes by D3, D4, and TR9. TR9 is switched off only in Read Mode by TR6. This clamping of the gate of TR10 provides a minimum of offset and overdrive after the Erase and Write Mode cycle.

TR10, TR11, and TR12 form a video amplifier bringing the Target signal amplitude up to 0.1 Vpp. To minimize interference and parasitics, the entire circuit of D1, D2, and TR10 was constructed in an aluminum shell which plugs directly onto the Alphechon rear base (see Figure 8).

The bandpass of the Target video amplifier was measured by driving the Target lead with a 1 M impedance RF current source, with 10 pF of capacitance, to simulate the driving impedance of the target. Typical bandpass is 4.5 MHz. The bandpass will vary with selected 2N3819's (TR10). The recovery time after the refresh cycle is approximately 0.2 second. This allows rapid refreshing of the stored video image for adjustment of the operating voltage levels.

4.4 Cathode Driver

In Write Mode the Cathode requires, typically, 40 Vpp of video. A limiting value of 75 Vpp was selected to allow full adjustment range. In Erase or Read Mode, the Cathode is held at 0 volts. At all times, vertical and horizontal blanking is injected by switching the Cathode to 80 volts. All of this is shown in Figure 4.

Figure 9 shows that the Erase, Read, and blanking voltages are generated by switching the last stage of the video amplifier on and off. This amplifier is allowed to be active only during the time between horizontal and vertical blanking in Write Mode.

Figure 8. Target Driver Front End

Figure 9. Cathode Driver

TR1 buffers the incoming video and provides for polarity reversal. TR2 through TR5 form a high voltage video amplifier, with a quasi-symmetric output stage. The dc level of the output is set by the 2.5 k trimpot in the TR4 emitter circuit. This level, in Write Mode, should be 40 volts. The output swing is clamped at approximately 80 volts through D2.

The base of TR4 operates normally at 0 volts. In Erase or Read Mode, TR6 is turned on, holding the base of TR4 at 4.7 volts. Also, TR8 is turned on, drawing 4.5 mA through the TR4 emitter circuit. This ensures that TR4 saturates.

During horizontal and vertical blanking time TR10 is turned on. This pulls the TR4 emitter to 4.7 volts. TR4 is then turned off in Write Mode as well as in Read and Erase modes. Because the Cathode driver is dc coupled to the Cathode of the Alphechon, recovery from this switching is effectively instantaneous.

Bandpass of the Cathode driver is 5 MHz at half of full gain. Some distortion occurs if the output swing exceeds 60 Vpp, and bandwidth falls to 4 MHz. The Cathode on/off switch is provided to protect the Alphechon target during warm-up, or during possible failure of the deflection system.

4.5 Refresh Cycle Generator

To sequence the element voltages which these drivers generate, the Erase, Write, and Read logic signals must be generated. Shown in Figure 10 is the three-bit shift register which accomplishes this. Its clock input is driven from either an internal 60 Hz synchronization signal from the power supplies, or the vertical synchronization signal from the deflection system. The selected signal is divided by two, (i.e. alternate pulses are selected), since each Mode signal lasts for one TV frame. When a "start"

signal is presented and held at the input to the shift register, it is shifted left every 33 ms through the three stages. By decoding two unique states of these flip-flops, the required signals are generated. These states are unique in that when the "start" signal is removed, the states of the shift register do not match those that were first generated.

The "start" signal is generated either by a pushbutton, or by the long period oscillator, shown in Figure 10. TR1 drives either 0 volts through the 150 k resistor across D1, or 200 volts through the collector resistor and D1. Thus, the driving impedance is symmetric. When switched on or off, the 5 μ F high impedance capacitor is discharged or charged. The NE-2 bulb, with one element biased at 100 volts, is a high impedance threshold device, which fires at 30 volts or at 170 volts. The positive or negative pulse due to the discharge sets or clears an RS flip-flop formed by TR2 and TR3. This reverses the state of TR1, causing oscillation. The period is adjusted by the 2M potentiometer which is the charge path from TR1 to the 5 μ F capacitor. The period is adjustable from a half second to a minute. Since the "start" signal is only the leading edge of the square wave from the oscillator, the period of the refresh cycle is adjustable from one second to two minutes.

4.6 Miscellaneous Circuits

The focus coil must be driven by a stable current source adjustable to 150 mA. It is driven by the circuit in Figure 11. To avoid loading a regulated power supply, an unregulated power source was used. TR3 forms an adjustable current source. The diode in the trimpot circuit cancels thermal drift. The 820 ohm resistor drops a voltage which TR2 subtracts with the voltage dropped across the 25 ohm resistor. The current from the focus coil

generates this second voltage. Again, a diode reduces thermal drift. The error signal from TR2 drives TR1, sinking the current from the focus coil. There is no noticeable drift, and very fine adjustment of the focus is possible.

Each of the alignment coils is driven by a bi-polar current supply, shown in Figure 12. The negative going current source of TR2 is added to the adjustable positive going current source of TR1. The result is a bi-polar current supply with a range of $\pm 20\text{mA}$.

Failure of the sweep of the Alphechon could destroy the target in a few seconds. An indicator of this condition was therefore needed, especially when the sweep was being externally supplied. The duty cycle of a 20 volt sync signal available from the Cohu deflection system determines when either vertical or horizontal sweeps have failed. The duty cycle filter, and regenerative lamp driver are shown in Figure 13.

4.7 Power Supplies

Five regulated power supplies are required by the Alphechon system: 5 volts, -12 volts, 200 volts, -200 volts, and 500 volts. In addition, the Cohu deflection system requires two more power supplies: 3.6 volts and 20 volts. All supplies are referenced to the -12 volt supply, which uses a zener diode for reference, and is therefore the only one which is not adjustable. Figures 14 through 16 describe the power supplies.

In addition, the power supplies contain the sync sources for the refresh cycle generator. The 750/500 volt supply was included to extend the focus range of the Alphechon. It drives the Accelerator Grid (G2). It had been found necessary to drive this grid at 600 volts in an early prototype of the Alphechon to enable writing. In the present system, this is unnecessary, and the G2 grid is driven at 500 volts.

Figure 12. Alignment Coil Current Supply

Figure 13. Sweep Failure Indicator

Figure 15. Power Supply-B

Figure 16. Power Supply-C

5. ADJUSTMENT PROCEDURES

5.1 Adjustments

To simplify operation of the Alphechon system, all significant controls will be catalogued.

Alignment-X	Adjusts current into horizontal alignment coil. Should be adjusted for best intensity.
Alignment-Y	As above, only for vertical coil.
EWR Sync Int/Ext	Selects the source of the sync signal for the Erase/Write/Read signals. When in Int position, the source is the ac line or the vertical sync pulses. When in Ext position, the SYNC in/out connector is the source. This control should never be in Ext position without external sync signals supplied since this may lock the system in Erase or Write mode.
EWR Sync Line/VD	When the EWR Sync Int/Ext switch is in Int position, selects either the ac line or the vertical drive pulse as the sync source for the Erase/Write/Read signals.
Focus EWR	Adjusts the electrostatic focus (G3) in Erase, Write, or Read Mode.
HTR On	Connects ac power to the Alphechon heater if power is on. It should be left off during tests of portions of the system not requiring the Alphechon directly, such as tests for deflection.
Intensity EWR	Adjusts the intensity (G1), adjusting the beam current in Erase, Write, or Read Mode.

Int Sync Phase	Adjusts the phase of the 60 Hz signal, from the power supplies; used as a sync source for the deflection system and the refresh cycle generator.
Int Sync+	Shifts the phase of the Int Sync signal (above) by 180° .
Cathode On	Connects the Cathode to the Cathode driver. When off, no current can flow in the Alphechon, protecting it during warm-up and during tests.
Mag Focus	Adjusts the current into the magnetic focus solenoid.
Power	Turns power supplies on.
Refresh Rate	Adjusts the period between refresh cycles from one second to two minutes. When turned fully counter-clockwise, the refresh cycle is initiated only by the Single Refresh push-button.
Single Refresh	Initiates a single refresh cycle when the Rate control is fully counter-clockwise.
Sweep Failure	Indicates failure of the sweep system - either horizontal or vertical. The Cathode should be switched off immediately. This light normally flashes when the system is turned on.
Target EWR	Adjusts the Target voltage in Erase, Write, or Read Mode.
W Contrast	Adjusts the gain of the Cathode video voltage on the Cathode in Write Mode. This can also be adjusted by varying the amplitude of the video source.
W Bias	Located on the Cathode driver board, adjusts the dc level of the Cathode in Write Mode. This level should be 40 volts.
W Phase	Controls the phase - positive or negative - of the video written relative to the video input.

3.6, 5.0, 20.0,
200, 500, 500/750,
-200

Adjust the respective power supplies. A special card when plugged into the Mag Focus board position makes all these voltages available. They should be periodically adjusted to $\pm 1\%$.

Additionally, several test points exist throughout the Alphechon system.

Focus T.P.	Located next to the Focus EWR controls, presents the voltages being driven to G3.
Intensity T.P.	Located next to the Focus EWR controls, presents the voltages being driven to G1.
Target T.O. 1	Located on Target driver card, presents the Read Mode Target voltage.
Target T. P. 2	Located on Target driver card, presents the Erase and Write Mode Target voltages.

External connections are located on the rear of the Alphechon system.

For the function of all but the following refer to the Cohu deflection system manuals (3).

Raw Video Out	Presents the (approximately) 0.1 Vpp video signal from the Target video amplifier.
Video In	Accepts (approximately) 1 Vpp video as the input to the Cathode driver.
Erase Sync Out	Presents the TTL logic Erase Mode signal. This facilitates synchronizing a scope to display the various test points.

5.2 Comments on Adjustment Procedures

Because 12-space is not a natural human environment, adjustment of the Alphechon system can be quite tedious. There are twelve major adjustments, and the performance of the Alphechon is quite sensitive to some of them. The

adjustment and alignment procedure cannot be regimented into a flow chart form; it is a skill. To aid in training, however, some of the more apparent characteristics will be mentioned.

First are the straightforward adjustments. All power supplies should be adjusted as described previously. The G2 supply is normally set at 500 volts. W bias should next be set so the dc level of the Cathode in Write Mode is 40 volts. The EWR sync should be set to Internal-Vert Drive. The Int Sync Phase is adjusted after the system is functioning to align the vertical position of the Alphechon scan with that of the source video.

Always allow the Alphechon heater to thoroughly warm-up before switching on the Cathode. Establish a pattern on the screen by adjusting the horizontal position until the edge of the Target appears. Adjust the "R" controls to optimize its contrast, linearity, etc. Intensity should be minimal, to enhance the lifetime of the stored image. Then adjust the magnetic focus, and recenter the scan onto the Target.

Main adjustments are performed with the Refresh Period as short as possible, to speed convergence. As an aid, the typical voltages for the elements of the Alphechon are listed in Figure 4. Using a multi-trace scope to display G1, G3, the Cathode and the Target can be of some help.

From this point, only sensitivities can be discussed, since there are innumerable "lost" states into which the Alphechon system can be adjusted. The Write Target voltage should be near 180 volts, and does not affect stored image quality very rapidly as it is changed. The Erase Target voltage, however, is very important. It effectively sets the background charge level of the Target. It should be very slightly higher than the Read Target voltage.

Excessively high contrast due to overdriving the Cathode driver can degrade the picture considerably. It can also reach a level which is past the primary crossover point, causing blotches in the written image. A similar

effect can occur with too high a Write Intensity level. Read Intensity, if too high, will erase the stored image rapidly, since it will essentially simulate Erase Mode. It should be as low as possible (and Read Target voltage as low as possible) but still provide an adequate video signal. Proper adjustment of the gain of the Cohu video amplifier will remove snow and streaking due to overdriving.

Erase Focus is practically unnecessary since the high beam current in Erase Mode is very disperse. Depending upon the intensity and contrast levels of the stored image, often one erase cycle is not adequate to completely remove an old image. This could be eliminated by causing Erase Mode to last for two television frames instead of one but this would exceed the tube specifications.

One important thing to note is that all the Alphechon element voltage adjustments cover a range which ensures no protection against abuse. The severely lost 12-space pilot could easily burn the target. Erase and Write Modes last for a short period, but Read Mode could last indefinitely. It is therefore very important that if no functional video image is being displayed while adjusting the Alphechon system, that an oscilloscope be used to display the various important voltages.

6. PERFORMANCE

Figure 17 is a typical test pattern used as input to the Alphechon system. It is presented here to compare with Figures 18 through 20. Figure 18 is a typical stored frame a few seconds after it was written into the Alphechon. Resolution at the center of the screen is 200 lines. There is a very apparent problem which the Alphechon presents; the image is severely shaded over the area of the screen. It is possible to attain 250 lines at the center of the screen, but overall resolution is no better than 150 lines. It was concluded that the cause of this problem was that the screen was nonplanar. This causes the focus to vary across the screen. In Figure 19 the focus has been lowered to a different portion of the screen. Very few flat regions were found on the Alphechon Target.

The lifetime of a stored image was short. In Figure 20 is the image of Figure 18 after it has been read out for two minutes. Once or twice in every ten minutes of operation, arcing inside the Alphechon would occur, usually destroying any stored image. The cause of this problem has not been determined, but since the Alphechon is being operated within its specifications, the problem must be internal to the Alphechon itself.

A solution to the shading problem is modulation of the Focus voltage by a square law signal synchronized with the horizontal and vertical deflection. Because this would be especially complicated, and its effectiveness is uncertain, it is not justified.

The gray scale of the stored image is relatively poor also. Note that the outer ring of the target in Figures 18 through 20 is almost completely missing. The gray scale can be improved by compromising the stored image strength.

Figure 17. Test Pattern Input

Figure 18. Stored Read Out of Figure 17

Figure 19. Stored Read Out of Figure 17 with Focal Plane Lowered

Figure 20. Figure 18 After Two Minutes of Continuous Read Out

The lifetime of a stored image is typically two or three minutes. If power is removed, the image will last for several hours. Erasure was complete in one TV frame, unless the intensity of the written image was exceptionally high. Then two erasure cycles would be required.

The voltage adjustments are exceptionally stable. When the system is initially powered up, usually only focus and contrast adjustments are required.

7. CONCLUSION

In the period of development of the Alphechon system, several new devices have appeared which should offer better performance. Princeton Electronics Products (4) is offering a device named the Lithocon. It is essentially of the same structure as the Alphechon. The Target is a monolithic silicon structure of islands. It offers a typical resolution of 800 lines, 12 minute read out lifetime, and a signal output of $1.8\mu A$.

Additionally, a new Sylvania type SP5105 Storage tube offers 1000 lines (5). The Target is a similar mosaic of islands, each with a silicon dioxide layer as a secondary emission medium.

Even more recently, Thompson (6) is offering a series of storage tubes with resolutions from 600 to 1200 lines. They require, however, very high target voltages.

It seems that there is an increasing number of new devices available on the market. With this in mind, application of little effort should easily generate a system which will surpass the performance of the Alphechon. The Alphechon system, as it presently functions, was deemed inadequate for OLF.T. The circuits developed around the RCA Alphechon prototype are very functional. They should find use in the construction and evaluation of similar devices.

Figure 21. Overall View of the Alphechon System

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