GATEABLE DELAY-GATE GENERATOR*

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Delay-gate generators are used in abundance in nuclear laboratories for gating of scalers and other instruments and for timing synchronization of slow coincidence pulses. These units are used in a direct mode or in a gated mode in which the output is inhibited unless a second input or gate is present. The unit described here will perform these functions and is relatively simple to construct.

The unit consists of five integrated circuits and a few discrete components. The circuit is shown in Fig. 1. Two Texas Instruments monostable univibrator integrated circuits, SN74121, are the heart of the unit. The delay is produced by using the trailing edge of the output of the first univibrator to trigger the second univibrator. The pulse width of each univibrator is determined by external timing components - 20K potentiometer and switch selected capacitors from 10 pf to 1 μ f. Delay and pulse width can be varied between 30 ns and 10 ms with these component values.

The output of the second univibrator is fed to two T.I. SN74450 driver ICs. The unit fed by the $\overline{Q}$ output produces positive going pulses from ground to 3.9v with the selected delay and width. The unit fed by the Q output produces an output complementary to the above - negative going from 3.9v to ground. This second output is useful for anticoincidence gating. The driver ICs consist of an NAND gate and a discrete

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transistor. With the addition of the second transistor, 2N1711 or 2N3866, the unit is capable of driving a terminated 50 ohm cable.

A standard TTL logic level will trigger the first univibrator. Minimum width of this signal is 30 ns. The univibrator input is protected from inadvertent overvoltages by an SN7404 inverter. In this manner inexpensive inverters will be blown instead of the more expensive univibrators. A simple diode clamp circuit could also be used for this purpose. The gate input is switch selectable. When in the gated position both inputs must be present to produce an output.

This unit can be constructed in a single width NIM bin. NIM voltages must be dropped to +5 volts for the ICs. Power supplies for this purpose are not critical since pulse width is virtually independent of V_{cc} and temperature of the IC. Pulse stability will be limited by temperature dependence of the external timing components.

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FIGURE 1. Delay-gate generator circuitry.

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DRN	10/78
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