PACKARD 45 TO DECTAPE COUPLER

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MASTER

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Introduction

This coupler was designed and built to aid in data taking for meteorological experiments. During the experiments, two Packard model 45 memories (with 4096 channels of 100,000 count capacity) are alternately filled with counting and timing information from sensors in the field. While one of the memories is accumulating data, the other is transferring the stored information to a permanent storage device such as magnetic tape. When accumulation is finished, the two memories interchange roles of accumulating and readout. This process continues until the end of the experiment. Until now, the magnetic tape units had been Packard cassettes which took approximately 30 seconds to transfer data from the memory. The present system uses two DEC* model TU 55 tape transports such as used in their PDP 15 data processing computers. Data transfer now occurs in under two seconds. The only operator assistance required is at startup and to change reels of tape when they are full. In addition to the increase in speed, the reels of magnetic tape are ready for direct processing of the data by a DEC computer.

*Digital Equipment Corp. Maynard, Mass.

Programs for special formatting of the blank tape prior to use and for reading the completed tapes were prepared by Dr. John Kosorok of the Radiological Chemistry section. The special recording format allows data to be stored on the tape faster and in greater quantity than if the standard DEC format were used. The hardware in the coupler is also considerably simplified.

Description of Operation of the Coupler

This section gives a general description of the operation of the coupler. A more detailed description is given later in the section on Discussion of Circuitry. This discussion is aided by the use of Figure one, the timing diagram.

Actual control of the accumulation and readout modes of the Packard 45s and the timing information stored by the 45s is accomplished by an existing controller-timer previously built by Richard Brodaczynski of the 329 Building instrument shop.

The present coupler derives its information on timing initiation and which 45 is being read out from signals generated from the controller. Data information is obtained from a rear connector on the 45 and appears in a "parallel-serial" form. All of the count data for a channel appears in parallel at the connector. When the coupler has used the data, it produces an address advance pulse to increment the channel address by one, and the

next channel's data then appear at the connector. This process moves sequentially or serially from channel 0 to channel 4095.

The initiating event for the coupler is the recognition that a Packard 45 has been switched to the readout mode. The coupler recognizes which 45 is active and stores this information. The TU 55 tape transport is started. After a startup delay of about 200 ms., timing marks are read from the tapes' timing track and are used for all further timing control in the coupler. As this coupler was designed to accommodate model 45 memories with count capacities of $[10^6-1]$ counts, 24 data bits are required (6 decades with 4 bits per decade). These 24 bits are recorded as eight - three bit bytes representing each channel. The bytes are three bits long because there are three channels for data recording on the tape.

The first 24 bits recorded after a tape startup are all binary "1"s, and serve as an indicator showing the beginning of a recording field. This indicator is non ambiguous as the initial formatting mentioned earlier includes setting all data storage locations on the tape to binary "0". It is clear that one must record data only on a freshly reformatted tape, otherwise previously recorded information could make the "beginning of field" marker worthless.

While the 1s are being recorded, the data from channel 0 is waiting in the coupler and as soon as the first eight bytes are recorded, the coupler starts on the next eight that represent the channel 0 data. The 24 bits of channel 0 data are serialized to eight three bit bytes, as mentioned before, and recorded. At the end of the eighth serialization (loading bits 22, 23, and 24), an address advance pulse is emitted from the coupler to the 45, advancing the address from channel 0 to channel 1. After a few microseconds, the channel 1 data appears at the connector and is ready for serializing. This sequence continues, with the address advance pulses being counted by a scaler of 4096 capacity. When the scaler overflows, all channels have been recorded and the overflow indication is used to shut down the recording system. The next initiating event starts the system again.

A "power up" circuit brings the circuitry to a predictable state when the coupler is first turned on. The TU 55 selected as number 8 comes on first.

A scaler is also included to count the number of records put on a tape. After 18 records, the recording is switched to the other TU 55 and an alarm is sounded. The operator must then fit a new spool of tape to the TU 55 and reset the alarm.

Field Operation

After initial setup and interconnection, operation is simple. The coupler, control, and Packard 45s are turned on and the alarm is reset. The TU 55s are powered from the coupler automatically. The select switch of one of the TU 55s should be set to 8, the other should be set to 1. Mount reels of tape, using the local control to wind on leader for two seconds (one thousand, two thousand). Too little leader results in recording starting before the coding already on the tape. Too much leader may result in running out of tape before the end of the last record.

The experiment is started by actuating the control-timer unit, with the coupler automatically following.

When the alarm sounds, the operator resets the alarm with the push button and, using local TU 55 control, winds the rest of the tape onto the right hand spool and removes it. A field label should be affixed at this time. The empty left hand reel is moved to the right location and a reel of formatted tape mounted on the left hub.

Leader is wound on as discussed above. BE SURE to have the TU 55 switches to WRITE ENABLED and REMOTE before leaving the machine. If the data collection time for the Packards is set for 3.2 seconds, the operator has about 57 seconds to complete his tasks.

Discussion of Circuitry

Reference will be made to Figures 1, 101, 102, 103, 104, 200, 201, 202, 203, 204, and 205 which (except for the first) refer to the respective circuit boards. DTL and TTL integrated circuits have been used and power connections have been omitted for clarity. NPN and PNP transistors are 2N 3904 and 3906 respectively and diodes (except one) are 1N4149 or equal. Physical location of the boards is given in the appendix along with the interboard wiring tables. Signal leads of the same name (e.g.: PACK 1) are connected to all boards using that signal. Clarity may be improved by referring to the table of signal leads in the appendix, showing the voltages on and functions of each lead. The transistors will be labeled by board number and transistor number, e.g. 201Q3. The integrated circuit terminals will similarly be noted, as 202IC5, p8. This refers to pin 8 of IC5 on board 202. Boards in the 100 series are for signal conditioning, parallel to serial conversion, and preparation for recording. Boards in the 200 series contain the control circuitry.

100 Series Circuits. A few of the Packard 45s have a memory capacity of 10^6 counts, while the standard units have a capacity of 10^5 counts. In order to make the coupler accept either type of unit, an interface (board 104) was installed. The interface output repeats its data input if the top decade is present and produces a logical "0"

output if the decade is absent. The output of this board is then wired to the input of the 101 boards as is the regular data input. The Packard output format is +5v for logic 1 and about -3v for logic 0. The DTL inputs of the 101 boards can accept the +5v and are protected against the negative voltage by the 1.5k resistor and the diode. The six 101 boards are arranged as gated data receivers for the 48 bits of data from two Packards and also act as level shifters to standard voltage levels. Boards 101-1, 2, and 3 receive the data in ascending order of significance from Packard 1 and boards 101-4, 5 and 6 similarly for Packard 2. When Packard 1 is being interrogated, the gate lines (pin 2) are high and the "low true" data output is fed out to boards 102-1 and 102-2. The two sets of 101 boards have their outputs connected with a "wired-or" and have separate gating, so the outputs are unambiguous. All of the conditioned data for a channel read out appears at once at the 24 inputs of the 102 boards. The low true inputs are inverted and gated by the SER 1 through SER 8 control pulses. Outputs from these gates are also "wired-or" resulting in three output lines (for the three data tracks on the tape) to which are serially connected to the 24 inputs, three bits at a time. The "beginning of record" identification is a channel frame of all "1s" as described earlier. This is achieved here by wiring the outputs of three other DTL gates (on board 203) in

parallel ("or") with the output lines (pins X,Y,Z) of the 102 boards. Timely operation of the board 203 gates forces the three output lines to zero volts (or logic 1), notwithstanding the data then existing from channel zero of the Packard.

The composite set of beginning of record bytes and data are fed to the 103 board where they are processed for the Manchester type of recording*, level shifted to the standard DEC levels of 0 and -3 volts, and sent to the three DEC Manchester read-write boards (G882). On the 103 board, each bit is strobed into a storage flip flop at LOAD time. The complementary outputs are taken from the flip flop and level shifted by Q1 and Q2 to the required DEC levels. At complement or toggle (TOG) time, the TOG pulse changes the state of the flip flop as required by the Manchester process. This completes the recording control for a typical three bit byte. The write portion of the G882 board consists of a gated power amplifier which forces current through the read-record head in one direction or the other as long as it is enabled at pin R. A coupler signal labeled GATE serves this function and will be discussed later.

*For a discussion of this type of magnetic recording, see, for example, the manual for the DEC TCO1 Control Unit, p 3-10, ff.

200 Series Circuits. These circuits accept signals from the external controller and the DECtape and produce the required control sequence of delays, timing, acceptance of data, etc. The entire sequence starts when one of the Packard memories, say number one, is switched by the controller from accumulate to readout mode. The voltage at its J340, p3 goes from about +5V to 0V and this is transmitted via coaxial cable to board 201, pin D. This step is passed by Q1 and Q_{1A} to CF1 (control flip flop #1) via a capacitor so that CF1 is only sensitive to the negative transition. The output of CF1 is buffered by IC2 to produce the PACK 1 and 2 signals which control the data acceptance on the 101 boards. The CF1 outputs are also differentiated to produce the E START signal at IC3, p6. This is a short negative pulse, occurring whenever either Packard is switched to readout. E START is used to advance the record counter on board 205, set two flip flops on board 203, and start a 15 microsecond delay on board 201. At the end of the delay, CF2 is set, producing the START and FIN (finish) levels for use on boards 202 and 205, and to control level shifters Q3 and Q4. The delay is incorporated to give changeover between TU 55 transports an adequate time for completion before actually starting the TU 55 to be used. Q3 and Q4 shift the START and FIN levels to DEC levels and the signals are relabeled GO and STOP. These

are applied directly to the TU 55s and control tape motion in the TU 55 unit selected. CF2 is reset at the end of the record by the negative transition of the END pulse, and tape motion halts.

At START time, the negative transition on the FIN line starts oneshot IC1 on board 202 and sets CF5, a flip flop generating a delay signal. The output of IC1 remains for about 500 microsecond. This is a delay incorporated so that the tape can get "up to speed" before recording starts and provide ample interrecord gap on the tape for use during processing. At the end of this delay, IC2 is started and enables an and gate for 65 microseconds. This allows at least one pulse from IC4 p11 to pass through the gate, starting IC3. After 25 microseconds, the IC3 output resets CF5. The purpose of CF5 is to produce a delay long enough for the tape to get up to speed, and for the delay to end between timing pulses to avoid pulse splitting. The output of CF5 is labeled Total Delay (TDLY) and its termination generates the RESET pulse via Q1.

Q2 and Q3 with IC4 form a level shifter and pulse shaper to translate the square wave from the TU 55 timing track to pulses used as time marks (IC4 p 11). These pulses are gated at IC5 p 6 by the START and TDLY signals and appear as the Tm1 pulses during the time the tape motion is energized and after the delay.

The TMI pulses and their complements are wired to board 203 where they form the basis for the LOAD and TOG pulses which are generated for use at board 103. The TMI pulses fire IC1, which, after 15 microseconds, pulses Q1 to form LOAD pulses. The end of the first 15 microsecond pulse also resets CF4, the EXTRA DELAY flip flop which was set by the ESTART pulse. The EXTRA DELAY, anded with TDLY forms DL2. DL2 is a delay which acts to prevent TMI pulses from becoming TOG pulses until after the first LOAD pulse is generated. The TOG pulses are used for toggling on board 103 and to advance the scale of 8 (board 203) which is responsible for the serializing done on boards 102.

This serializing is done with the help of board 204 which acts as a full decode for the scale of 8 and has as its output the pulses SER1 through SER8. These, as discussed earlier, serialize the 24 bits of data into eight-three bit bytes. The overflow pulses from the scale of 8 form the ADVØ pulse. During this interval, the outputs of IC4 p6,8,11 are low, forming the logic 1 levels used at the input of board 103 as the beginning of record identification.

As TMI pulses are gated by the START and TDLY signals, track to pulses used as time marks. There are LOAD, TOG, ADVØ, and SER pulses exist only during the actual recording interval.

As the TMI pulses during the time of a motion is energized and after the delay to generate ADV1 and ADAV pulses. RESET is used to trigger a 430 microsecond oneshot which gives a delay long enough

to ensure that the beginning of record and channel 0 of the Packard have been recorded. After this delay, the Packard's address is advanced (at ADVØ time) through the rest of the 4096 channels. This is accomplished via the circuits on board 200. There, the ADAV pulses are anded with the appropriate PACK level to provide ADAV 1 or 2 pulses to the Packard from which data are currently being recorded.

ADV 1 pulses from board 201 are routed to the scale of 4096 on board 203 where they are counted. When the scaler overflows (at the end of recording all the channels), the overflow transistion resets CF2 on board 201, stopping the whole sequence.

Board 205 contains some miscellaneous control functions. First is a "Power-up" delay which serves to bring several circuits to a known status when power is first turned on. START is forced low so that neither of the TU 55 transports will start until an appropriate later time. IC2 is triggered which resets the record counter and TU 55 selector. The record counter is a scaler and decoder (IC3,4,6) which emits a pulse at IC4 p11 after 18 records have been written on a DECTape. This pulse fires a oneshot (IC4 p3,6) which resets the record counter, toggles the TU 55 selector, and sets the alarm flip flop, IC5 p8. The record counter is then ready to count records by counting ESTART pulses put onto the alternate TU 55. The TU 55 selector chooses which transport is to be used for recording by means of the SEL 1

or SEL 8 leads. The TU 55 units are paralleled and the unit to be operated is chosen by grounding the SELECT lead corresponding to that unit. The unit selector switches must be set to 1 on one TU 55 and 8 on the other. Unit 8 comes on first when power is applied. Q2 and Q3 are used as level shifters to match up the output of IC5 p5,6 to DEC levels.

The alarm flip flop is reset by the front panel push button which grounds the ALR line, clearing the flip flop. The flip flop drives Q1, a level shifter and driver for the SONALERT*annunciator on the front panel.

A pair of resistors and the -15V supply provide -3V to the FWD line, which causes the TU 55 transports always to go in the "forward" direction. The REV line is grounded as required at the DEC card connector.

IC6 p8, Q4, and Q5 on board 202 are used to keep the GATE lead at 0V except during recording. This lead goes to pin R of the three G882 boards. The GATE lead is at 0V until after the power delay has elapsed, a TU 55 has started, and the time delay finished, at -15V during recording, then reverts to 0V after the last channel has been recorded (at END time).

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APPENDIX

This section contains information on board locations, chassis wiring, signal leads, power supply, a control simulator, Packard settings, and board schematic diagrams.

The ICs used have been 7400 TTL and 15830 DTL series standard devices made by T. I., National, Motorola, and equivalent types may be substituted as necessary. The transistors used have been 2N3904 (NPN) and 2N3906 (PNP). Others with similar characteristics may be used as replacements. e.g. 2N2219 and 2N2905. Diodes are 1N4149 or 1N4148, 914, or 916.

In event of malfunction, the maintenance people working on the unit are asked not to change the under-chassis wiring as this would make further repair very difficult.

The control simulator shown on a following sheet is a small box, obtaining its power from one of the Packards, which supplies control pulses to the PACK inputs of the chassis and signals to the Packard control inputs. Operation of the front panel switch simulates the output of the existing controller for purposes of testing the Packard-coupler-DEctape system.

It is worthwhile for maintenance purposes to buy or build one or two extenders for the circuit boards. These

may be built from the 22 pin edge connector and the MKB-OA circuit board in stores. A pair of DEC W980 extenders can easily pay for themselves, too.

The power supply for the coupler is a DEC H716 supplemented by an included +10V supply and a -15V supply to increase the system capacity as current in the -15V lead may reach 2.5 A. Schematics for these are included.

A small section is included in rough form showing experimentally found conditions of operation for the TU 55 tape transport.

REAR PANEL (COUPLER, BNC, 1340P5)

PACK 1 OR 2

ESTART

START

GO

202 IC1 p6 (START DELAY)

202 IC4 p11 - TIMING PULSES

202 IC2 p6

202 IC3 p6

TDLY

RESET

TM1

LOAD

DL2

TOG

SER 1

SER 2

SER 3

SER 4

SER 5

SER 6

SER 7

SER 8

BEGIN (203 IC3 p8)

ADV 0

DELAY (201 IC4 p1)

ADAV

L.S. BIT, SCALE OF 4096

M.S. BIT, SCALE OF 4096

FIGURE 1

APPRO. FOR CONFORMANCE WITH DESIGN CRITERIA		DATE		U. S. ATOMIC ENERGY COMMISSION	
BY				RICHLAND OPERATIONS OFFICE	
FOR				PACIFIC NORTHWEST LABORATORY	
APPRO				OPERATED BY BATTTELLE MEMORIAL INSTITUTE	
DRAWN				TIMING DIAGRAM	
CHECKED				DUAL PACKARD MODEL 45	
SCALE				MEMORIES TO TWO DECTAPES	
REVISIONS				UNCLASSIFIED	
COMMENT PRT ISSUE NO.		DATE		CHECK PRT ISSUE NO.	
DATE		DATE		DATE	
DRAWING STATUS					
NEXT USED ON

Figure 101

Input Conditioners and Gating

IC1-6 MC846P

Figure 102
Serializer to 3 Bit Bytes

Figure 103

Manchester Formatter and Level Shifter

F 2 In
H 2 Out
J 4 In
K 4 Out
L 8 In
M 8 Out

Packard 1

Packard 2

P 1
R 1 1/2 1/2 1/2 1/2
S 2 1/2 1/2 1/2 1/2
T 2
U 4 1/2 1/2 1/2 1/2
V 4
W 8
X 8
Y 3 1/2 1/2 1/2 1/2
Z 1000 (loads FFs)
1000 (loads FFs)

IC 1-3 7400
IC 4,5 7474

Figure 104
 10^5 Decade Interface

Manchester Formulator and Level Form

Routes ADAV pulses to the Packard being read out.

Figure 200
Control 0

IC1 7400
IC2 7440
IC3 846
IC4 74121
IC5 7410

Figure 201
Control 1

Figure 202

Control 2

Control 1

Figure 203
Control 3

IC 1,2 7404
IC 3-5 7410

Decodes Scale of 8 to SER 1-8 outputs

Figure 204.

Control 4.

IC 1,4 846
 IC 2 74121
 IC 3 8281A
 IC 5,6 7474

Figure 205
 Control 5

Figure 207
Power Supplies

WYLE BIN WIRING

Back (wiring)
view of bin

← Pin A at top

Board Number

Definition: 8Z Means Board 8, Pin Z

Board Locations

Board 1	BLANK	Board 7	101-6	Board 13	BLANK
2	"	8	101-5	14	200
3	101-1	9	101-4	15	201
4	101-2	10	102-1	16	202
5	101-3	11	102-2	17	203
6	104	12	103	18	204
				19	205

Signal Designation

Wire 17D	to	12Y	LOAD
17L		12Z	TOG
15F		3Z, 4Z, 5Z	PACK 1
15H		7Z, 8Z, 9Z	PACK 2
15J		17H 19H	ESTART
15K		16W 19E	START
15L		16F	FIN
15M		17X	END
15R		17M	ADVØ
15S		16K, 17S	RESET
15T		17F	DL2
15U		17W	ADV 1
16Y		17K	<u>TM 1</u>
16Z		17E	<u>TM 1</u>
16X		17J	TDLY
16V		19D	PWR
17T		18D	SC8-1
17U		18E	SC8-2
17V		18F	SC8-4
18H		10H	SER 1
18J		10M	SER 2
18K		10S	SER 3
18L		10W	SER 4
18M		11H	SER 5
18N		11M	SER 6
18P		11S	SER 7
18R		11W	SER 8

Signal Designation

Wire	10X	to	11X, 12D, 17N	BIT 1
	10Y		11Y, 12H, 17P	BIT 2
	10Z		11Z, 12L, 17R	BIT 3
	19F		To PB N.O.	ALR
	19B		To PB COM	(COMMON)
	19J		To SONALERT +	ANNUN
	19C		to SONALERT -	(-15V)
	15P	to	DEC CONN 2A-C	GO
	15N		DEC CONN 2A-D	STOP
	16N		DEC CONN 2B-U	882U
	16P		DEC CONN 2B-V	882V
			2B-R	
	16T		DEC Conn 3A-R	GATE
			3B-R	
	15D		"PACK 1" BNC	PACK 1 J340-3
	15E		"PACK 2" BNC	PACK 2 J340-3
	15B		3 BNC COMMON CONN	(COMM)
	19M		DEC CONN 2A-F	FWD
	19K		DEC CONN 2A-M	SEL 1
	19L		DEC CONN 2A-V	SEL 8
1, J606A-P22			14D	
2, J606A-P22			14E	
	15V		14V	
	15F		14F	
	15H		14H	

DEC CONNECTOR WIRING

Back (wiring)
view of
connector →

A Level

B Level

This is CONN 2B, PIN L
(2B-L)

Connector

4 3 2 1

15F

CARD ASSIGNMENTS

1-A,B	W032	Cable to Tape Heads
2A	W023	TU55-Control Cable
2B	G882	T TRK READ, BIT 1 WRITE
3A	G882	BIT 2 WRITE
3B	G882	BIT 3 WRITE

DEC WIRING

+10 to ALL PIN A (Not necessary on 2A-A, 1A-A, 1B-A)
 -15 to ALL PIN B (Not necessary on 2A-B, 1B-B)
 COM to ALL PIN C EXCEPT on 2A (2A-C) (Not necessary on
 1A-C, 1B-C)

2A-E	to	3A-C	COM (For FWD)
2A-E		2A-H	COM (For all HALT)
3B-C		16-B	>#14 Wire Common Interconnection
2B-C		{ 1A-S, 1A-T	COAX SHLDS TO COM
		{ 1A-K, 1B-E, 1B-L	
		{ 1A-J, 1A-R, 1A-U	
		{ 1B-F, 1B-M	
			HEAD CNTR TAPS TO COM
1A-F		2B-D	T TRK: HEAD TO READ AMP
1A-H		2B-E	
12E		2B-N	DATABIT 1 "1" to WRITE AMP
12F		2B-P	1 "0"
12J		3A-N	2 "1"
12K		3A-P	2 "0"
12M		3B-N	3 "1"
12N		3B-P	3 "0"
2B-K		1B-P	DATABIT 1: WRITEAMP TO HEAD
2B-J		1B-N	
3A-K		1B-J	2
3A-J		1B-H	
3B-K		1B-D	3
3B-J		1A-V	

DATA WIRING

Pack 1			Remarks	7 COND
J606B-1	to	3D	10°-1 R	CABLES TO
2		3F	10°-2 Y	PACK 1
3		3J	10°-4 GR	
4		3L	10°-8 WH	CABLE 1
5		3N	101-1 BLU	
6		3R	101-2 BRN	
7		3T	101-4 BLK	
8		3V	101-8 R	
9		4D	102-1 Y	
10		4F	102-2 GR	
11		4J	102-4 WH	CABLE 2
12		4L	102-8 BLU	
13		4N	103-1 BRN	
14		4R	103-2 BLK	
15		4T	103-4 R	
16		4V	103-8 Y	
17		5D	104-1 GR	
18		5F	104-2 WH	CABLE 3
19		5J	104-4 BLU	
20		5L	104-8 BRN	
21		6D	105-1 BLK	
22		6F	105-2 R	
23		6J	105-4 Y	
J606B-24		6L	105-8 GR	
J606A-23		3B	COM GND	WH
22		14D	AD AV1	BLU
			SPARE	BRN
			SPARE	BLK
6E	5N		105-1	Buffered
6H	5R		105-2	"
6K	5T		105-4	"
6M	5V		105-8	"

Pack 2

6R	7N	105-1	Buffered
6T	7R	2	"
6V	7T	4	"
6X	7V	8	"

DATA WIRING

Pack 2			Remarks	
J606B-1	to	9D	10°-1 R	7 COND
2		9F	2 Y	CABLES TO
3		9J	4 GR	PACK 2
4		9L	8 WH	
5		9N	10 ¹ -1 BLU	CABLE 1
6		9R	2 BRN	
7		9T	4 BLK	
8		9V	8 R	
9		8D	10 ² -1 Y	
10		8F	2 GR	
11		8J	4 WH	CABLE 2
12		8L	8 BLU	
13		8N	10 ³ -1 BRN	
14		8R	2 BLK	
15		8T	4 R	
16		8V	8 Y	
17		7D	10 ⁴ -1 GR	
18		7F	2 WH	CABLE 3
19		7J	4 BLU	
20		7L	8 BRN	
21		6P	10 ⁵ -1 BLK	
22		6S	2 R	
23		6U	4 Y	
J606B-24		6W	8 GR	
J606A-23		6B	COM GND	WH CABLE 4
22		14E	AD AV2	BLU
			SPARE	BRN
			SPARE	BLK

Pack 2

6R	7N
6T	7R
6V	7T
6X	7V

DATA WIRING

101 BDS to 102 BDS

3E	9E	10D	10 ⁰ -1
3H	9H	10E	2
3K	9K	10F	4
3M	9M	10J	8
3P	9P	10K	10 ¹ -1
3S	9S	10L	2
3U	9U	10N	4
3W	9W	10P	8
4E	8E	10R	10 ² -1
4H	8H	10T	2
4K	8K	10U	4
4M	8M	10V	8
4P	8P	11D	10 ³ -1
4S	8S	11E	2
4U	8U	11F	4
4W	8W	11J	8
5E	7E	11K	10 ⁴ -1
5H	7H	11L	2
5K	7K	11N	4
5M	7M	11P	8
5P	7P	11R	10 ⁵ -1
5S	7S	11T	2
5U	7U	11U	4
5W	7W	11V	8

J340 PIN3 IS LOW FOR READOUT, +5 FOR ACCUMULATE

Schematic
CONTROL SIMULATOR

CONTROL SIGNALS

<u>Signal</u>	<u>Boards Using the Signal</u>	
Ser 1	102-1	204
2		
3		
4		
5	102-2	
6		
7		
8		
LOAD	103	203
TOG	103	203
PACK 1	201	101-1,2,3;200
PACK 2	201	101-4,5,6;200
ESTART	201	203 205
START	201	202 205
FIN	201	202
END	201	203
GO	201	
STOP	201	To DEC CONN
ADVØ	201	203
RESET	201	202 203
DL 2	201	203
ADV 1	201	203
AD AV	201	200
882 U	202	
882 V	202	To G882 #1, T. TRK. READ AMP
TM 1	202	203
TM 1	202	203
TDLY	202	203
PWR	202	205
GATE	202	to 3-G882 WRITE AMPS
SC8	203	204
ALP	205	to PB
ANNUN	205	to SONALERT to -15V
SEL 1		
SEL 8	205	→ DEC CONN
FWD		
AD AV 1	200	to PACK 1 PRINT ADV 606A-22
AD AV 2	200	to PACK 2 PRINT ADV 606A-22

J340 PINS IS LOW FOR READOUT, +5 FOR ACCOUNTING

Schematic

CONTROL SIGNALS

TU 55 OPERATING CONDITIONS

(Experimentally determined for use in system design or unit maintenance).

1. WRITE ENABLE switch does not have to be on to move the tape.
2. Pin H (All Halt) of connector A5, W023 must be grounded and one of the positions selected (pin M-V) by grounding for the tape to move.
3. *If the tape is moving and pin H becomes ungrounded, all torque disappears from both motors, leaving the tape free. Turning to stop puts on a drag torque plus a brake.
4. *If the tape is moving and the select line is ungrounded, the tape keeps on moving even if you try to stop it or reverse the direction.
5. About 31 seconds is required to slew through a tape.
6. In the regular stop condition, forward drag torque and the trailing brake are on.
7. If tape is stopped and ground is removed from pin H, the unit stays in stop (with torque and brake).
If start is then commanded, both reels are completely free.

*Moral: Stop the unit before selecting or "all-stop"ing.

8. If unit is stopped and SELECT is ungrounded, it stays stopped and locked. If start is then commanded, no action results.
9. If SELECT is grounded in the GO position or status, the tape starts and will not stop unless ground is applied (as before).
10. Need logic level of about 1 volt to go, ergo -3V is plenty.
11. About 150 milliseconds are required to get up to speed; about 100 milliseconds to stop.

PACKARD SETTINGS

Rear Panel

Address Sw to overflow.

"With Printer" switch down.

Front Panel

Channels per trace - 4096

Initial Channel Sw - all out

Readout limits (Start, Stop). All zeros

Counts full scale - to suit

Vertical display - to suit (probably LIN)

Channel Intensification - LIMITS

Horizontal Expansion - 1

Control Pushbuttons - DIGITAL

Mode - P.H.A.

Arithmetic - ADD

Permanent display - ON

Master Control - AUTO

Destructive - Non Destructive Readout Switch - Destructive