THE ANALYSIS OF AN INPUT BUFFER FOR REMOTE CONTROL OF LOGIC CIRCUITS

by

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DISCLAIMER

ABSTRACT

In logic circuitry, the use of relays, switches, or contacts for control can give incorrect information due to contact bounce. This analysis is of a buffer used to isolate a digital circuit from external noise while allowing remote control. The analysis is made by breaking the circuit operation into three parts -- Delay, Switching, and Recovery -- with a fourth part to describe the effect of noise on the input lines. These four parts describe the limits on the input pulse width and pulse rate for various conditions and give the output pulse which could be expected. Experimental data are used to verify the analysis and give an indication of the possible variations in the circuits due to component changes. The analysis is not a worst-case calculation and does not describe the change of circuit operation due to component variations, but is a method of analysis of an unusual and somewhat unconventional silicon controlled rectifier circuit.

ACKNOWLEDGEMENTS

The writer expresses his appreciation to those people who have helped with the preparation of this thesis; and to the Bendix Corporation whose policies and assistance made this work possible. The writer is greatly indebted to his Advisor, Dr. J.N. Warfield, for his advice, guidance, and encouragement in this project. Special thanks are given to Mrs. W.J. Frisbie for her invaluable aid in typing this thesis. The writer is thankful to his wife, for her patience and helpfulness.

H. G. Thorpe

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CHAPTER I

INTRODUCTION

Statement of the Problem. In logic circuitry, the use of relays, switches, or contacts for control can give incorrect information due to the contact bounce. A circuit may generate two or more outputs for a given input, triggering the extra times on the contact bounce. Logic circuitry may also be triggered with pick-up noise when long lines are used for remote control. Because of this, special circuits are used to serve as buffers between the circuitry being controlled and the contact closure. The buffer circuit to be described is insensitive to contact bounce or noise pickup on long lines and therefore does not require special shielding.

General Description of the Circuit. This buffer, shown in Figure 1, page 2, operates from contact closures to give a pulse output. The Silicon Controlled Rectifier (SCR) is connected common-gate with the input applied to the cathode and a transformer anode load. The transformer acts as a differentiater and gives a pulse on the output winding. The operation of the circuit begins as an input is supplied by the closure of the contacts, S_1. This closure completes a circuit composed of the capacitor, C_1; the timing resistor, R_T; and any line resistance, R_I. The closure of S_1 Starts the capacitor to discharge. When the capacitor discharges to a given voltage level, the SCR switches to its conductive state. This discharges the capacitor, C_2, through the transformer, T1, producing an output to the load,

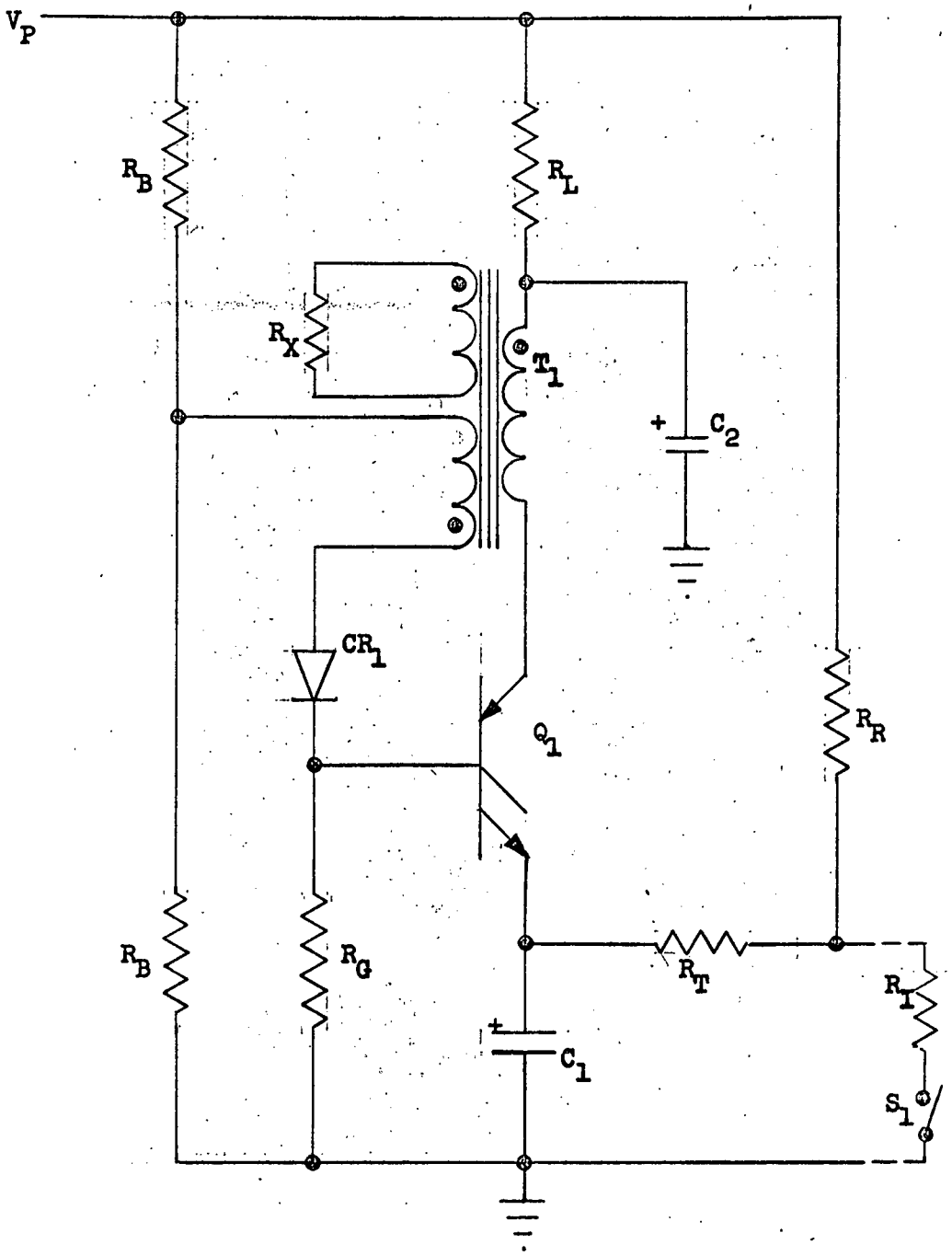

FIGURE 1 Schematic Of An Input Buffer

R_x. The circuit remains in this state with C_1 and C_2 continuing to discharge through the contacts, S_1, until they are opened. When this occurs, the circuit begins to recover to its original state. The SCR will change from its conducting to its blocking state when the current in its anode drops below the hold current and the gate voltage is not positive with respect to the cathode.

The circuit is protected against contact bounce and line noise by the RC network on the input. This insures a single output pulse for each input closure.

Method of Analysis. From the description of the circuit, it is easily seen that the circuit operation can be divided into three periods. The first period is the Delay and is defined as the time from the contact closure of S_1 until the SCR begins to switch. The second period, or Switching period, covers the time between the switching of the SCR and the opening of the contacts. The third and last period is the Recovery period and starts as the contacts open. This period ends either when the circuit is at its original state or the contacts close again. For the circuit to operate properly, the SCR must be allowed to switch to its blocking state.

The analysis is divided into these three states and each is calculated separately. Experimental data were taken and compared to the calculated data. A fourth section is used for the Noise calculations.

CHAPTER II

THE DELAY

The delay is defined as the time from the closure of S_1 to when the SCR starts to conduct. The SCR will begin conducting when the cathode becomes more negative than the gate. The closure of S_1 is a reference point for the calculation and is $t = t_o$.

For calculations of the delay, the portion of the complete circuit shown in Figure 2, page 5, can be used.

For conduction to begin, the gate to cathode voltage must be some value, V_g, set by the particular SCR chosen. The voltage on the gate when the SCR begins to conduct is set by R_B, CR_1, R_G, and the input gate current. If the gate current and the current through R_G are small compared to the current through the bias resistors, R_B, and the voltage, V_D, across the diode, CR_1, is a constant voltage when it is conducting, then voltage on the gate, V_b, is $V_b = \frac{V_P}{2} - V_D$.

The delay, then, is from the closure of $S_1(t_o)$ to $t_1(V_1+V_g=V_b)$. At t_o the voltage on the capacitor is $V_1 = E_1$.

The circuit can now be redrawn as a simple RC network to determine the delay as shown in Figure 3a, page 5.

Using the Thevenin's Equivalent, the circuit, at the closure of S_1, becomes as shown in Figure 3b, page 5.

The equation defining the voltage V_1 is

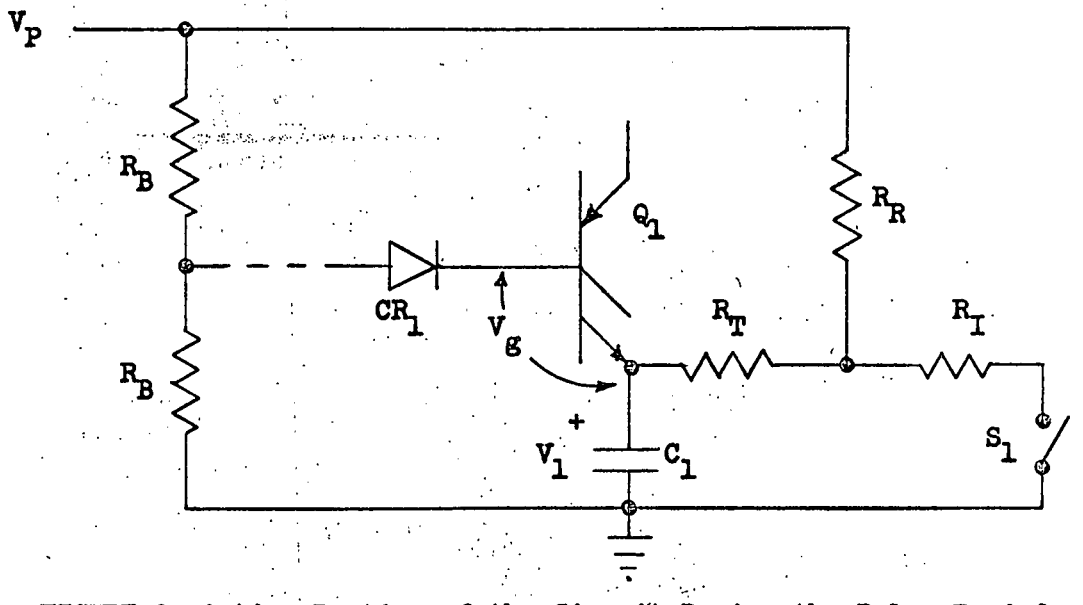

FIGURE 2 Active Portion of the Circuit During the Delay Period

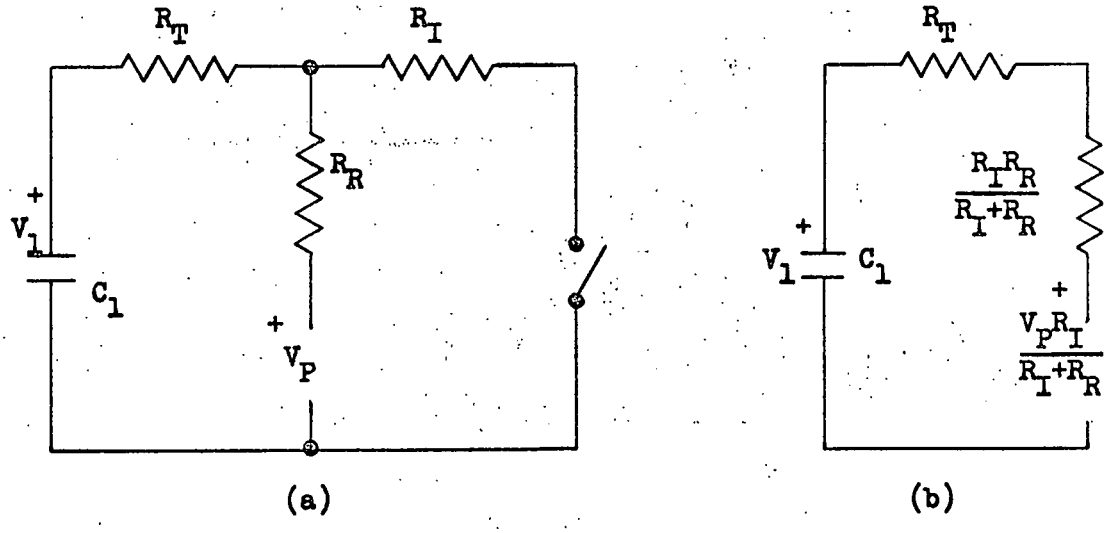

FIGURE 3 (a) Simple RC Circuit

(b) Thevenin's Equivalent Used in Calculations of Delay

$$V_1 = \left(E_1 - \frac{V_P R_I}{R_I+R_R}\right) \exp \frac{-t}{C_1\left[R_T + \frac{R_I R_R}{R_I+R_R}\right]} + \frac{V_P R_I}{R_I+R_R} . \qquad \text{II-1}$$

With C_1 initially charged to V_P, the equation becomes

$$V_1 = V_P \left[\exp \frac{-t}{C_1\left(R_T + \frac{R_I R_R}{R_I+R_R}\right)} + \left(\frac{R_I}{R_I+R_R}\right) \left(1 - \exp \frac{-t}{C_1\left(R_T + \frac{R_I R_R}{R_I+R_R}\right)}\right) \right] \qquad \text{II-2}$$

Figure 4, page 7, shows three sets of curves plotted on the same time base. The first is a plot of equation II-2 with R_I changing and V_1 normalized to V_P. These are calculated with R_T = 4700 ohms, and C_1 = 4.7 μf. The second is a comparison between the experimental and actual delay times versus R_I for a 2N886A SCR. The third set of curves are identical to the second except a TSW61S SCR is used.

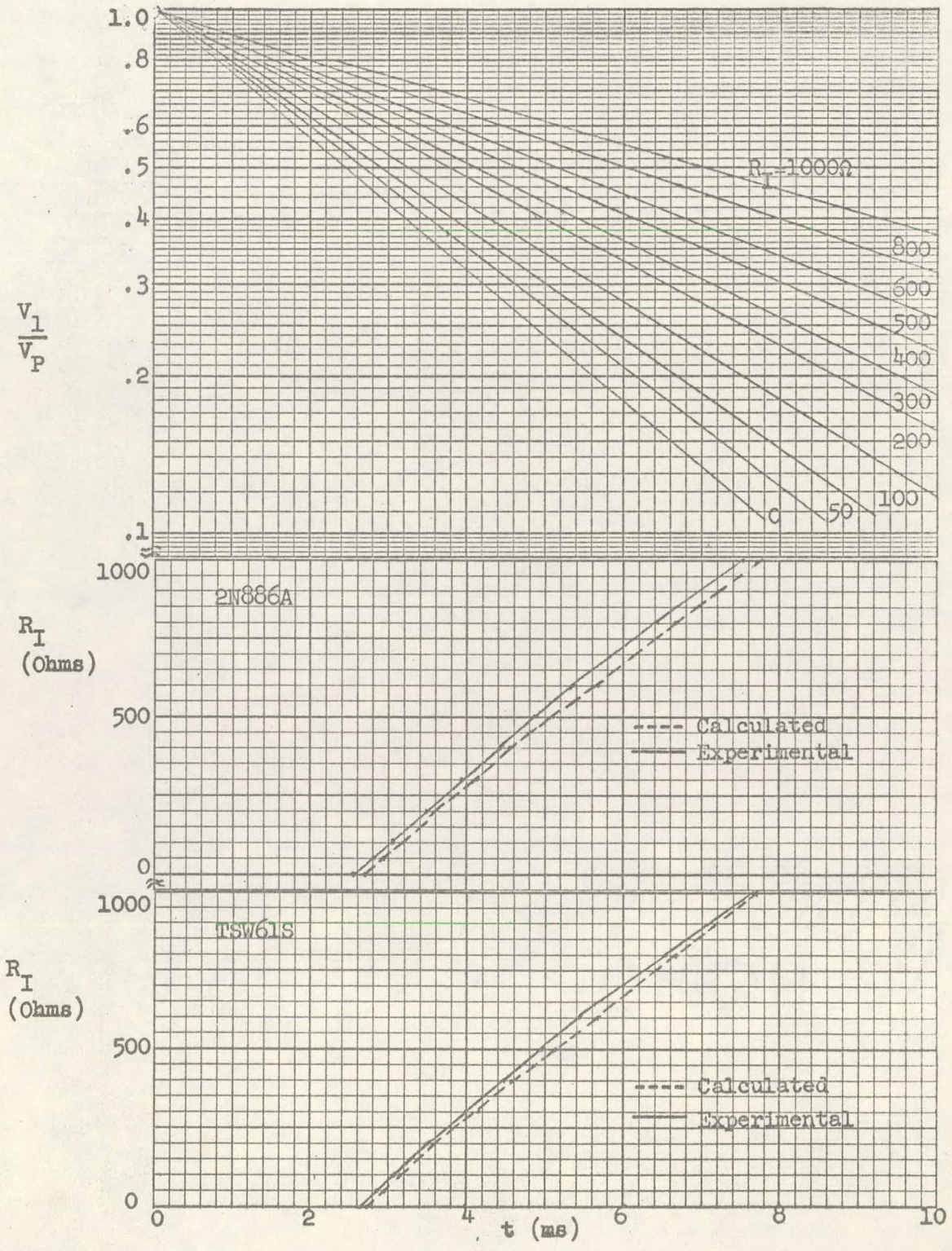

FIGURE 4 A Comparison of Actual to Calculated Delay for Variations of R_I

CHAPTER III

SWITCHING

The switching portion begins as the gate to cathode voltage, V_{GC}, becomes positive and gate current begins to flow. The gate current is amplified in the SCR causing it to conduct heavily, appearing like a very small impedance from gate to cathode and from anode to cathode. The capacitor, C_2, is discharged through the transformer primary, generating a pulse in the load. The switching portion continues with C_1 and C_2 discharging until S_1 is opened.

The active portion of the circuit during this period is shown in Figure 5a, page 9. In Figure 5, the SCR is replaced by a battery-resistor combination from anode to cathode and from gate to cathode. The diode is also replaced with a resistor-battery combination. During the time the transformer is active the voltage across C_1 will not change appreciably if the value of $C_1 >> C_2$. Under these conditions, the DC voltages across $R_B/2$, R_D, R_{GC}, and R_G will not change. The load presented to the transformer, if R_G is much greater than the other three resistances, will be approximately $R_D+R_{GC}+R_B/2 = R_Z$. These approximations were made to simplify the equations necessary to describe the circuit. Further simplifying the circuit by replacing the transformer with a six-terminal black box, whose equations are developed in Appendix C, and the input resistances R_R, R_I, and R_T with their Thevenin's Equivalent as in Chapter II, gives the circuit shown in Figure 5b, page 9. This figure also shows the currents

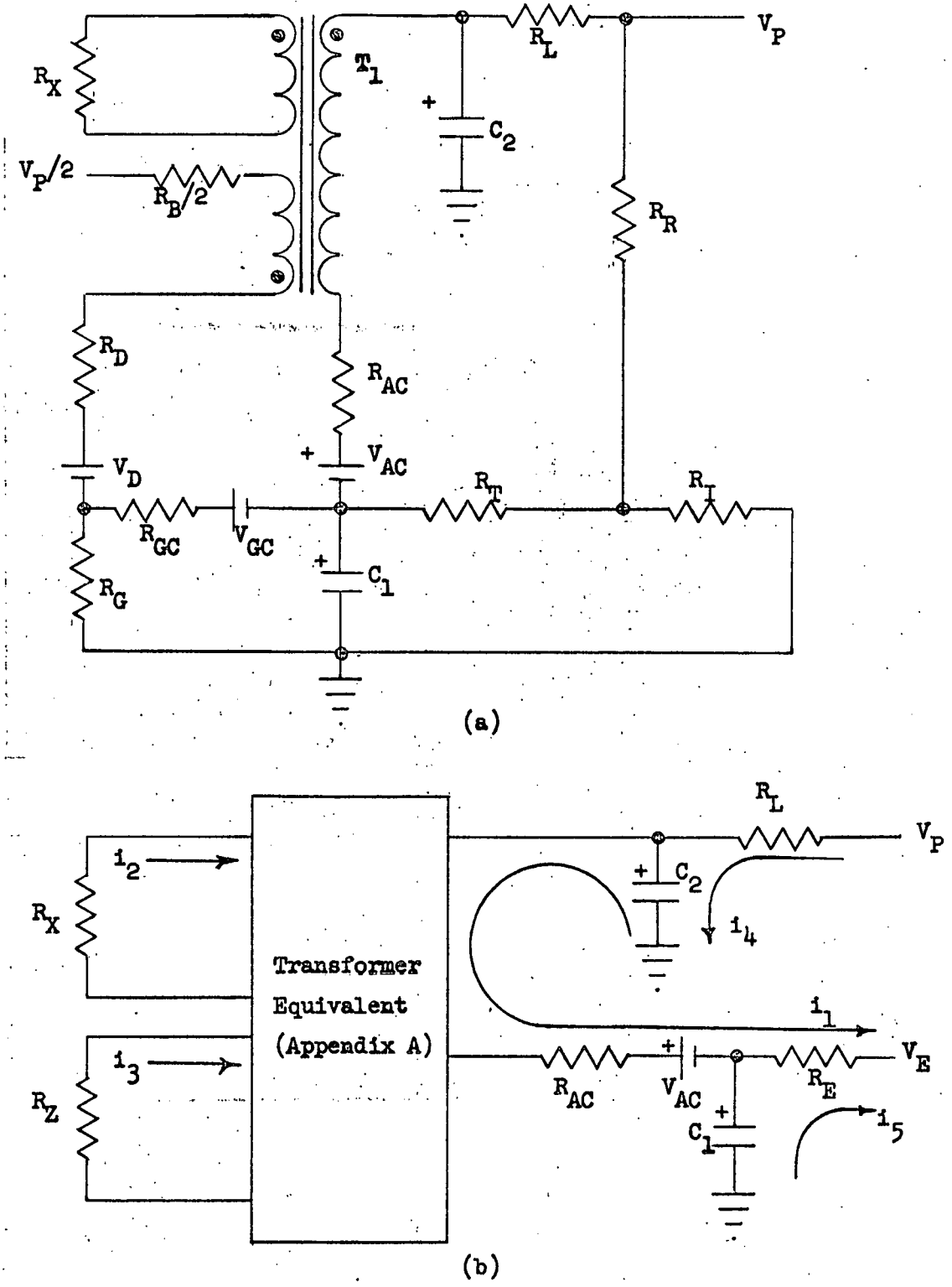

FIGURE 5 (a) Active Portion of the Circuit During Switching

(b) Simplified Circuit Used in Calculations

with their directions which are used in the following calculations.

The actual analysis concerns the voltage pulse amplitude and wave shape across the load, R_X. This is obtained by calculating the current in the primary of the transformer, i_1; from it, calculating the current in the transformer secondary, i_2; and finally multiplying the secondary current times the load to get the output voltage. Initially, the voltage across C_1 is $V_1 = V_P/2-V_D-V_{GC}$ and the voltage across C_2 is $V_2 = V_P$. The primary current can be found by writing the loop equations for i_1, i_4, and i_5. Writing these directly in Laplace form yields:

$$\frac{V_2-V_E-V_{AC}}{2} = I_1\left(\frac{1}{C_2S} + R_{AC}+R_E+A\right) - \frac{I_4}{C_2S} + I_5R_E \qquad \text{III-1}$$

$$\frac{V_P-V_2}{2} = \frac{-I_1}{C_2S} + I_4\left(R_L+\frac{1}{C_2S}\right) \qquad \text{III-2}$$

$$\frac{V_1-V_E}{S} = I_1R_E + I_5\left(\frac{1}{C_1S} + R_E\right) \qquad \text{III-3}$$

where A is the Laplace transform of the transformer input impedance. Substituting as follows:

$$E_A = V_2 - V_E - V_{AC}$$

$$E_B = V_1 - V_E$$

noting that $V_P - V_2 = 0$, and solving for I_1 gives:

$$I_1 = \frac{\begin{vmatrix} \frac{E_A}{S} & -\frac{1}{C_2 S} & R_E \\ 0 & R_L + \frac{1}{C_2 S} & 0 \\ \frac{E_B}{S} & 0 & R_E + \frac{1}{C_1 S} \end{vmatrix}}{\begin{vmatrix} \frac{1}{C_2 S} + R_{AC} + R_E + A & -\frac{1}{C_2 S} & R_E \\ -\frac{1}{C_2 S} & R_L + \frac{1}{C_2 S} & 0 \\ R_E & 0 & R_E + \frac{1}{C_1 S} \end{vmatrix}} \qquad \text{III-4}$$

which is reduced to

$$I_1 = \frac{\left[\frac{(E_A - E_B)R_E}{S} + \frac{E_A}{C_1 S^2}\right]\left[R_L + \frac{1}{C_2 S}\right]}{R_L R_E R_{AC} + \frac{1}{2}\left[\frac{R_L(R_E + R_{AC})}{C_1} + \frac{R_E(R_{AC} + R_L)}{C_2}\right] + \frac{1}{S^2}\left[\frac{R_L + R_E + R_{AC}}{C_1 C_2}\right]}$$

$$+ \frac{A}{S^2}\left[R_L R_E S^2 + \frac{R_E S}{C_2} + \frac{R_L S}{C_1} + \frac{1}{C_1 C_2}\right] \qquad \text{III-5}$$

To find the waveform of i_1, substitutions are made using the circuit values. These are listed below with the value for A from Appendix C and the values of the Thevenin Equivalent. A line resistance, R_1, of 200 ohms is used.

$R_L = 10^5$ ohms $\qquad V_P = 28$ volts

$R_T = 750$ ohms $\qquad V_{AC} = 0.67$ volts

$R_{AC} = 13$ ohms $\qquad V_{CG} = 0.29$ volts

R_E = 940 ohms	V_2 = 28 volts
R_Z = 1710 ohms	V_1 = 13.01 volts
R_X = 1000 ohms	V_E = 1.15 volts
R_B = 3320 ohms	E_A = 26.18 volts
$C_1 = 4.7(10)^{-6}$ farads	E_B = 11.86 volts
$C_2 = 47(10)^{-9}$ farads	$E_A - E_B$ = 14.32 volts

$$A = \frac{s^3 + 5.3233(10)^6\, s^2 + 0.46857(10)^{12}\, s + 0.89896(10)^{15}}{1401.3\left[s^2 + 1.4834(10)^6\, s + 8.0191(10)^9\right]}$$

When the above values are put into equation III-5 and the terms collected, the equation becomes:

$$I_1 = \frac{20.066(10)^3\left[s+413.81\right]\left[s+212.77\right]\left[s+5.3865(10)^3\right]\left[s+1.4887(10)^6\right]}{s\left[s^5+5.3420(10)^6 s^4+527.63(10)^9 s^3+45.938(10)^{15} s^2+252.06(10)^{18} s + 54.675(10)^{21}\right]} \qquad \text{III-6}$$

or written with the roots of the denominator

$$I_1 = \frac{20.066(10)^3\left[s+413.81\right]\left[s+212.77\right]\left[s+5.3865(10)^3\right]\left[s+1.4887(10)^6\right]}{s\left[s+5.2430(10)^6\right]\left[s+5.6170(10)^3\right]\left[s+226.21\right]\left[s^2+93.122(10)^3 s + 8.2072(10)^9\right]} \qquad \text{III-7}$$

Although the value of i_1 can be found, it is not necessary, for i_2 can be found using I_1. The Laplace transform of i_2 is I_2 and is found by multiplying I_1 by the transfer function of the transformer $\frac{I_2}{I_1}$.

$$\frac{I_2}{I_1} = \frac{-107.07s\left[s+2.2375(10)^6\right]}{\left[s+5.1756(10)^3\right]\left[s+771.48(10)^6\right]} \qquad \text{III-8}$$

Multiplying, I_2 becomes

$$I_2 = \frac{(-107.07)\left[20.066(10)^3\right]\left[s+2.2375(10)^6\right]\left[s+413.81\right]\left[s+212.77\right]}{\left[s+5.1756(10)^3\right]\left[s+771.48(10)^6\right]\left[s+5.6170(10)^3\right]\left[s+226.21\right]} \times$$

$$\times \frac{\left[s+5.3865(10)^3\right]\left[s+1.4887(10)^6\right]}{\left[s+5.2430(10)^6\right]\left[s^2+93.12(10)^3 s+8.2072(10)^9\right]} \qquad \text{III-9}$$

Expanding by partial fractions I_2 becomes

$$I_2 = \frac{-1.1726(10)^{-3}}{s+5.2430(10)^6} + \frac{0.61429(10)^{-3}}{s+5.6170(10)^3} + \frac{0.10541(10)^{-6}}{s+226.21} + \frac{0.51015(10)^{-3}}{s+5.1756(10)^3}$$

$$+ \frac{2.7909(10)^{-3}}{s+771.48(10)^6} - \frac{2.7406(10)^{-3}\left[s+46.561(10)^3\right]}{\left[s+46.561(10)^3\right]^2+\left[77.713(10)^3\right]^2}$$

$$- \frac{21.203(10)^{-3}\left[77.713(10)^3\right]}{\left[s+46.561(10)^3\right]^2+\left[77.713(10)^3\right]^2} \qquad \text{III-10}$$

Taking the inverse Laplace transform, i_2 is

$$i_2 = 641.29(10)^{-6}\exp\left[-5.6170(10)^3 t\right] + 105.41(10)^{-9}\exp\left[-226.21t\right]$$

$$+ 510.15(10)^{-6}\exp\left[-5.1756(10)^3 t\right] + 2.7909(10)^{-3}\exp\left[-771.48(10)^6 t\right]$$

$$- \left[2.7406(10)^{-3}\cos 77.713(10)^3 t\right.$$

$$\left. + 22.203(10)^{-3}\sin 77.713(10)^3 t\right]\exp\left[-46.561(10)^3 t\right]$$

$$-1.1726\,(10)^{-3}\exp\left[-5.2430(10)^6 t\right] \qquad \text{III-11}$$

The output voltage is $e_2 = -i_2 R_X$. The calculated waveform for e_2 is

shown in Figure 6, page 15, with the actual circuit waveform. It can easily be seen that initially the two waveforms are not alike. Taking the difference to be an error in the transformer equations due to the simplifying assumptions made, the difference between the experimental and calculated waveforms for a step-function into the transformer can be added to the calculated waveshape of e_2 for the circuit. The difference to be added is shown in Figure 13, page 40, in Appendix C. A new comparison is shown in Figure 7, page 16, with this difference added to the calculated values of e_2.

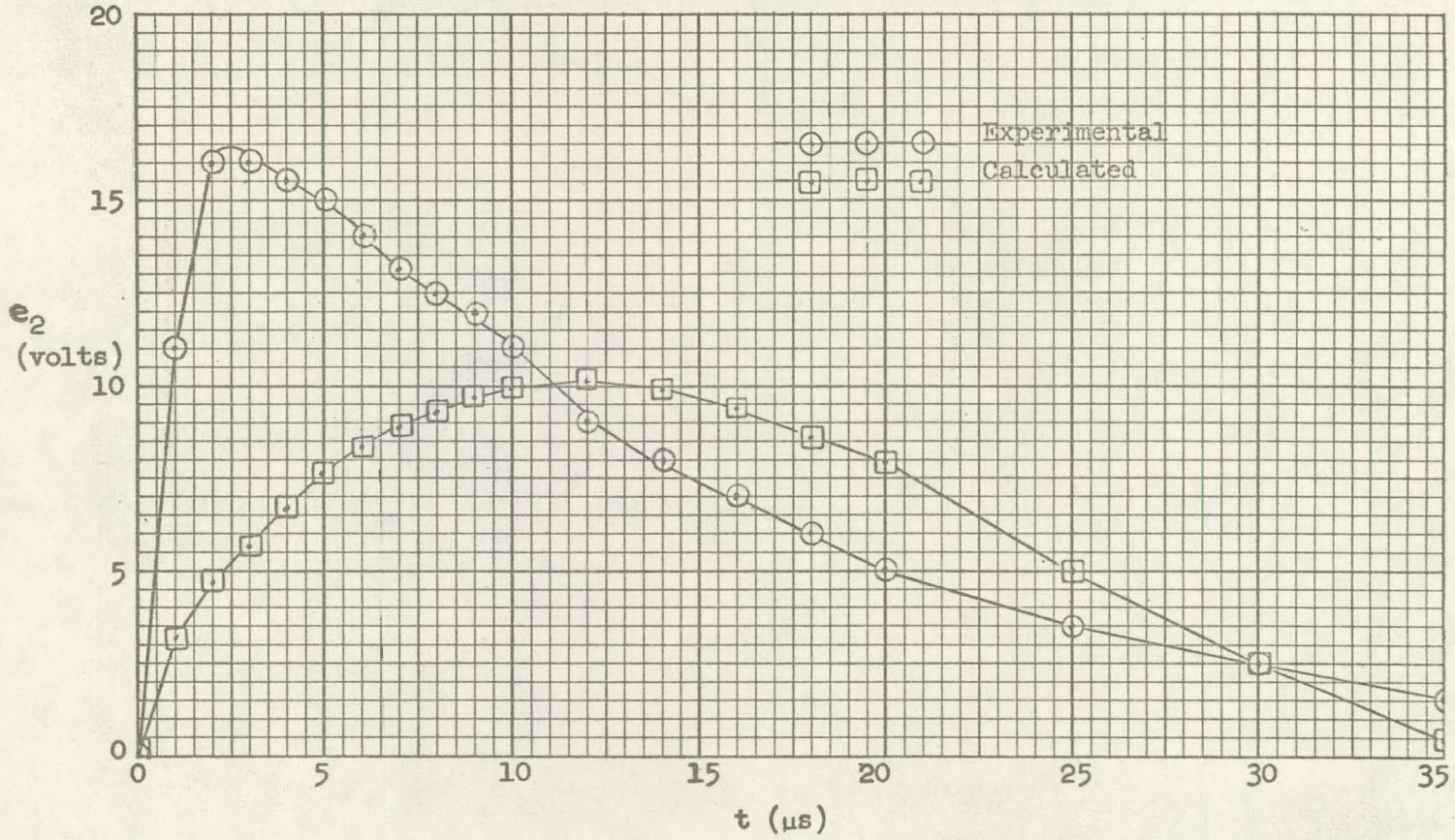

FIGURE 6 A Comparison of Actual to Calculated Output Waveform

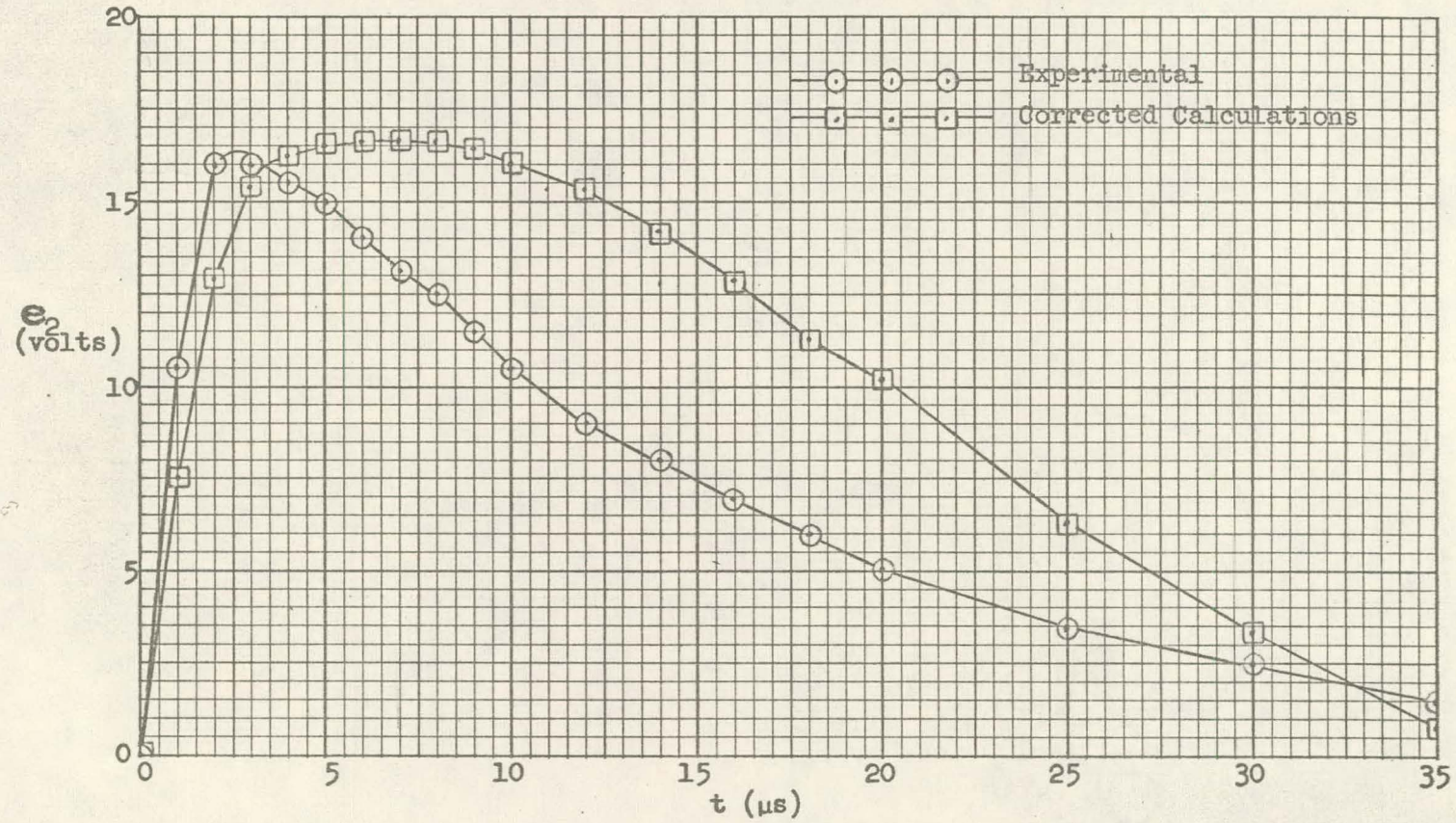

FIGURE 7 A Comparison of Actual to Corrected Calculated Output Waveform

CHAPTER IV

THE RECOVERY PERIOD

The recovery period is defined as the period of time from the opening of S_1 to when it is closed again. For operation of the circuit, enough time must be allowed for the SCR to revert to its blocking state and C_2 to charge to 90% of V_P. Maximum recovery period, then, is the time from the opening of S_1 until the SCR recovers to its blocking state and C_2 recovers to approximately 90% of V_P. The SCR recovers when the anode current drops below a minimum value called the hold current and the gate is not positive with respect to the cathode.

The active part of the circuit is shown in Figure 8, page 19. Here again, the SCR is represented with a battery and resistance for the drop from anode to cathode. The gate current is assumed to have a negligible effect on the circuit operation, except that it sets a minimum voltage to which C_1 can discharge. The resistance in the anode, R_L, is chosen to limit the anode current after C_2 is discharged to less than the hold current required by the SCR. Because of this, the recovery of the SCR is obtained by the charging of C_1 until the gate-cathode voltage is zero. During this time the voltage across C_2 will follow the voltage across C_1. This charging of C_1 is through R_R and R_T with a minimum current being supplied through the SCR. If the voltage across C_1 is initially $V_o = \frac{(V_P/2 - V_{CG} - V_D) R_T}{R_T + R_B/2}$ - no line

resistance - the maximum recovery period will be the time required for C_1 to charge through R_T and R_R from V_o to $V_P/2$ plus the time for C_2 to charge from $V_P/2$ to approximately $.9V_P$. The $.9V_P$ voltage is enough to give an adequate output signal on reclosure of S_1. The time required for C_1 to charge to $V_P/2$ from its V_o is: $t_A = (R_R+R_T)\, C_1 \ln \frac{V_P-V_o}{V_P-V_P/2}$. The time required for C_2 to charge to $0.9V_P$ from $V_P/2$ is:

$t_B = (R_L+R_1)\, C_2 \ln \frac{V_P-V_P/2}{V_P-0.9V_P}$.

The maximum recovery time is: $t_{max} = t_A+t_B$

using

$R_R = 4700$ ohms
$R_T = 750$ ohms
$R_L = (10)^5$ ohms
$R_1 = 80$ ohms
$R_B = 3320$ ohms

$V_P = 28$ volts
$V_{CG} = .39$ volts
$V_D = .60$ volts
$V_o = 4.05$ volts
$C_1 = 4.7\ (10)^{-6}$ farads
$C_2 = 47\ (10)^{-9}$ farads

T_{max} becomes

$$T_{max} = (4700 + 750)(4.7)(10)^{-6} \ln\frac{28-4.05}{28-14.0} + (100{,}000+80)(47)(10)^{-9} \ln\frac{28-14}{28-.9(28)}$$

$$= 25.65(10)^{-3} \ln 1.715 + 4.7(10)^{-3} \ln 5.0 = 21.86 \text{ m sec.}$$

This is the maximum time which must be allowed between closures of S_1 to generate proper output pulses. Experimental data taken using six sample each of two different SCR's give average T_{max} of 20.18 μsec. and 20.26 μsec.

The maximum recovery time required can be shortened by always having some line resistance which will give a divide voltage with R_R.

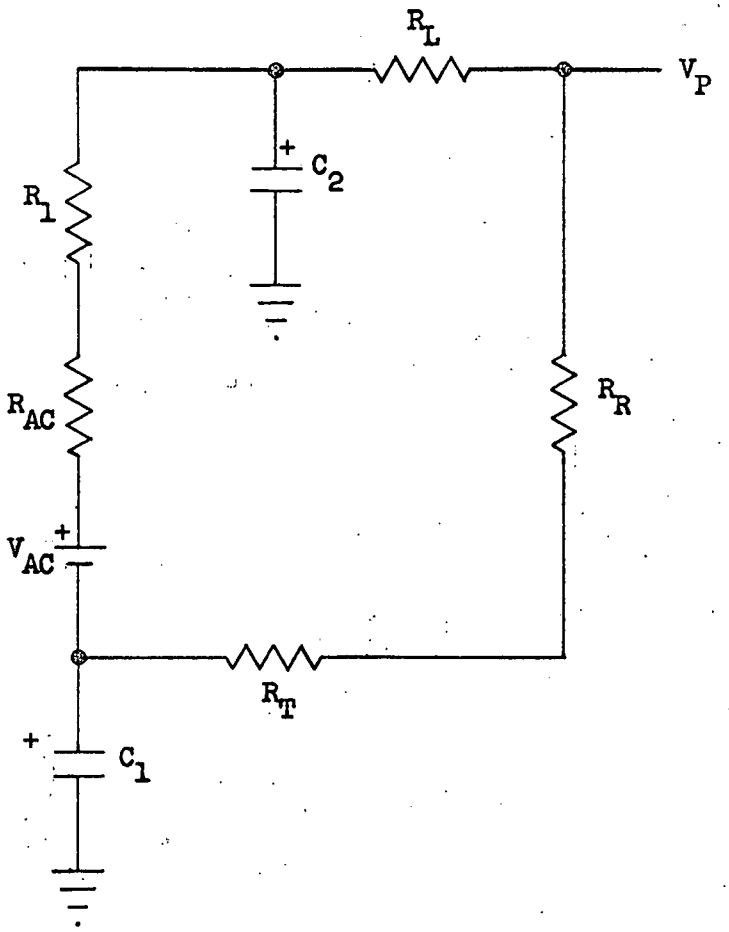

FIGURE 8 Active Portion of the Circuit During Recovery

CHAPTER V

NOISE

Noise on the input lines can be divided into two areas, contact bounce and pick-up. The contact bounce has the effect of lengthening the initial delay time. This requires a slightly longer closure time to cover this additional time. Contact bouncing for three milliseconds or less can be tolerated by the circuit.

Pick-up noise could fire the circuit, but the capacitor, C_1, and the resistor, R_T, form a low frequency filter section. This R-C network requires a voltage of $V_P/2$ across the capacitor for the SCR to trigger. The voltage, V_1, across the capacitor for an input to the buffer of $V_x \sin wt$ is

$$V_1 = V_P - V_x \frac{X_c}{\sqrt{X_c^2+R_R^2}} \sin(wt-\phi) \quad (\phi = \tan^{-1}\frac{X_c}{R_R})$$

This assumes that the input lines have an impedance greater than $20R_R$. Normalizing with respect to V_P and setting $V_1/V_P = 1/2$, the capacitor voltage becomes:

$$.5 = \frac{V_X}{V_P} \frac{X_c}{\sqrt{X_c^2+R_R^2}} \sin(wt-\phi)$$

A plot of the ratio $\frac{V_X}{V_P}$ versus frequency is shown in Figure 9, page 21. The noise input required to trigger the SCR varies from approximately $.5V_P$ at 1 cps to $2.1V_P$ at 1000 cps.

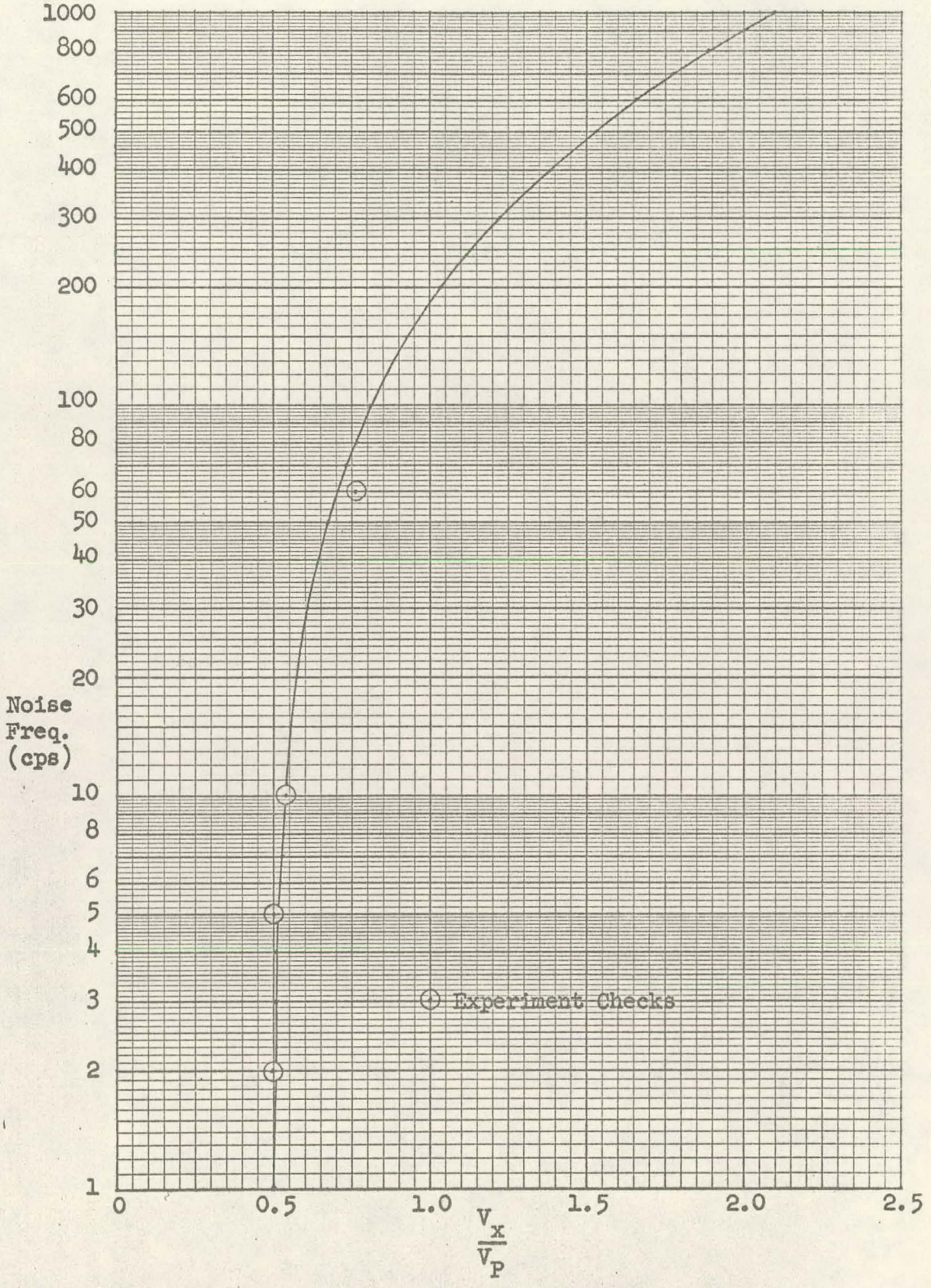

FIGURE 9 Sinusoidal Noise Input Required to Trigger Buffer

CHAPTER VI

CONCLUSIONS

General. The purpose of this thesis was to make an analysis of an Input Buffer of unusual design. This was done to show a method of calculation which would be usable for worse-case analysis or for modifications of the circuit for new applications. For this reason, the calculations were kept simple to allow fairly swift recalculation without requiring the use of a computer. These simplifications show up principally in the switching calculations and produce a minimum circuit output. For example, the uncorrected, calculated output waveform, shown in Figure 6, page 15, does not have as great a peak amplitude nor as fast a rise time as the actual output. Corrections could be made to the analysis, especially in the transformer equivalent, that would give a more accurate comparison with experimental data. These would complicate the equations and impair the practical advantage of the analysis. With this in mind, the comparison between calculated and experimental data will be discussed for each of the principal chapters.

Delay. The calculated and experimental data averages agree very well, although the calculated delay is always greater. This could be due to a difference in the gate to cathode voltage or a variation in the actual value of C_1, the 4.7μf capacitor.

Recovery. The experimental data agreed very well with the calculated maximum. The experimental data is listed in Table IV, page 44.

Noise. The curve shown in Figure 9, page 21, was checked at only four places due to the lack of low impedance, high voltage signal generators. The four checks indicated a very good agreement between the calculated and experimental data.

Switching. These calculations are not in very good agreement with the experimental data. Figure 6, page 15, shows the output waveform the equations give. The total volt-millisec area of the curve is very close to that of the experimental curve, but the peak amplitude is less and the rise-time is not as fast. The calculated output wave could be corrected using the error in the transformer equations from Appendix C. This is shown in Figure 7, page 16, and gives the proper rise-time and good agreement on amplitude, but the pulse width is greater than the actual output.

A subsequent digital circuit designed to trigger on the calculated output shown in Figure 6, page 15, would have no trouble in triggering using the actual waveform.

Summary. From the tables and figures, typical operation can be described. This Input Buffer is capable of being triggered thirty times per second with long lines having a maximum resistance of 1000 ohms. The minimum closure time required under these conditions would be 8 msec. The output which could be expected would have a peak voltage of at least 10 volts and half-amplitude width of approximately 20 μsec. The rise-time of the output would be approximately 0.75 μsec.

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BIBLIOGRAPHY

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APPENDIX

APPENDIX A

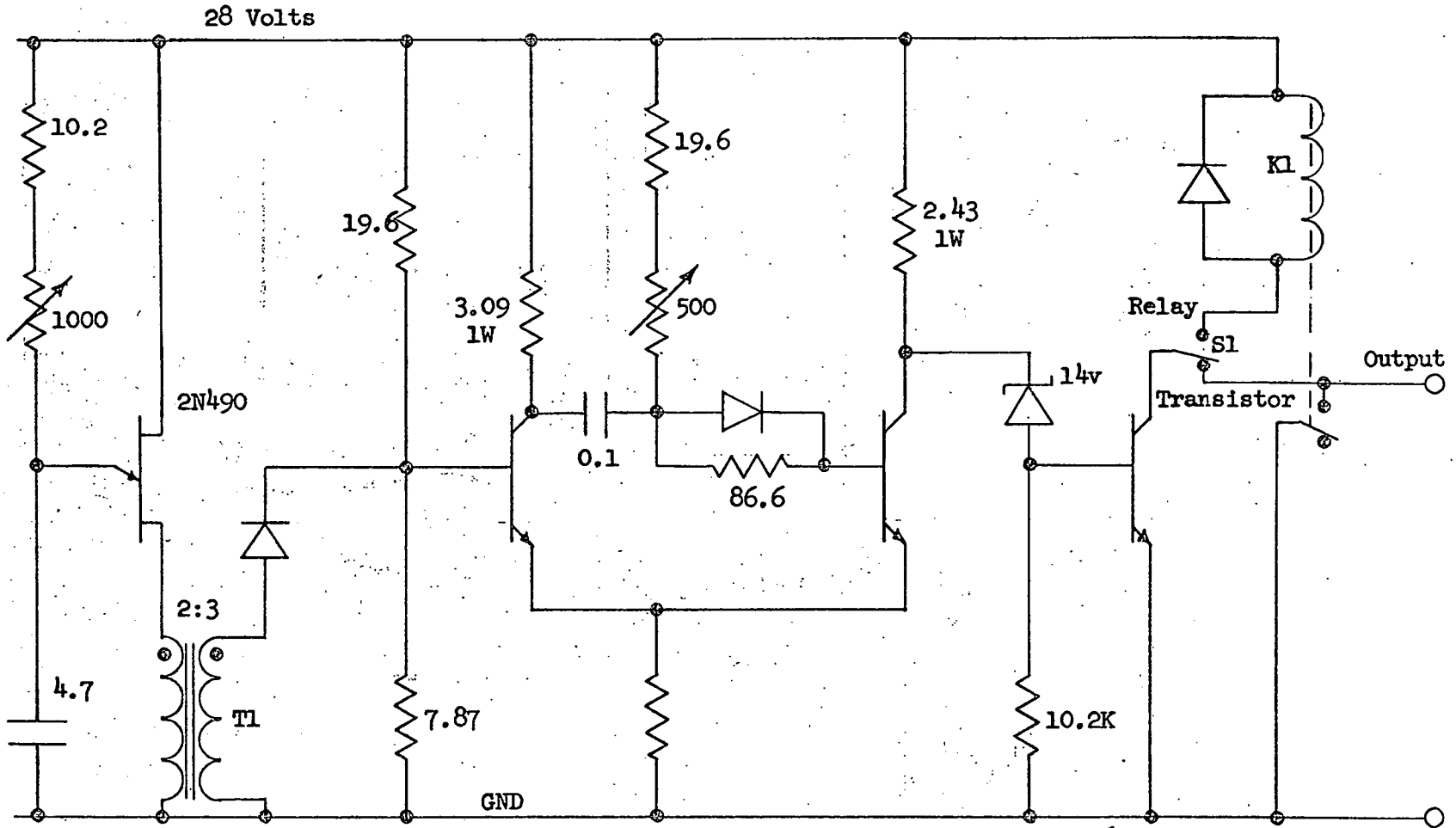
Description of Test Equipment

General. The Input Buffer requires a power supply and a Driver for operation. To monitor the circuit operation, a digital voltmeter, an electronic counter, and an oscilloscope were used. The Driver was built for this thesis to the schematic shown in Figure 10, page 28. The rest are commercial test equipment as listed below:

Power Supply	Power Design Inc. Model 4005
Electronic Counter	Hewlett-Packard Model 5233L
Digital Voltmeter	Hewlett-Packard Model 3440A
Oscilloscope	Tektronix Type 513
	Tektronix Plug-In Type CA.

The input resistance was varied using a General Radio Type 1432-K Decade Resistance Box.

Noise. During the tests to determine the susceptibility of the circuit to noise, the Driver was disconnected and a signal generator was connected to the input of the Buffer through a 30 microfarad capacitor. The signal generator used was a Hewlett-Packard Test Oscillator Model 650A.



Unless otherwise noted, all resistors are in $(10)^3$ ohms, capacitors in $(10)^{-6}$ farads, diodes are FD200, and transistors are 2N1613.

FIGURE 10 Driver Schematic

APPENDIX B

Calculation and Experimental Data for the Delay

Calculations. The equation I-2 can be written in the form

$$V_1 = V_P \left[\exp \frac{-t}{A} + R_E \left(1 - \exp \frac{-t}{A}\right) \right]$$

where $R_E = \frac{R_I}{R_I + R_R}$ and $A = C_1 \left(R_T + \frac{R_R R_I}{R_R + R_I}\right)$

Normalizing, the equation becomes

$$\frac{V_1}{V_P} = \left[\exp \frac{-t}{A} + R_E \left(1 - \exp \frac{-t}{A}\right) \right]$$

Solving for the normalized voltage at the times $t = \frac{A}{2}$ and $t = A$ for varying values of R_I gives the data to plot the Delay. These values are shown in Table I, page 30.

The experimental data was taken on two types of SCR's using six samples each. One type is a Transitron TSW61S; the other is a Solid State Products Inc. 2N886A. The measured delay for various R_I using the twelve SCR's is shown with their averages in Table II, page 31.

TABLE I

CALCULATED POINTS USED TO PLOT DELAY CURVES

R_I (ohms)	A (milliseconds)	V_1/V_P at $t = \frac{A}{2}$	V_1/V_P at $t = A$
0	3.53	0.607	0.368
50	3.76	0.611	0.374
100	3.99	0.615	0.381
200	4.43	0.623	0.394
300	4.85	0.630	0.406
400	5.26	0.637	0.417
500	5.65	0.644	0.429
600	6.03	0.651	0.439
800	6.74	0.663	0.460
1000	7.40	0.676	0.479

TABLE II

MEASURED DELAYS AND AVERAGES FOR VARIOUS R_I

	R_I (ohms)	Sample No. 1	2	3	4	5	6	Average
2N886A	0	2.56	2.59	2.57	2.54	2.58	2.64	2.58
	50	2.80	2.83	2.79	2.80	2.80	2.87	2.82
	100	3.01	3.05	3.01	3.02	3.02	3.09	3.03
	200	3.46	3.52	3.45	3.47	3.46	3.55	3.48
	300	3.91	3.97	3.90	3.92	3.92	4.02	3.94
	400	4.37	4.44	4.37	4.39	4.38	4.50	4.41
	500	4.86	4.92	4.85	4.87	4.87	4.99	4.89
	600	5.35	5.42	5.35	5.37	5.36	5.50	5.39
	800	6.38	6.44	6.37	6.42	6.40	6.58	6.43
	1000	7.49	7.56	7.47	7.52	7.50	7.74	7.53
TSW61S	0	2.69	2.57	2.68	2.60	2.57	2.71	2.64
	50	2.93	2.79	2.90	2.82	2.78	2.93	2.86
	100	3.16	3.01	3.13	3.04	3.00	3.16	3.08
	200	3.61	3.45	3.60	3.49	3.44	3.63	3.52
	300	4.09	3.90	4.07	3.95	3.90	4.10	4.00
	400	4.57	4.37	4.56	4.43	4.37	4.59	4.47
	500	5.07	4.85	5.06	4.91	4.84	5.09	4.97
	600	5.59	5.35	5.56	5.42	5.34	5.60	5.45
	800	6.68	6.37	6.64	6.48	6.38	6.70	6.54
	1000	7.81	7.47	7.78	7.60	7.48	7.85	7.67

All delay measurements are in milliseconds.

APPENDIX C

Development Of The Transformer Equations

The following equations for a three winding transformer were developed using the same method used on two winding transformers.[1] The schematic diagram for a three winding transformer is shown in Figure 11, page 33.

The primary inductance is L_1; the secondary L_2; and the ternary L_3. There are three mutual inductances - M_{12} between primary and secondary windings; M_{23} between secondary and ternary windings; and M_{13} between primary and ternary windings. The resistances of the winding are R_1, R_2, R_3 for the primary, secondary and ternary windings. To keep the calculations simple, the capacitance between windings will be ignored. Also, the core loss and nonlinearity of the magnetic circuit will be neglected. The transformer has the relative polarity of the windings marked with dots. Increasing current into a dotted terminal in one winding will produce an induced voltage in the other windings, with the dotted terminal positive with respect to the undotted. Considering the voltages and currents as defined, the voltage equations around the three loops are:

---

[1] Walter C. Johnson, Transmission Lines and Networks, (New York: McGraw-Hill Book Company, Inc., 1950) pp. 262-66; Drs. Jacob Millman and Herbert Taub, Pulse and Digital Circuits, (New York: McGraw-Hill Book Company, Inc., 1956) pp. 253-56.

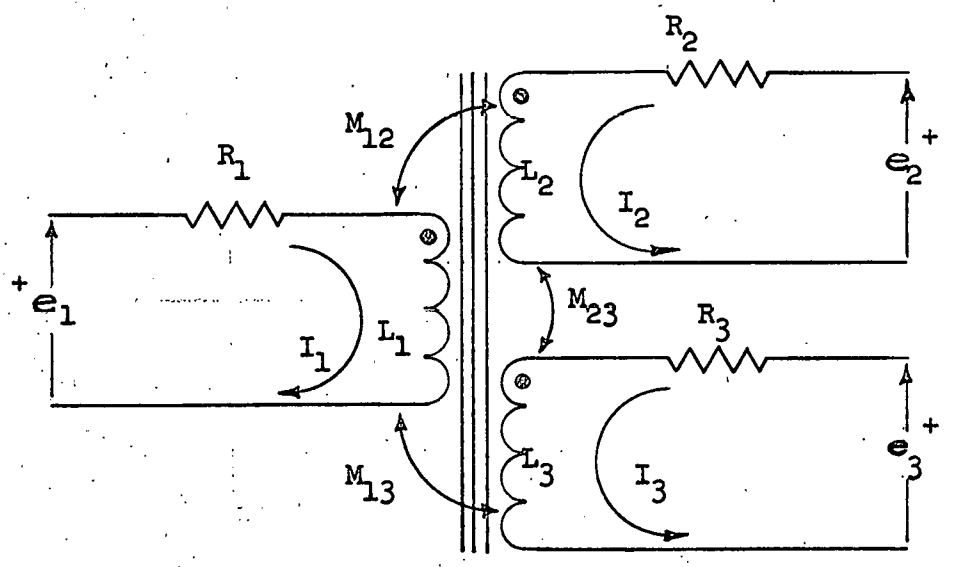


FIGURE 11 Schematic Circuit of the Transformer

$$e_1 = i_1R_1 + L_1\frac{di_1}{dt} + M_{12}\frac{di_2}{dt} + M_{13}\frac{di_3}{dt}$$

$$e_2 = M_{12}\frac{di_1}{dt} + R_2i_2 + L_2\frac{di_2}{dt} + M_{23}\frac{di_3}{dt}$$

$$e_3 = M_{13}\frac{di_1}{dt} + M_{23}\frac{di_2}{dt} + R_3i_3 + L_3\frac{di_3}{dt}$$

Multiplying and dividing the current term i_2 in the equations by an arbitrary constant, a, and the current term i_3 by another arbitrary constant, b, the following equations are obtained:

$$e_1 = i_1R_1 + L_1\frac{di_1}{dt} + aM_{12}\frac{d}{dt}\left(\frac{i_2}{a}\right) + bM_{13}\frac{d}{dt}\left(\frac{i_3}{b}\right)$$

$$ae_2 = aM_{12}\frac{di_1}{dt} + a^2R_2\left(\frac{i_2}{a}\right) + a^2L_2\frac{d}{dt}\left(\frac{i_2}{a}\right) + abM_{23}\frac{d}{dt}\left(\frac{i_3}{b}\right)$$

$$be_3 = bM_{13}\frac{di_1}{dt} + abM_{23}\frac{d}{dt}\left(\frac{i_2}{a}\right) + b^2R_3\left(\frac{i_3}{b}\right) + b^2L_3\frac{d}{dt}\left(\frac{i_3}{b}\right)$$

Letting $e_2 = -i_2R_x$ then $ae_2 = -a^2R_x\left(\frac{i_2}{a}\right)$

also $e_3 = -i_3R_z$ then $be_3 = -b^2R_z\left(\frac{i_3}{b}\right)$, then the above equations become;

$$e_1 = i_1R_1 + L_1\frac{di_1}{dt} + aM_{12}\frac{d}{dt}\left(\frac{i_2}{a}\right) + bM_{13}\frac{d}{dt}\left(\frac{i_3}{b}\right)$$

$$0 = aM_{12}\frac{di_1}{dt} + a^2(R_2 + R_x)\frac{i_2}{a} + a^2L_2\frac{d}{dt}\left(\frac{i_2}{a}\right) + abM_{23}\frac{d}{dt}\left(\frac{i_3}{b}\right)$$

$$0 = bM_{13}\frac{di_1}{dt} + abM_{23}\frac{d}{dt}\left(\frac{i_2}{a}\right) + b^2(R_3 + R_z)\frac{i_3}{b} + b^2L_3\frac{d}{dt}\left(\frac{i_3}{b}\right)$$

In Laplace $\mathcal{L}(e_1) = I_1(R_1 + L_1S) + aM_{12}\left(\frac{I_2}{a}\right)S + bM_{13}\left(\frac{I_3}{b}\right)S$

$$0 = aM_{12}SI_1 + (a^2E_2 + a^2R_x + a^2L_2S)\left(\frac{I_2}{a}\right) + abM_{23}\left(\frac{I_3}{b}\right)S$$

$$0 = bM_{13}SI_1 + abM_{23}\left(\frac{I_2}{a}\right)S + (b^2R_3 + b^2R_z + b^2L_3S)\frac{I_3}{b}$$

$$I_1 = \frac{\begin{vmatrix} \mathcal{L}(e_1) & aM_{12}S & bM_{13}S \\ 0 & a^2R_2+a^2R_x+a^2L_2S & abSM_{23} \\ 0 & abM_{23}S & b^2R_3+b^2R_z+b^2L_3S \end{vmatrix}}{\Delta}$$

$$\frac{I_2}{a} = \frac{\begin{vmatrix} R_1+L_1S & \mathcal{L}(e_1) & bM_{13}S \\ aM_{12}S & 0 & abM_{23}S \\ bM_{13}S & 0 & b^2R_3+b^2R_z+b^2L_3S \end{vmatrix}}{\Delta}$$

$$\frac{I_3}{b} = \frac{\begin{vmatrix} R_1+L_1S & aM_{12}S & \mathcal{L}(e_1) \\ aM_{12}S & a^2R_2+a^2R_x+a^2L_2S & 0 \\ bM_{13}S & abM_{23}S & 0 \end{vmatrix}}{\Delta}$$

where $\Delta =$

$$\begin{vmatrix} R_1+L_1S & aM_{12}S & bM_{13}S \\ aM_{12}S & a^2R_2+a^2R_x+a^2L_2S & abM_{23}S \\ bM_{13}S & abM_{23}S & b^2R_3+b^2R_z+b^2L_3S \end{vmatrix}$$

Removing $\mathcal{L}(e_1)$ from the matrix, the currents can be written as follows

$$I_1 = \mathcal{L}(e_1) \frac{\begin{vmatrix} a^2R_2+a^2R_x+a^2L_2S & abSM_{23} \\ abM_{23}S & b^2R_3+b^2R_z+b^2L_3S \end{vmatrix}}{\Delta}$$

$$\frac{I_2}{a} = -\mathcal{L}(e_1) \frac{\begin{vmatrix} aM_{12}S & abM_{23}S \\ bM_{13}S & b^2(R_3+R_z+L_3S) \end{vmatrix}}{\Delta}$$

$$\frac{I_3}{b} = \mathcal{L}(e_1) \qquad \frac{\begin{vmatrix} aM_{12}S & a^2(R_2+R_x+L_2S) \\ bM_{13}S & abM_{23}S \end{vmatrix}}{\Delta}$$

Before solving the matrix equations, the following values will be substituted for the resistance, inductance, and mutual inductance of the transformer as described in Appendix G, page 47.

$L_1 = 26.9$ mh	$M_{12} = 73.5$ mh	$R_1 = 80$ ohms
$L_2 = 218$mh	$M_{13} = 26.5$ mh	$R_2 = 225$ ohms
$L_3 = 27.3$ mh	$M_{23} = 73.5$ mh	$R_3 = 80$ ohms

The values used for a and b will be the turns ratios, $a = \frac{N_1}{N_2} = 1/3$; $b = \frac{N_1}{N_3} = 1$. A value of 1000 ohms for R_x and 1710 ohms for R_z will be used. The input to the transformer will be carried as $\mathcal{L}(e_1)$. Making these substitutions, the determinate for Δ becomes:

$$\Delta = \begin{vmatrix} 80+26.9(10)^{-3}S & 24.5(10)^{-3}S & 26.5(10)^{-3}S \\ 24.5(10)^{-3}S & 136.1+23.1(10)^{-3}S & 24.5(10)^{-3}S \\ 26.5(10)^{-3}S & 24.5(10)^{-3}S & 1790+27.3(10)^{-3}S \end{vmatrix}$$

Expanding Δ becomes:

$$\Delta = 80+26.9(10)^{-3}S\left[(136.1+23.1(10)^{-3}S)(1790+27.3(10)^{-3}S)-(24.5(10)^{-3})^2S^2\right]$$
$$-24.5(10)^{-3}S\left[24.5(10)^{-3}S(1790+27.3(10)^{-3}S)-(24.5)(26.5)(10)^{-6}S^2\right]$$
$$+26.5(10)^{-3}S\left[(24.5)^2(10)^{-6}S^2-26.5(10)^{-3}S(136.1+23.1(10)^{3}S)\right]$$

or

$$\Delta = 19.490(10)^6+10.159(10)^3S+0.115415S^2+21.680(10)^{-9}S^3$$

Using this value and repeating the process I_1 becomes:

$$I_1 = \mathcal{L}(e_1) \qquad \frac{\begin{vmatrix} 136.1+23.1(10)^{-3}s & 24.5(10)^{-3}s \\ 24.5(10)^{-3}s & 1790+27.3(10)^{-3}s \end{vmatrix}}{\Delta}$$

$$I_1 = \frac{\mathcal{L}(e_1)\left[\left\{136.1+(23.1)(10)^{-3}s\right\}\left\{1790+24.3(10)^{-3}s\right\} - (24.5)^2(10)^{-6}s^2\right]}{\Delta}$$

$$I_1 = \mathcal{L}(e_1)\,\frac{243.62(10)^3+45.065(s)+30.38(10)^{-6}s^2}{19.490(10)^6+10.159(10)^3s+0.11541s^2+21.680(10)^{-9}s^3}$$

Dividing to give unit values for s^2 in the numerator and s^3 in the denominator, I_1 becomes:

$$I_1 = 1.4013(10)^3\ \mathcal{L}(e_1)\,\frac{s^2+1.4834(10)^6s+8.0191(10)^9}{s^3+5.3233(10)^6s^2+.46857(10)^{12}s+.89896(10)^{15}}$$

The input current can be written as $I_1 = \mathcal{L}(e_1)/A$ with A as the primary impedance or

$$A = \frac{s^3+5.3233(10)^6s^2+0.46857(10)^{12}s+0.89896(10)^{15}}{1401.3\left[s^2+1.4834(10)^6s+8.0191(10)^9\right]}$$

Factoring the numerator and denominator of I_1

$$I_1 = \frac{1401.3\,\mathcal{L}(e_1)\left[s+5386.5\right]\left[s+1.4887(10)^6\right]}{\left[s+1962.3\right]\left[s+5.2334(10)^6\right]\left[s+87539\right]}$$

The output current into the load R_x is the waveform desired. This can be found by multiplying the primary current (I_1) by the transfer function $(\frac{I_2}{I_1})$. This function is determined as follows:

$$\frac{\frac{I_2}{a}}{I_1} = \frac{-\mathcal{L}(e_1)\begin{vmatrix} aM_{12}s & abM_{23}s \\ bM_{13}s & b^2(R_3+R_z+L_3s \end{vmatrix}/\Delta}{\mathcal{L}(e_1)\begin{vmatrix} a^2(R_2+R_x+L_2s) & abM_{23}s \\ abM_{23}s & b^2(R_3+R_z+L_3s) \end{vmatrix}/\Delta}$$

Multiplying by a, and dividing like terms

$$\frac{I_2}{I_1} = \frac{\begin{vmatrix} aM_{12}S & abM_{23}S \\ bM_{13}S & b^2(R_3+R_z+L_3S) \end{vmatrix}}{\begin{vmatrix} a^2(R_2+R_x+L_2S) & abM_{23}S \\ abM_{23}S & b^2(R_3+R_z+L_3S) \end{vmatrix}}$$

Expanding, collecting terms and dividing like terms

$$\frac{I_2}{I_1} = \frac{S^2(M_{12}L_3-M_{13}M_{23})+M_{12}(R_3+R_z)S}{S^2(L_2L_3-M_{23}^2)+S\left[(R_2+R_x)L_3+(R_3+R_z)L_2\right]+(R_2+R_x)(R_3+R_z)}$$

Substituting the values for the constants, multiplying, and collecting terms

$$\frac{I_2}{I_1} = \frac{-\left[58.80(10)^{-6}S+131.57\right]S}{0.54915(10)^{-6}S^2+423.66S+2.1928(10)^6}$$

The final form of the transfer function is found by factoring the denominator and dividing for unity values of S.

$$\frac{I_2}{I_1} = \frac{-107.08\left[S+2.2375(10)^6\right]S}{(S+5175.6)\left[S+771.48(10)^6\right]}$$

Using this I_2 becomes

$$I_2 = \frac{I_2}{I_1}\ I_1$$

$$= \frac{-107.08\left[S+2.2375(10)^6\right]S(1401.3)\mathcal{L}(e_1)(S+5386.5)\left[S+1.4887(10)^6\right]}{(S+5175.6)\left[S+771.48(10)^6\right](S+1962.3)\left[S+5.2334(10)^6\right](S+87539)}$$

$$= \frac{-0.15004(10)^6\mathcal{L}(e_1)\left[S+2.2375(10)^6\right](S+5386.5)\left[S+1.4887(10)^6\right]S}{(S+5175.6)\left[S+771.48(10)^6\right](S+1962.3)\left[S+5.2334(10)^6\right](S+87539)}$$

Let e_1 by a 10 volt step, then $\mathcal{L}(e_1) = \frac{10}{S}$. Making the partial fraction expansion, I_2 becomes:

$$I_2 = \frac{1.9512(10)^{-3}}{S+771.48(10)^6} - \frac{0.81683(10)^{-3}}{S+5.2334(10)^6} + \frac{13.286(10)^{-3}}{S+87539} + \frac{0.98252(10)^{-3}}{S+5175.6}$$

$$- \frac{15.402(10)^{-3}}{S+1962.3}$$

Taking the Inverse Laplace, i_2 is as follows:

$$i_2 = 1.9512(10)^{-3}\exp\left[-771.48(10)^6 t\right] - 0.81683(10)^{-3}\exp\left[-5.2334(10)^6 t\right]$$
$$+13.286(10)^{-3}\exp(-87539t) + 0.98252(10)^{-3}\exp(-5175.6t)$$
$$-15.402(10)^{-3}\exp(-1962.3t)$$

The output voltage is $c_2 = i_2 R_x$.

Figure 12, page 40, is a comparison of experimental and calculated waveforms of e_2. The difference in the two waveforms is shown in Figure 13, page 41, and represents the error in the Transformer calculations. This error is primarily due to ignoring the winding capacitance in the calculations. The points used to plot these two figures are tabulated in Table III, page 42.

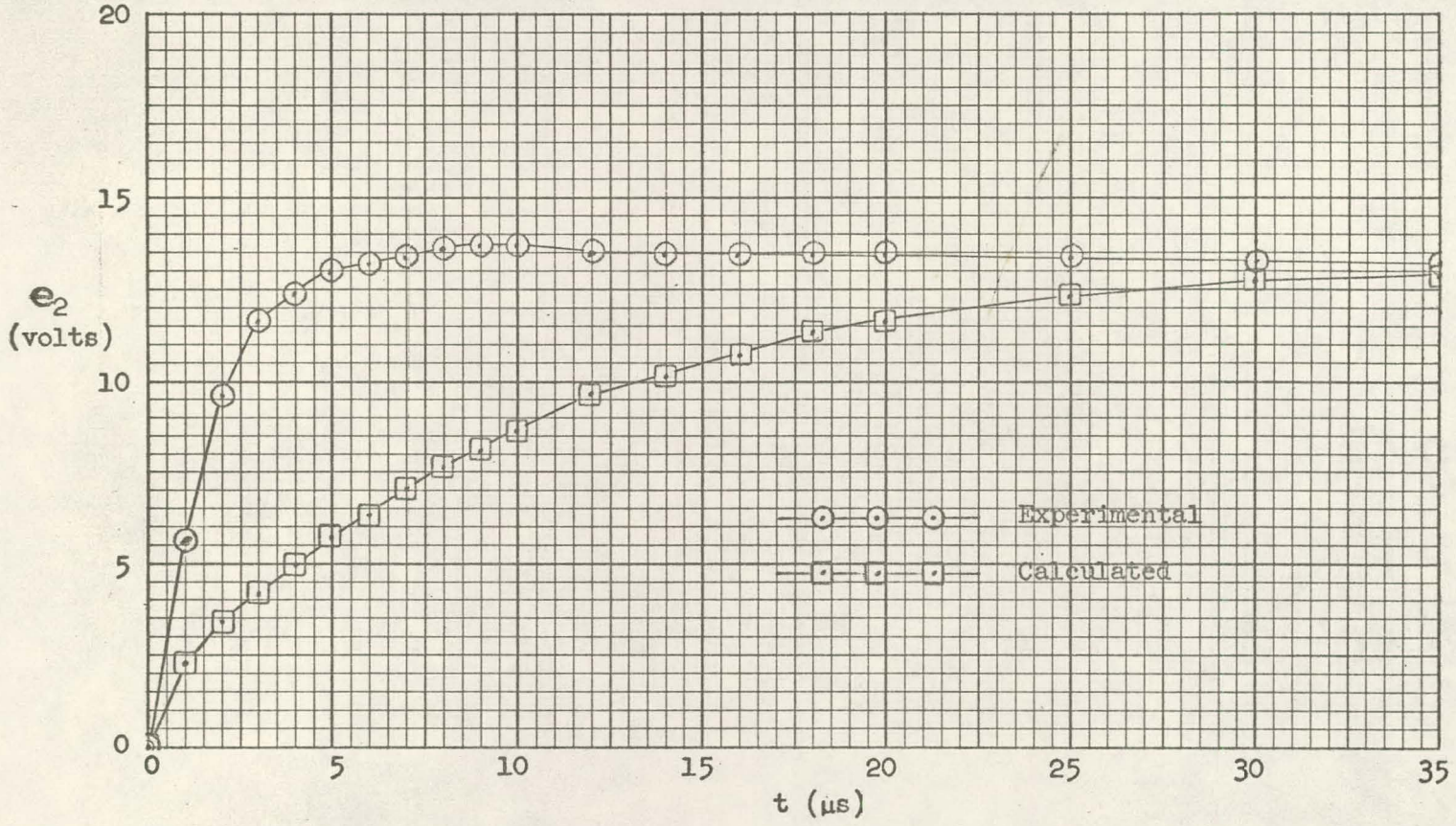


FIGURE 12 Comparison of Actual to Calculated Transformer Output Waveforms

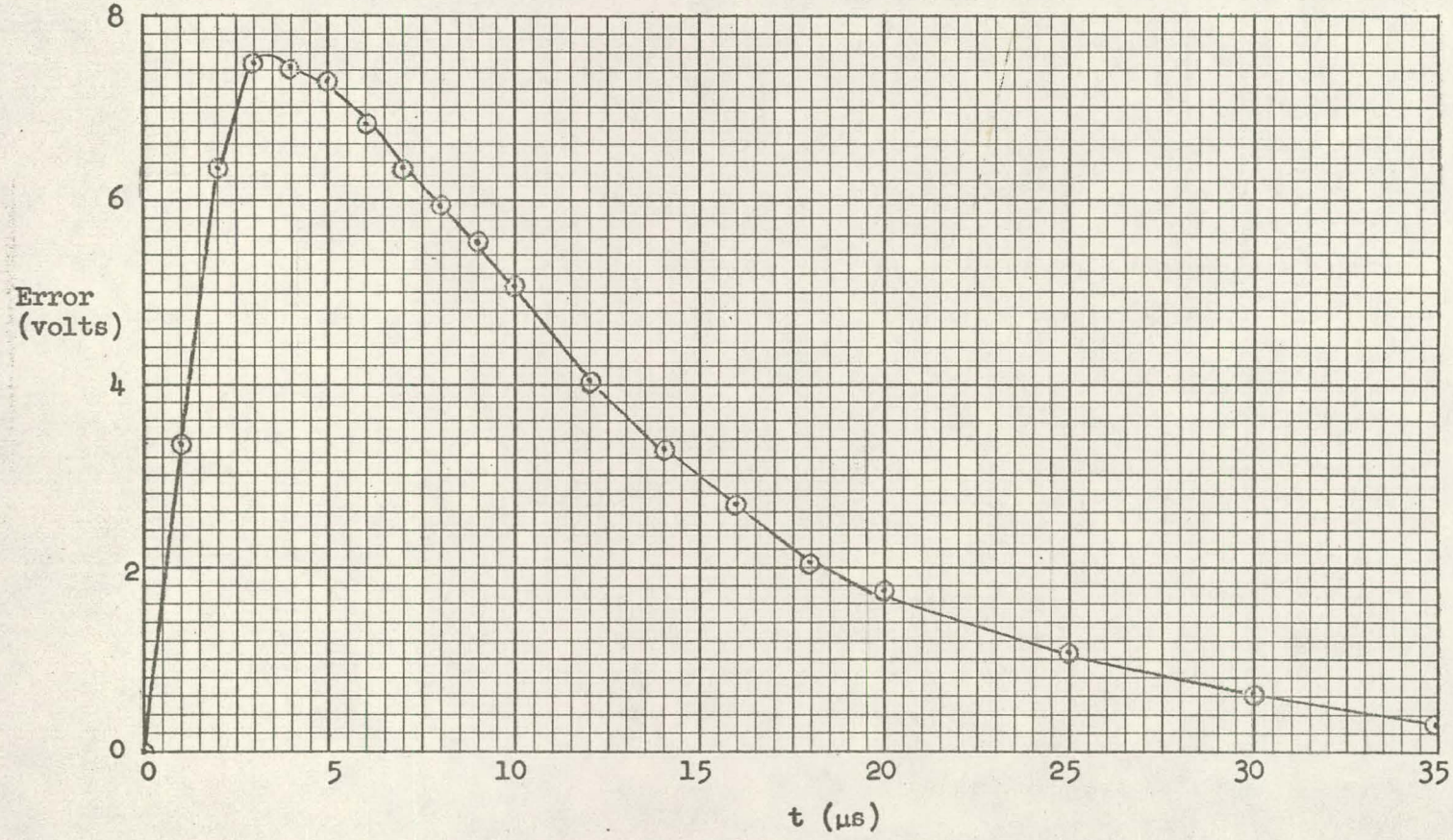


FIGURE 13 Transformer Error between Actual and Calculated Output Waveforms

TABLE III

Data for Comparison of Calculated and Measured Transformer Output Voltage and Error

Time (μs)	e_2 Calculate	e_2 Measured	Error
0	0.001	0.00	0.00
1	2.242	5.60	3.36
2	3.40	9.60	6.37
3	4.141	11.60	7.46
4	4.981	12.40	7.42
5	5.723	13.00	7.28
6	6.384	13.20	6.82
7	7.041	13.40	6.36
8	7.630	13.60	5.97
9	8.149	13.70	5.55
10	8.642	13.70	5.06
12	9.470	13.50	4.03
14	10.139	13.45	3.31
16	10.740	13.43	2.69
18	11.390	13.42	2.03
20	11.616	13.40	1.78
25	12.308	13.35	1.04
30	12.696	13.30	0.61
35	12.935	13.20	0.27

All values in volts unless otherwise noted.

APPENDIX D

Calculations and Experimental Data for the Switching

The current waveform of i_1 was found to make initial and final condition checks. Starting with equation III-7:

$$I_1 = \frac{20066(S+413.81)(S+212.77)(S+53865)\left[S+1.4887(10)^6\right]}{S\left[S+5.243(10)^6\right](S+5617)(S+226.21)\left[s^2+93122S+8.2672(10)^9\right]}$$

Making the partial fraction expansion, I_1 becomes

$$I_1 = \frac{259.12(10)^{-6}}{S} + \frac{7.4272(10)^{-6}}{S+226.21} - \frac{2.7891(10)^{-3}}{S+5.243(10)^6}$$

$$- \frac{155.82(10)^{-6}}{S+5617} + \frac{2.6778(10)^{-3}(S+46561)}{(S+46561)^2+(77713)^2} + \frac{72.319(10)^{-3}(77713)}{(S+46561)^2+(77713)^2}$$

Taking the inverse Laplace transform to obtain i_1,

$$i_1 = 259.12(10)^{-6}+7.4272(10)^{-6}\exp(-226.21t)-2.7891(10)^{-3}\exp\left[-5.243(10)^6t\right]$$

$$-155.82(10)^{-6}\exp(-5617t)+2.6778(10)^{-3}\exp(-46561t)\cos 77713t$$

$$+72.319(10)^{-6}\exp(-46561t)\sin 77713t.$$

At the time the SCR switches, the current flow in the transformer primary should be zero. Substituting t=0 in the equation for i_1 gives $i_1 = 0.584(10)^{-6}$ ma. When the SCR has been switched for a very long time ($t = \infty$) the current becomes

$$i_1 = (V_P-V_E-V_{AC})/(R_L+R_{AC}+R_E+R_{Trans.})$$

$$= 259.12(10)^{-6} \text{ ma.}$$

Substituting the value $t = \infty$ for time in the equation gives

$i_1 = 259.12(10)^{-6}$ ma. These checks both agree well within round off error.

The calculated and experimental data used to plot the waveforms shown in Figures 6 on page 15, and 7 on page 16 is shown in table IV.

TABLE IV

Calculated and Experimental Values of Output Voltage

Time (μs)	Experimental Data (Volts)	Calculated Points From Eg III-II (Volts)	Transformer Error (App. C) (Volts)*	Corrected Calculated Points (Volts)
0	0.0	0.002	0	-0.002
1	11.0	3.139	4.37	7.51
2	16.0	4.664	8.27	12.93
3	16.0	5.662	9.70	15.36
4	15.5	6.697	9.64	16.27
5	15.0	7.560	9.47	17.03
6	14.0	8.304	8.86	17.16
7	13.2	8.898	8.27	17.17
8	12.5	9.371	7.77	17.14
9	12.0	9.700	7.22	16.92
10	11.0	9.922	6.58	16.50
12	9.0	10.129	5.24	15.37
14	8.0	9.860	4.31	14.17
16	7.0	9.361	3.50	12.86
18	6.0	8.639	2.64	11.28
20	5.0	7.924	2.31	10.23
25	3.5	4.942	1.35	6.29
30	2.5	2.538	0.79	3.33
35	1.5	0.395	0.35	0.75

*Error voltage was adjusted for a 13 volt step.

APPENDIX E

Experimental Recovery Data

The data shown in Table V is the maximum time required from the opening of S_1 for C_2 to charge to 0.9 V_P. Data was taken by decreasing the pulse to pulse time until the following pulse occurred when the voltage across C_2 reached 0.9 V_P. The Recovery time was measured as the time S_1 was open.

TABLE V

Maximum Recovery Time

SAMPLE	TSW61S	2N886A
1	20.21	20.23
2	20.26	20.30
3	20.15	20.25
4	19.98	20.24
5	20.23	20.30
6	20.24	20.21
Avg	20.18	20.26

All times in milliseconds.

APPENDIX F

Noise Date - Experimental and Calculated

Figure 8, page 19, is plotted from the data in Table VI. This Table also includes the four points of experimental data shown in this figure. Only four points are shown due to lack of test equipment with capability to drive low impedance loads at fairly high voltages. The data has been normalized to V_p = 28 volts.

TABLE VI

Noise Amplitude Required to Misfire

Frequency (cps)	Calculated Peak Input	Experiment Peak Input
1	0.505	
2	0.508	0.50
3	0.512	
4	0.516	
5	0.521	0.50
6	0.524	
7	0.529	
8	0.533	
9	0.536	
10	0.540	0.536
20	0.575	
30	0.612	
40	0.645	
50	0.676	
60	0.706	0.768
70	0.735	
80	0.762	
90	0.789	
100	0.815	
200	1.039	
300	1.222	
400	1.385	
500	1.535	
600	1.656	
700	1.775	
800	1.888	
900	2.000	
1000	2.095	

APPENDIX G

Data Sheets

General. This Appendix contains the commercial information on the SCR, the Diode, and the transformer. Some calculations and experimental work are included here where parameters not specified by the data sheet were needed for the analysis. Only three items are included here as they are the only ones which are difficult to define. Each will be listed separately.

Transformer. This transformer defined by a Data Sheet. Measurement where made using a General Radio Impedance Bridge Type 1650-A and the information on inductance and resistance is listed in Table VII on page 48.

The mutual inductances were calculated from experimental data with the winding connected aiding and opposing. The Primary, Secondary, and Trinary winding are listed as shown in Figure 11 on page 33, in Appendix C.

Silicon Controlled Rectifier. Two SCR's were used in the calculations. The data sheets for the TSW61S are shown on pages 50, 51, 52, and 53; for the 2N886A on pages 54, 55, 56, and 57. The values for R_{AC} and V_{AC} were calculated from Figure 3 of the TSW61S data sheets; for R_{GC} and V_{GC} from Figure 11.

Diode. The diode used is a special version of the 1N661. This diode is screened to meet the following conditions over and above the data sheet requirements:

TABLE VII

Transformer Parameter

	Parameter	Measurement	Value Used
Winding Inductance	L_1	26.9 mh	26.9 mh
	L_2	218 mh	218 mh
	L_3	27.3 mh	27.3 mh
Winding Resistance	R_1	80 ohms	80 ohms
	R_2	225 ohms	225 ohms
	R_3	80 ohms	80 ohms
Mutual Inductance	$L_1+L_2+2M_{12}$	395 mh	
	$L_1+L_2-2M_{12}$	99.9 mh	
	$L_2+L_3+2M_{13}$	109 mh	
	$L_2+L_3-2M_{13}$	1.6 mh	
	$L_1+L_3+2M_{13}$	394 mh	
	$L_1+L_3-2M_{13}$	99.0 mh	
	M_{12}	74.9mh(+) 73.4mh(-)	73.5 mh
	M_{23}	26.3(+) 27.4(-)	26.5 mh
	M_{13}	74.8mh(+) 73.1mh(-)	73.5 mh

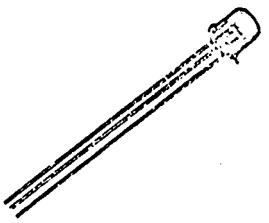
The (+) and (-) indicate values calculated from the aiding and opposing connections respectively.

Forward Voltage Drop	1.6 VDC Maximum at 20 ma
Reverse Current	5.0 μ amp maximum at 240 VDC
Reverse Recovery	0.3 μ sec maximum

The data sheet for this diode is on page 58.

Transitron CONTROLLED SWITCH

CONTROLLED SWITCH



1 ma to 200 ma

Transitron's silicon controlled switch is a PNPN bistable switching device. These units feature high gate sensitivity and low holding currents for low level switching from 1 ma to 200 ma. Further, these units are particularly useful in controlled rectifier trigger circuits as these switches offer precise and consistent control of the firing angle, and in circuits requiring fast switching speed.

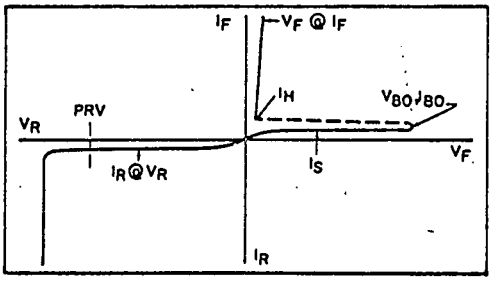
ABSOLUTE MAXIMUM RATINGS
(at noted ambient temperatures)

TYPE	Maximum Forward Voltage ①	Maximum Reverse Voltage
TSW31S	30	30
TSW61S	60	60
TSW101S	100	100
TSW201S	200	200

Average Forward Current:	200 ma @ 75°C
One Cycle Surge (60CPS @ 75°C)	1 A
Peak Gate Current @ 125°C for 8 msec	100 ma
Peak Gate Power @ 125°C for 8 msec	200 mW
Average Gate Power @ 125°C	20 mW
Operating and Storage Temperature Range:	-65°C to 150°C

SPECIFICATIONS AND TYPICAL CHARACTERISTICS
(at noted ambient temperatures)

Maximum Forward Voltage @ 25°C (V_F)	2V @ 200 ma 1.2V @ 10 ma
Maximum DC Forward and Reverse Currents @ Rated Voltage (I_S, I_R) ①	1 μa @ 25°C 20 μa @ 125°C
Maximum Gate Current to Fire @ 25°C (I_{GF}) ②	20 μa
Maximum Gate Voltage to Fire (V_{GF}) @ 25°C	1 volt
Maximum Holding Current @ 25°C (I_H) ②	1 ma
Minimum Gate Breakdown Voltage @ 25°C ③	-5 volts
Typical Output Capacitance @ 25°C	4 μμf
Typical Turn-on Time ($t_d + t_r$)	0.2 Microseconds
Typical Turn-off Time (t_o)	1.0 Microseconds



TYPICAL V-I CHARACTERISTICS

① With negative gate current of 20 μa
② Without gate bias
③ Voltage measured with inverse current of 10 ma

THIS BULLETIN SUPERSEDES TE-1356E DATED 8-60

TE-1356F 8-61

LITHO-IN U.S.A.

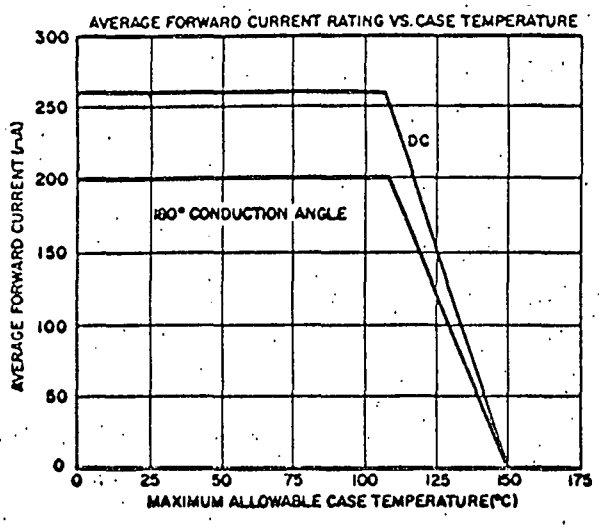


Fig. 1

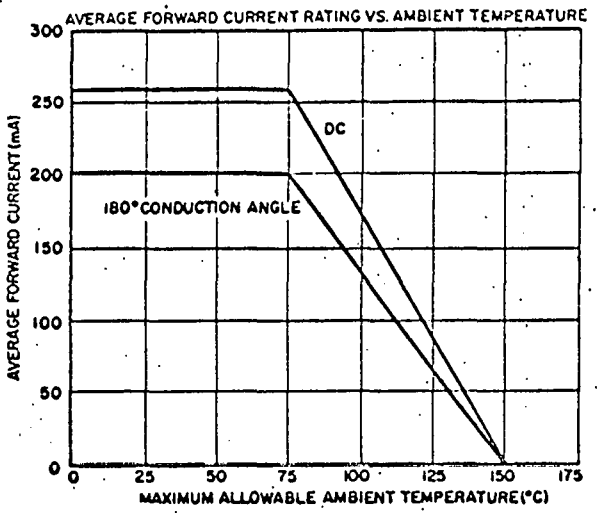


Fig. 2

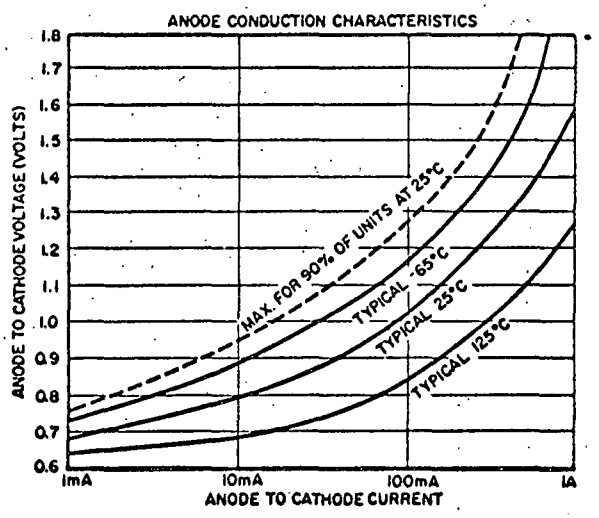


Fig. 3

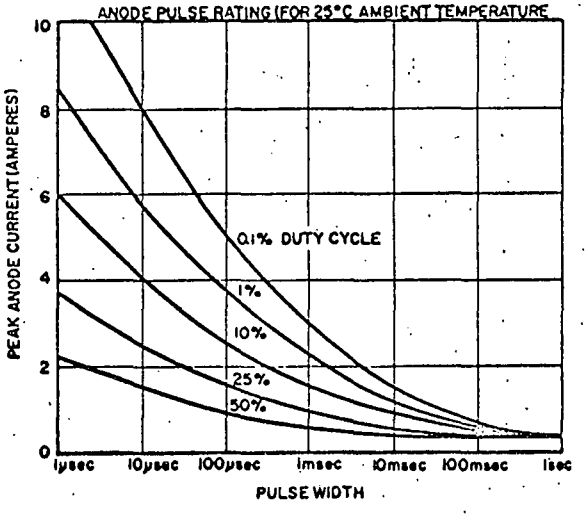


Fig. 4

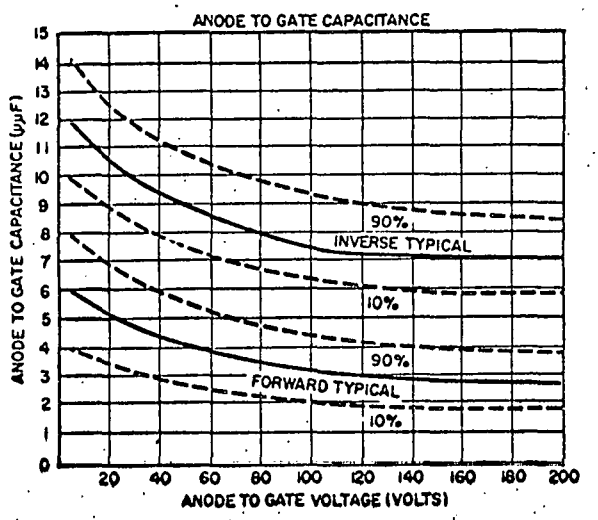


Fig. 5

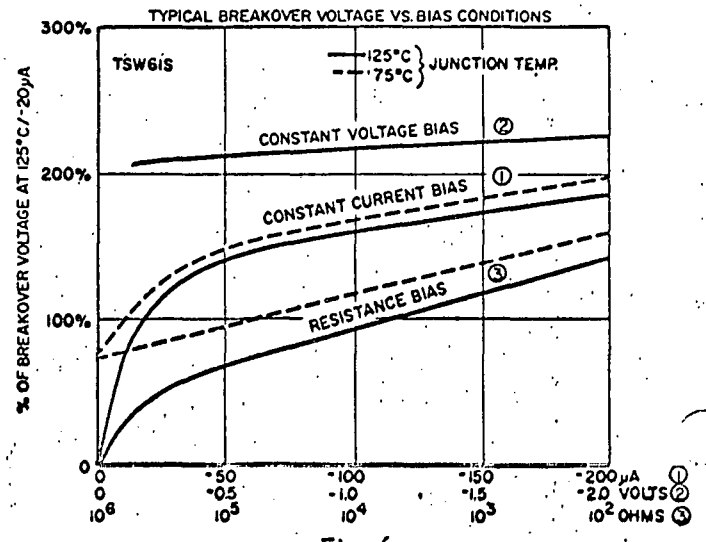


Fig. 6

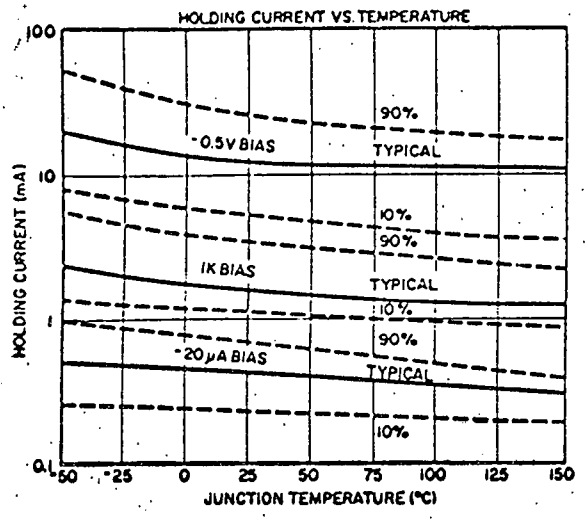


Fig. 7

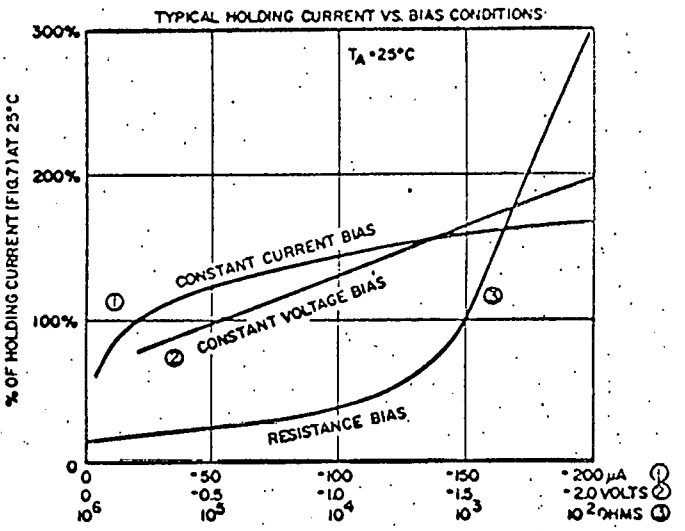


Fig. 8

GATE CHARACTERISTICS

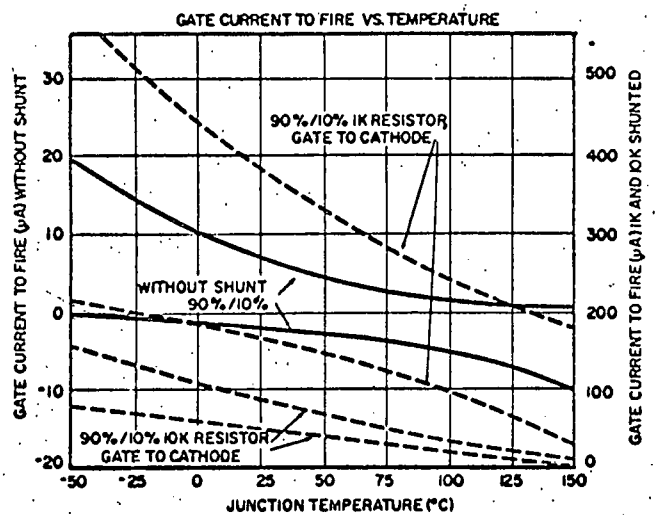


Fig. 9

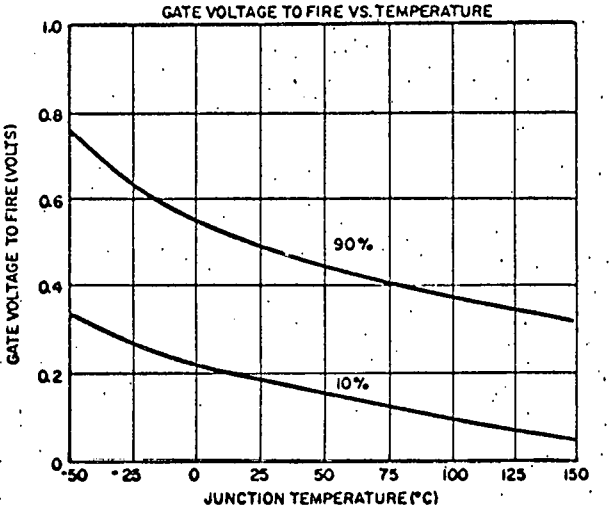


Fig. 10

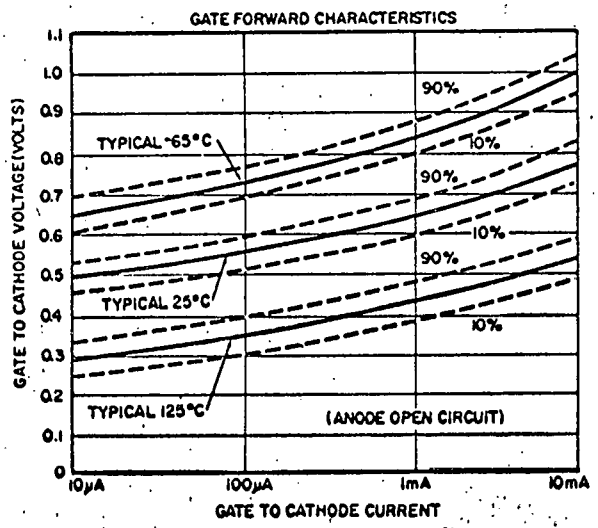


Fig. 11

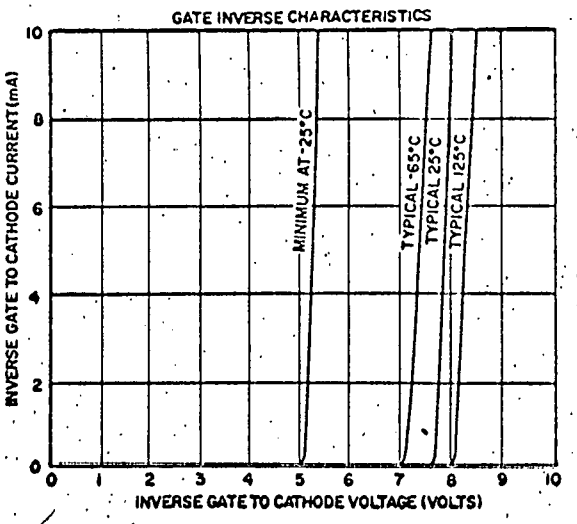


Fig. 12

SWITCHING CHARACTERISTICS

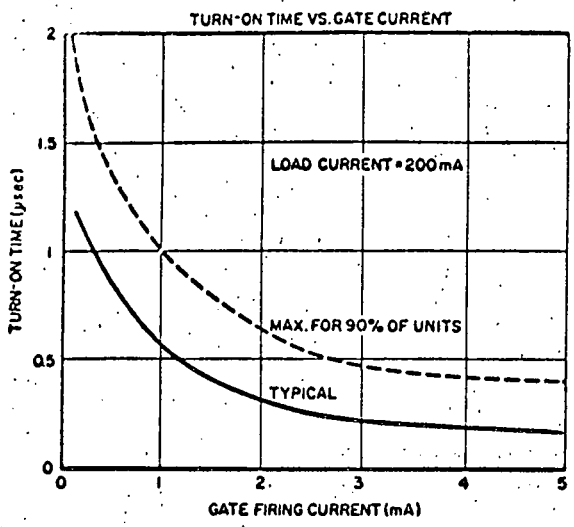


Fig. 13

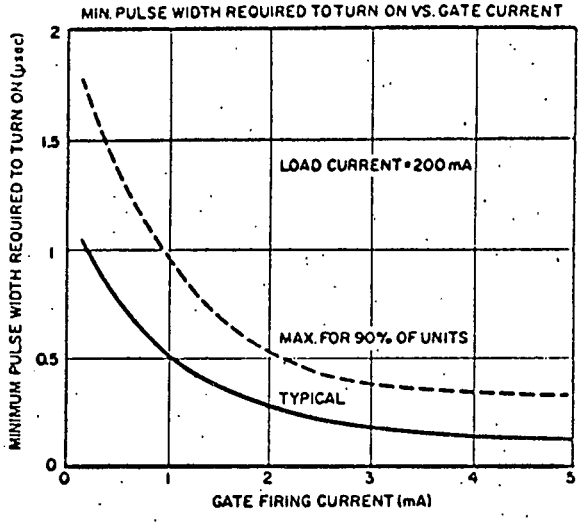


Fig. 14

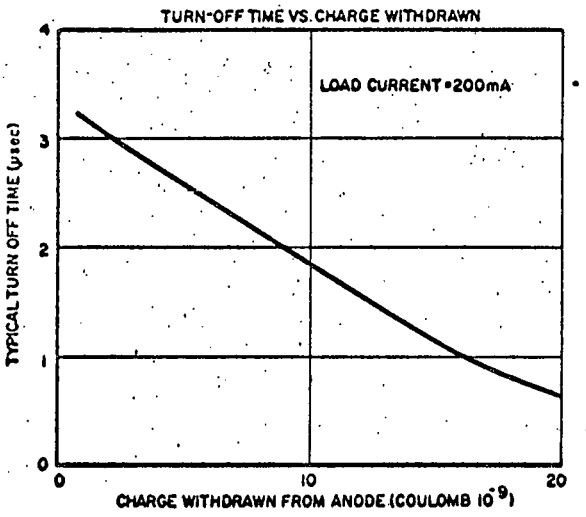


Fig. 15

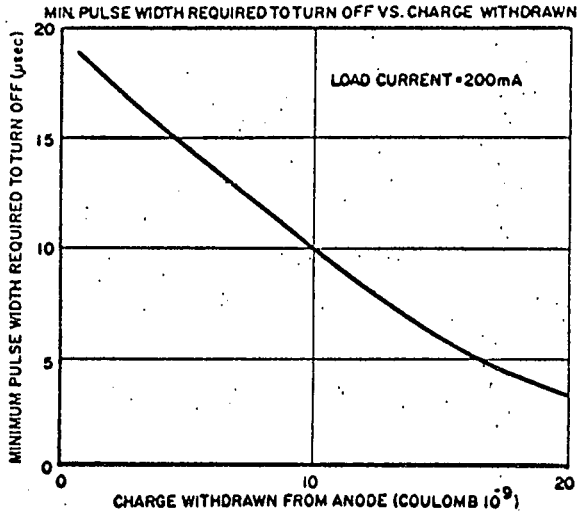
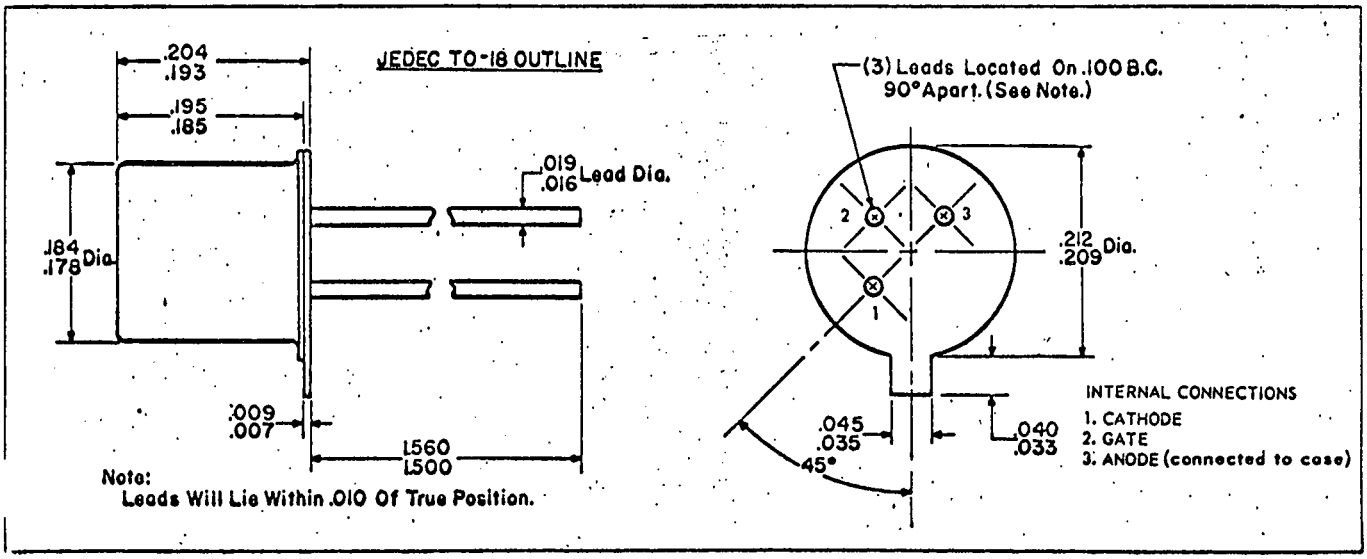


Fig. 16

MECHANICAL DATA



SILICON
DIFFUSED JUNCTION PNPN
CONTROLLED SWITCH

Types 54

2N884 2N887
2N885 2N888
2N886 2N889

C 420-03, 1-61

HIGH SENSITIVITY SERIES

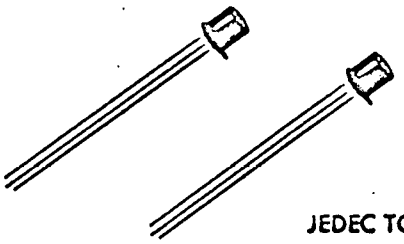
Available for the first time in the miniature TO-18 case, these units offer the same high sensitivity and close characteristics control introduced by SSPI in pioneering PNPN devices for control and logic applications.

The Silicon Controlled Switch (CS) is a three junction semiconductor device with thyratron-like characteristics. It will block in both its forward and reverse direction until turned on by a low level positive pulse to its gate. When "on", its forward direction has a very low impedance.

The precise firing characteristics of these devices make them ideal for timing and time delay circuits, voltage limit detectors, high gain static switching, logic circuits, and related applications.

With the high surge capability of this series, squib firing systems requiring pulse currents up to 5 amperes can be greatly miniaturized without sacrificing design margin. In addition, the low 1 mA holding current level is particularly useful in many programming, control and logic circuits.

Designed to meet the requirements of MIL-S-19500, these units are subjected to extensive temperature storage and cycling, as well as 100% acceptance testing, as a regular part of the manufacturing procedure.



JEDEC TO-18 CASE

- Operating D.C. current range 1-200mA
- Peak pulse current to 10 amps
- 20 μA maximum gate current to "fire"
- Firing voltage .52±.08V
- Voltage ratings to 200V
- Rise time typically 0.1 μsec.
- Low "on" voltage, 1.5V max. at 200mA

ABSOLUTE MAXIMUM RATINGS

Type	Anode Voltage (DC or Peak AC) ±Volts (Note 1)
2N884	15
2N885	30
2N886	60
2N887	100
2N888	150
2N889	200

Continuous D.C. Forward Current, 75°C Ambient	200 mA
100°C Case	350 mA
Peak recurrent Forward Current (Note 2)	up to 10 amps
Surge current, 0.05 seconds	5 amps
Peak Gate current	250 mA
Average Gate current	25 mA
Reverse Gate voltage	5 volts
Reverse Gate current	3 mA
Operating and Storage temperature range	−65 to +150°C

NOTE 1. With the gate biased off, the forward "breakover" voltage will occur at a value in excess of the rated anode voltage within the rated operating temperature range. See Bulletin D420-01 for specific design data on biasing.

NOTE 2. Limiting value based on pulse width, repetition rate, and operating temperature. See Curve 6.

SOLID STATE Products, Inc.
ONE PINGREE STREET • SALEM, MASSACHUSETTS
PIONEER 5-2900

SPECIFICATIONS

TESTS AT 25°C AMBIENT UNLESS OTHERWISE SHOWN

TEST	SYMBOL	MIN.	TYPICAL	MAX.	UNITS	CONDITIONS
"OFF" CHARACTERISTIC						
Anode cut-off current, 25°C	I_{AGO}	—	0.3	1	μA	V_{AC} = +Rating V_{GC} = −0.5V
125°C	I_{AGO}	—	5	20	μA	V_{AC} = +Rating, 125°C V_{GC} = −0.5V
Reverse anode cut-off current, 25°C	I_{AOR}	—	0.3	1	μA	V_{AG} = −Rating
125°C	I_{AOR}	—	5	20	μA	V_{AG} = −Rating, 125°C
Cathode cut-off current	I_{CGO}	—	0.5	10	μA	V_{CG} = 2V
"TURN ON" CHARACTERISTIC						
Gate current to "fire"	I_{GT}	—	5	20	μA	V_{AC} = +5V
Gate voltage to "fire"	V_{GGT}	.44	.52	.60	V	
Anode "on" voltage	V_{AGon}	0.7	1.1	1.5	V	I_A = 200 mA
Anode "firing" current (Note 1)	I_{AT}	—	100	—	μA	V_{AG} = +5V
Anode "drop-out" current	I_{AH}	0.1	0.6	1.0	mA	I_G = −50 μA
SWITCHING TIME						
Delay time	t_d	—	0.3	—	μsec	I_{GT} = 20 mA
Rise time	t_r	—	0.1	—	μsec	I_{Aon} = 500 mA
Gate time to hold (Note 2)	t_{GH}	—	0.2	—	μsec	
Gate time to recover (Note 3)	t_{GR}	—	10	—	μsec	I_G = −1 mA I_{Aon} = 500 mA

Note 1: For a maximum limit of 50 μA on this parameter, add suffix "/A" to type designation. For example, 2N885/A.

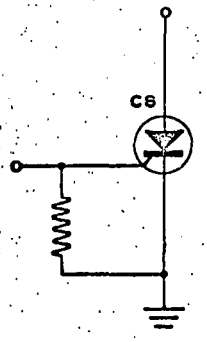
Note 2: Duration of gate trigger-on pulse must exceed t_{GH} for CS to remain in the "on" state.

Note 3: Anode voltage must be held at zero or a negative value for a time exceeding t_{GR} for CS to remain in the "off" state.

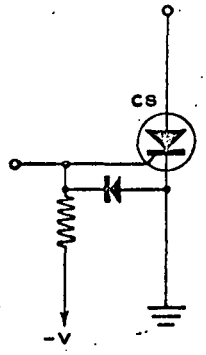
GATE BIAS CONSIDERATIONS

The CS is a very high gain device and should not be operated or tested with the gate open or floating. For operation up to 125°C junction temperature, a resistor between gate and cathode, (See Fig. 1) will provide adequate bias. Suggested values are 3.9K ohms up to 125°C, 12K ohms up to 100°C, and 27K ohms up to 75°C.

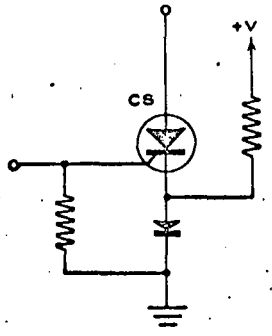
For maximum firing sensitivity as well as operation up to 150°C junction temperature, negative gate biasing is recommended. Figures 2 and 3 show two possible arrangements.



RESISTOR BIAS
FIG. 1



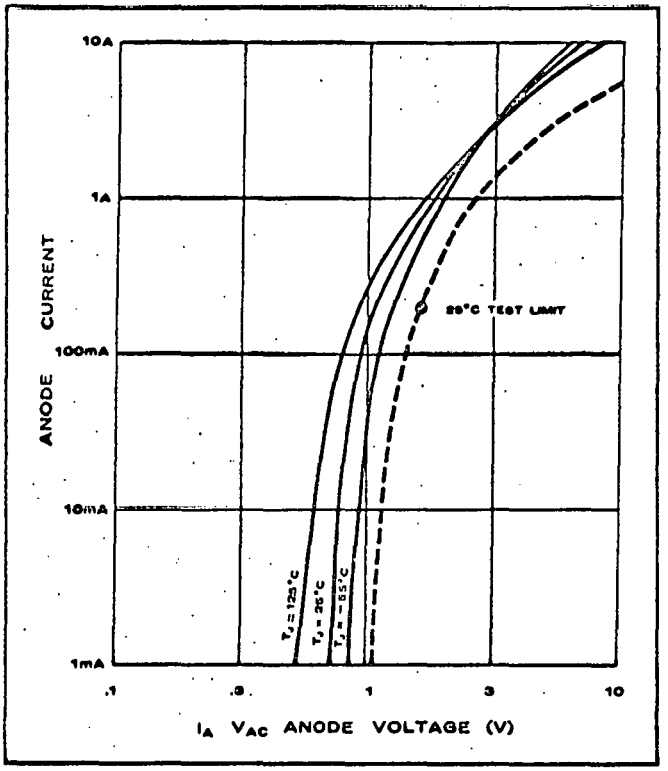
NEGATIVE GATE BIAS
FIG. 2



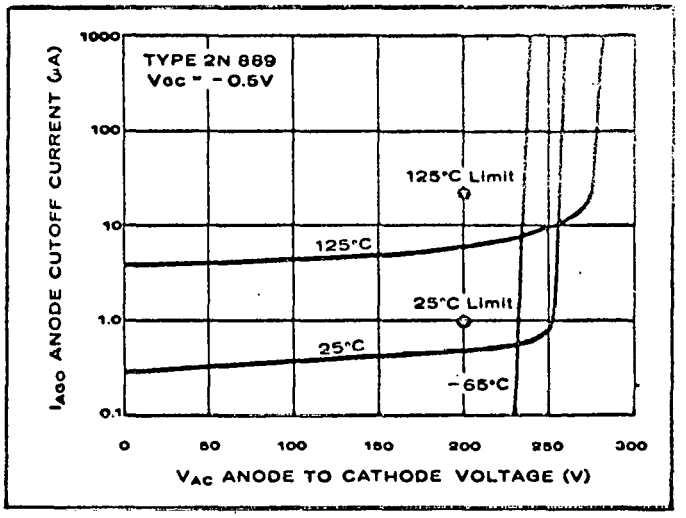
POSITIVE CATHODE BIAS
FIG. 3

DESIGN DATA CURVES

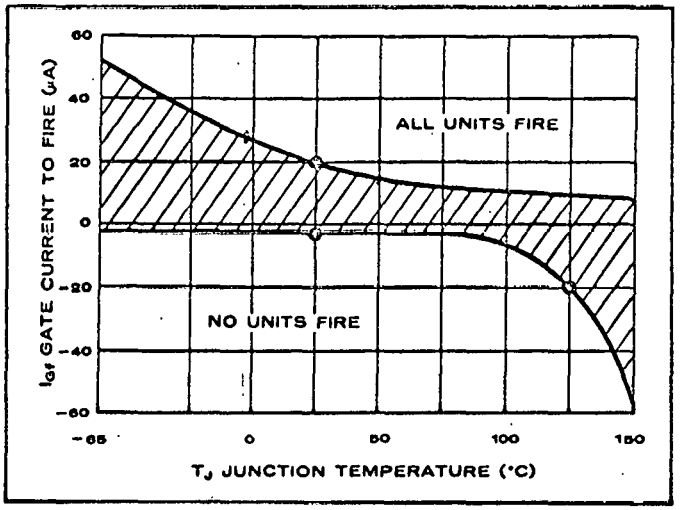
1. FORWARD "ON"



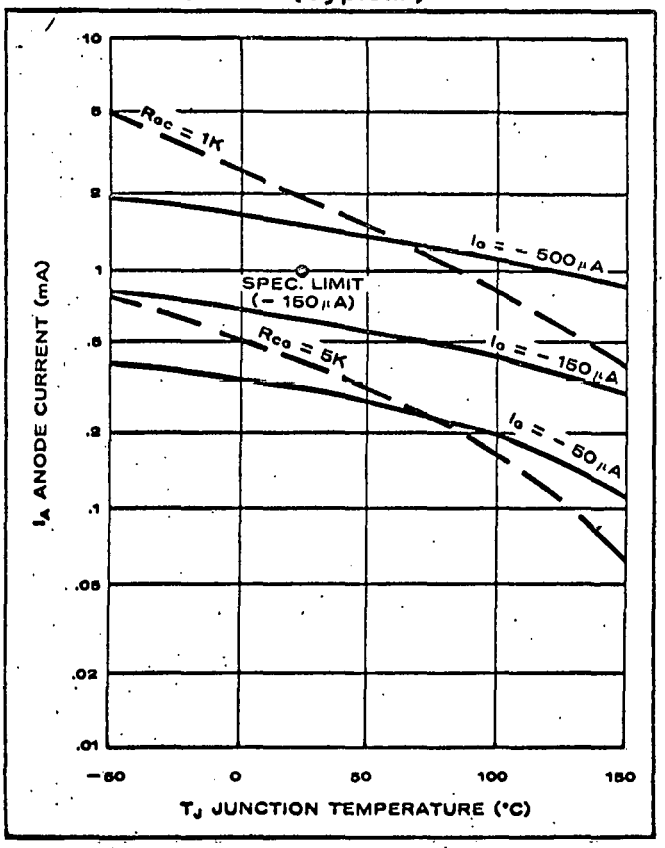
2. FORWARD CUTOFF



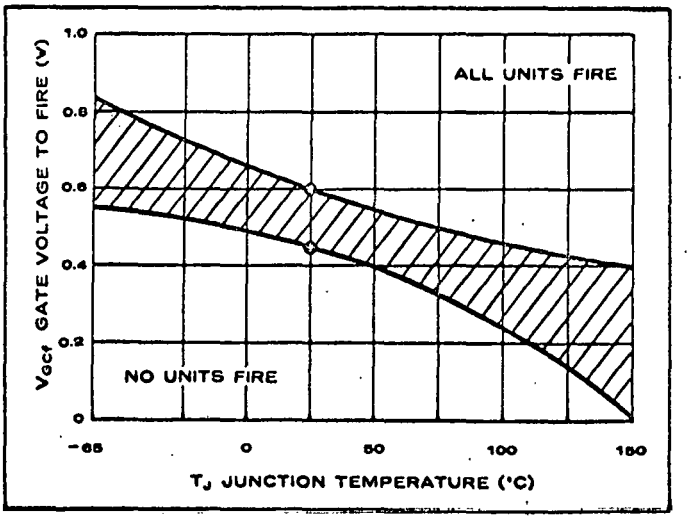
3. GATE FIRING CURRENT



5. ANODE DROPOUT (Typical)



4. GATE FIRING VOLTAGE

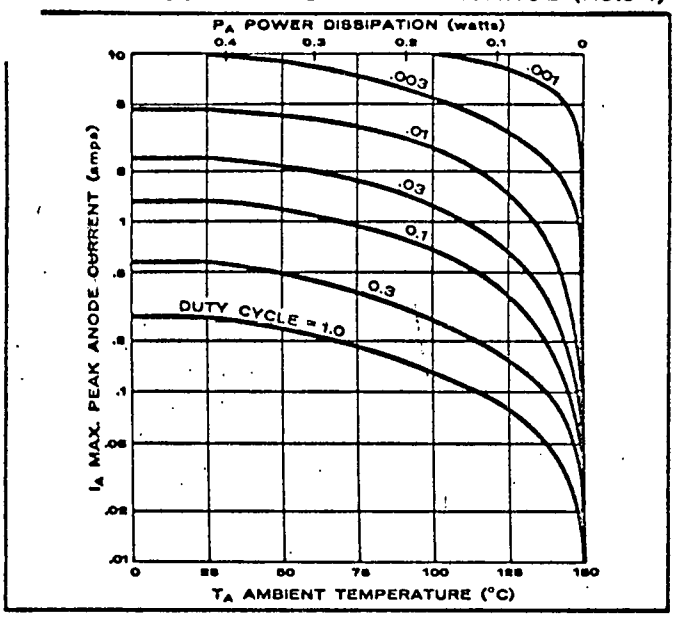


DESIGN DATA CURVES

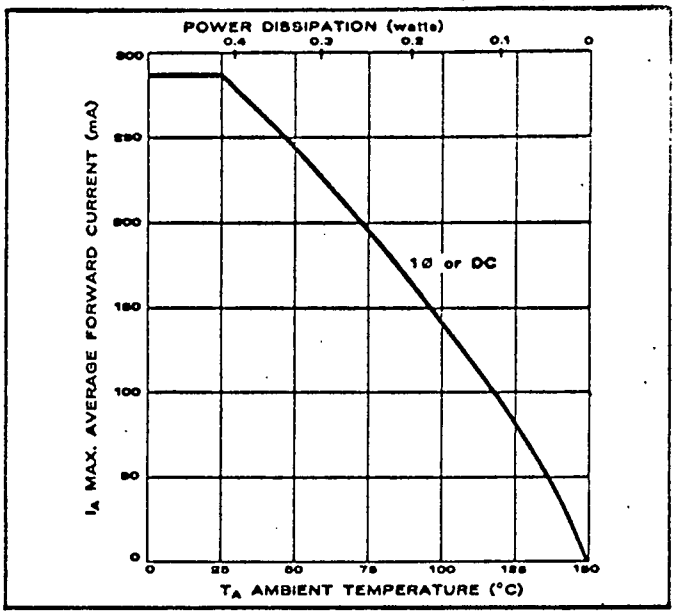
57

SSP

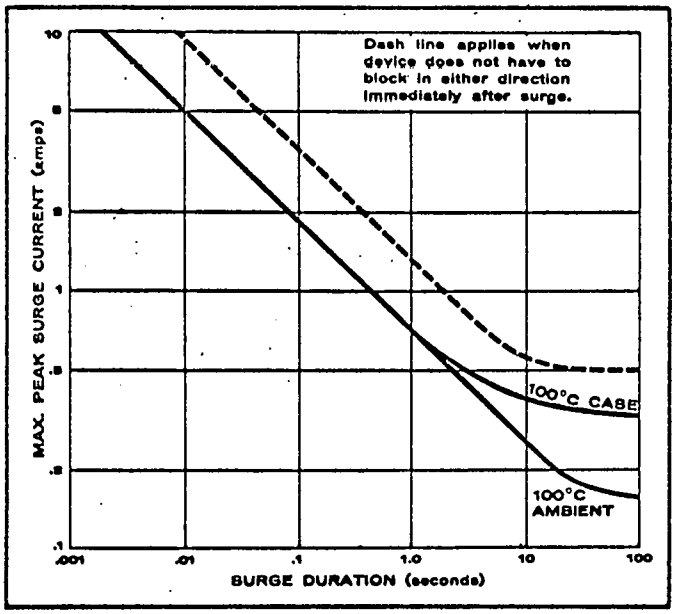
6. PEAK RECURRENT CURRENT RATINGS (Note 1)



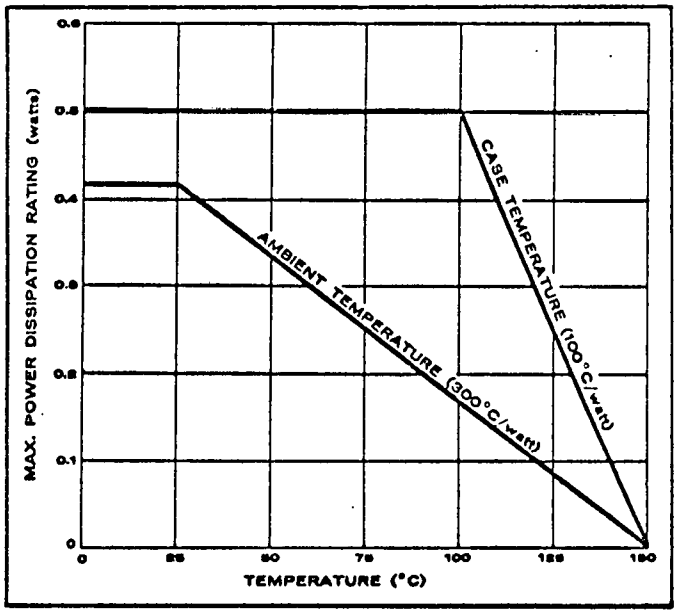
7. AVERAGE CURRENT RATINGS (Note 1)



8. SURGE CURRENT RATINGS

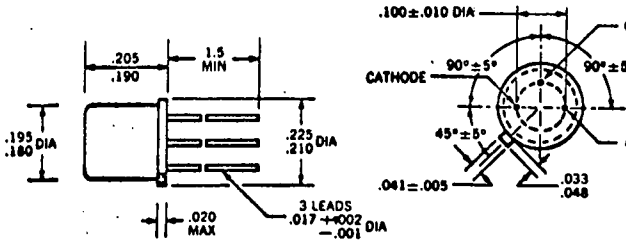


9. POWER RATINGS



Note 1: Curves 6 & 7 apply for repetition rates above 60 cps. Below 60 cps use DC rating.

MECHANICAL DATA



NOTE: Anode internally connected to case.

CASE: Welded hermetic seal. Glass to metal matched seals between case and leads.

FINISH: High dielectric silicone paint.

LEADS: Gold plated.

WEIGHT: Approx. 1 gm.

LEAD SOLDERING: Leads may be soldered to within 1/16" of base. Heat sinking not required if temperature-time exposure is less than 230°C for 10 seconds.

MOUNTING POSITION: Any

SOLID STATE Products, Inc.

ONE PINGREE STREET • SALEM, MASSACHUSETTS

PIONEER 5-2900

Printed in U. S. A.

TYPES 1N659, 1N660 AND 1N661
DIFFUSED SILICON HIGH POWER COMPUTER DIODES

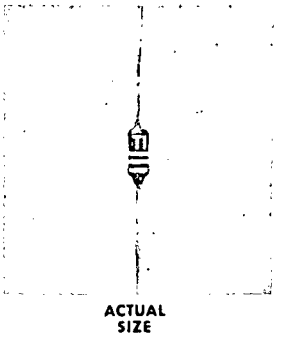
TYPES 1N659, 1N660 AND 1N661
PRODUCT SPECIFICATION No. DL-S 781, AUGUST, 1957

0.3 μsec. Maximum Recovery Time 50 to 200 VOLTS PIV

100 mA average rectified forward current

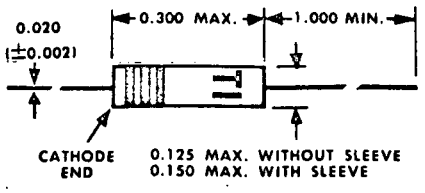
Ruggedized to meet stringent military requirements

Designed for • fast recovery • higher conductance
• low capacitance

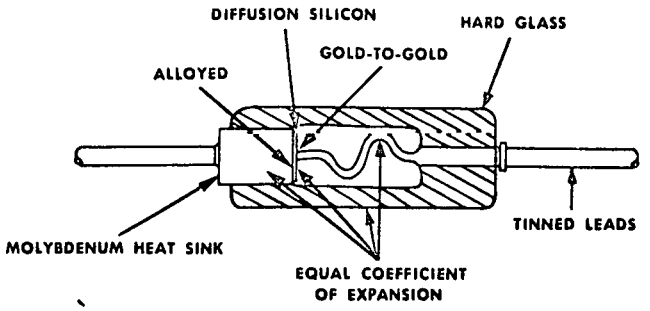


mechanical data

Hard glass hermetically sealed case with gold-to-gold contact. Unit weight is 0.195 gram.



ALL DIMENSIONS IN INCHES



maximum ratings

		1N659	1N660	1N661	
Peak Inverse Voltage at −65 to +150°C	PIV	50	100	200	V
Average Rectified Forward Current at +25°C	I_O	100	100	100	mA
Average Rectified Forward Current at +150°C	I_O	30	30	30	mA
Recurrent Peak Forward Current at +25°C	i_f	320	320	320	mA
Operating Temperature, Ambient	T_A	−65 to +150			°C
Altitude		100,000			ft

specifications

Minimum Breakdown Voltage at +100°C	V_Z	60	120	240	V
Maximum Reverse Current at PIV at +25°C	I_b	5	5	10	μA
Maximum Reverse Current at PIV at +100°C	I_b	25	50	100	μA
Maximum Voltage Drop at I_O = 6mA at 25°C	E_b	1	1	1	V
Maximum Reverse Recovery Time*		0.3	0.3	0.3	μsec
Typical Capacitance at −10V at 1 mc	C	2.7	2.7	2.7	$\mu\mu$fd

* Recovery time to 400K when switched from 30 mA forward current to −35V. Measurement made with a Hauman ND-1 standard pulse recovery test set approved by JETEC-14 and described in JAN-256.

SEMICONDUCTOR-COMPONENTS DIVISION

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