**THE PACIFIC NORTHWEST LABORATORY
HYBRID COMPUTER SYSTEM**

M. D. ERICKSON

JANUARY, 1968

**AEC RESEARCH &
DEVELOPMENT REPORT**

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HYBRID COMPUTER SYSTEM

By

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ABSTRACT

A hybrid computer system was developed by interfacing a Beckman Model 2133 analog computer with a Digital Equipment Corporation PDP-7 digital computer. The interface includes a 24 channel multiplexer, a high speed analog-to-digital converter, and 24 high speed digital-to-analog converters. Control interface circuits enable the digital computer to direct all hybrid functions. The hybrid computer system has been used in the simulation and control system development for the Fast Flux Test Facility.

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INTRODUCTION

Certain types of problems are best solved on digital computers, other problems on analog computers. Problems which are not easily solved on digital or analog computers alone are often times readily solved by a hybrid computer system where the advantages of both types of computers are available. For example, the analog computer is best suited to perform integration whereas the digital computer can perform logical operations and generate nonlinear functions. A hybrid computer can solve problems where the system can be described in terms of both discrete and continuous variables. A hybrid combines digital precision, logic capability, and storage capacity with analog speed, integration ability, and patch programming.

The need to simulate complex physical systems in real time and faster than real time (X10, X100, X1000), has stimulated computer manufacturers and users to devote considerable effort to developing hybrid computers. The ability to experiment directly and in real time with a hybrid dynamic model, as opposed to numerically solving complex sets of equations, speeds up the processes of system synthesis and system analysis.

The Pacific Northwest Laboratory (PNL) recognized the need for a hybrid simulator in its control system development for the Fast Flux Test Facility (FFTF).⁽¹⁾ The analog computer already in use was not large enough to simulate both a plant and complex control system. Since digital computers are rapidly becoming the standard controllers of large plants, further need for a hybrid system was apparent because digital control systems are not easily simulated by analog computers.

In the FFTF reactor dynamics simulation, the analog computer is used to solve the reactor kinetics and sodium coolant mixing by means of nonlinear differential equations, and the heat exchanger by solution of nonlinear partial differential equations.⁽²⁾ The digital computer supplies the variable time delay for both the coolant flow rate and the solution of nonlinear algebraic equations. The simulation of sodium pumps and pump drive assemblies is performed by the digital computer. Since a general purpose analog computer and a general purpose digital computer were available for development into a hybrid system, the interface hardware was purchased and the hybrid system developed.

The purpose of this document is to present a general description of the hardware and software associated with the PNL Hybrid Computer System. A discussion of the interface design evolution and subsequent development is included. The operating performance of the completed system is discussed. The instructions required to execute hybrid operations are also presented.

SUMMARY

The PNL Hybrid Computing System consists of a Beckman Model 2133 analog computer, a Digital Equipment Corporation PDP-7 general purpose digital computer, Adage Inc. data conversion equipment, and the associated control interface. The system provides complete hybrid capability for both data and control.

The data interface includes a 24 channel high speed multiplexer, an analog-to-digital converter, and 24 digital-to-analog converters. The digital computer performs the following control functions: (1) sets analog computer modes, (2) senses analog computer mode status, (3) addresses any

variable in the analog computer, (4) reads the value of a variable into core memory using the digital voltmeter, and (5) sets analog computer potentiometers.

A digital logic system was developed and installed in the analog computer to provide hardware programmable logic operations such as up-down counters, buffer and shift registers, gates, analog comparators, and analog switches.

SYSTEM DESCRIPTION

DIGITAL COMPUTER

The PDP-7 is a binary, fixed point digital computer containing 8,192 words of random access core memory, the hardware arithmetic option, two clocks, and 16 levels of automatic priority interrupt.⁽³⁾ The 18 bit word allows the user to directly address 8,192 core locations while executing a memory reference instruction. The computer (See Figure 1) has a basic read/restore cycle time of 1.75 μ sec, an add time of 3.5 μ sec, an average multiply time of 7 μ sec, and an average divide time of 11 μ sec.

Central Processor Modifications

The central processor has been modified to perform added arithmetic functions.⁽⁴⁾ Changes include the addition of the instructions Compare and Three-way Branch (CAS), One's Complement Subtract (SUB), and Increment the Accumulator (IAC). These instructions increase programming flexibility for direct-digital control studies and hybrid simulation.

Two clocks have been installed in the central processor. The first is crystal controlled with a frequency of 5 kHz, and the second operates from line frequency of 60 Hz. Both clocks operate through the Automatic Priority Interrupt as interval timers.

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FIGURE 1. PDP-7 and Hybrid Interface

Peripheral Devices

The PDP-7 has associated with it peripheral devices that allow input and output of user programs and data. A simplified block diagram of the system is shown in Figure 2.

A Model KSR 35 Teletypewriter is interfaced to the computer. It operates in simplex or duplex mode, and off-line. Standard PDP-7 programs using the KSR 35 have been modified to utilize automatic vertical and horizontal tabulation and form feed.

A 300 character per second paper tape reader and a 63 line per second paper tape punch provide high speed paper tape input/output with the PDP-7. These units utilize fan-fold paper tape having eight channels of data processed in either alphanumeric or binary modes.

A dual Dectape, Type 555, is coupled to the digital computer. This magnetic tape system provides high density program and data storage that is easily and quickly transferred into and out of core memory. Each reel of tape contains three million bits of information, and data is transferred at the rate of 90,000 bits per second.

A 25,000 word drum memory is an integral part of the digital computer. This drum, having an average access time of 20 msec, and a transfer rate of 50,000 words per second is used for bulk storage of user programs. The drum transfers blocks of data to and from core memory via the Data Break facility of the PDP-7.

Source program card decks and data cards may be input to the PDP-7 through an IBM 713 card reader. It reads cards under program control at the rate of 150 cards per minute. Cards are used when off-line program preparation or on-line program modification is desired.

FIGURE 2. Hybrid Computer System Simplified Block Diagram

Software

The software package provided with the PDP-7 has been modified for improved operation and to satisfy the needs of the existing hardware configuration. Hybrid software has been developed to provide the user with the required functions in simulation and control studies. This software includes function generation, logarithms, time delays, limiters, and two and three mode control routines. The hybrid utility program library includes an automatic analog computer potentiometer setting routine, a drum/core memory data transfer routine, and analog/digital data converter interface servicing routines.

Input and Output

Transfers of data between the PDP-7 and the hybrid interface occur through the Information Distributor and Information Collector, which are connected directly to the accumulator of the digital computer. Transfers of control signals from the PDP-7 to the interface occur through the memory buffer and device selector. Control signals (flags) from the interface to the PDP-7 occur through the Skip, Program Interrupt, and Automatic Priority Interrupt facilities. Figures 3 and 4 show the standard input and output data interface.

Excessive current flow on the analog computer's high quality ground lines would result in a degradation of analog signals. To avoid excessive current flow, isolation of analog and digital computer grounds was implemented. Pulse transformers provide the isolation for digital data that is pulsed between the digital computer and the interface. One side of the transformer primary is connected to the analog computer ground, and one side of the secondary is connected to the digital computer ground. Isolation of logic levels is obtained using a floating digital driver (refer to Appendix A).

FIGURE 3. PDP-7 Input Data Transfer

FIGURE 4. PDP-7 Output Data Transfer

To control the transfer of information to and from the I/O bus, input/output transfer (IOT) instructions are used in the PDP-7. Six of the eighteen bits in the instruction word specify which interface device is to be involved in the data transfer. Three bits command the issuing of three input/output pulses (IOPs) to execute the instruction, and four bits may be used for microcoding. In this fashion, instructions may be created in order to execute an input/output operation or checking a status flag. An explanation of IOT instructions and diagram of the device selector are contained in Appendix B. The Digital Logic Handbook gives a description of the symbology used in the PDP-7 and control interface logic diagrams.⁽⁵⁾

ANALOG COMPUTER

The Beckman Model 2133 analog computer (See Figure 5) contains 156 amplifiers, 72 integrators, 32 multipliers, and 16 function generators. It has 240 servo-set pots that utilize the DO/IT system. This computer contains two iterative mode controllers (IDACAS). The Model 2133 may be coupled to a Beckman Model 1132 analog computer for added hardware capability to solve large problems. The Model 1132 analog is slaved to the mode controls on the Model 2133, and data is transferred between the two on coaxial trunk lines. Both the Model 2133 and the Model 1132 are vacuum tube computers having relay switching, except for mode control, which is solid state. Peripheral devices for the Model 2133 analog computer include an X-Y plotter, a Brush eight-channel strip-chart recorder, a cathode-ray tube display, a Friden flexowriter, and a Tektronix type 564 storage oscilloscope.

A Digital Logic System (DLS) has been developed and made an integral part of the Model 2133 analog computer (See Figure 6). The DLS utilizes Digital Equipment Corporation Logic Laboratory hardware and "Flip Chip" logic modules.⁽⁵⁾ It is programmed

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FIGURE 5. Hybrid Computer System

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FIGURE 6. Digital Logic System Panel

by means of nonshielded patchcords in the conventional analog manner. This logic system extends the capability of the Model 2133 analog computer by adding flexible logical operations such as up-down counters, preset counters, buffer and shift registers, gates, analog comparators, and analog switches. The digital logic provides program interrupt signals that are dependent upon the value (voltage) of an analog variable. It also provides analog computer "flags" that will initiate, upon flag searching, a digital computer program branch.

HYBRID CONTROL INTERFACE

The control interface consists of the digital logic that provides the decoding, signal conditioning, and gating of information between the PDP-7 and Model 2133 computers. A detailed block diagram of the interface is shown in Figure 7. Most operations normally carried out by means of controls on the analog computer console may be performed through the control interface by executing hybrid instructions in the PDP-7. The PDP-7 functions as the master of the hybrid system since it sends all system control signals, and senses the status of all control modes by searching flags.

The hybrid control interface (See Figure 8) is constructed using two-megahertz "Flip-Chip" digital logic modules. A list of the engineering drawings that describe the interface is given in Appendix C. Control interface status indicators (See Figure 9) are mounted at the top of PDP-7 computer Bay 5 for easy observation.

Model 2133 Analog Computer Address Select

The analog computer address select circuitry enables the digital computer to select any address on the Model 2133 analog console. This circuitry is used for reading analog variables through the digital voltmeter, setting pot coefficients, checking

FIGURE 7. Hybrid Interface Detailed Block Diagram

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FIGURE 8. Hybrid Control Interface

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FIGURE 9. Control Interface Indicator Panel

BNWL-538

amplifier initial conditions, as well as addressing data lines to the hybrid interface and trunking lines to the Model 1132 analog computer.

The addressing function is performed, first, by loading the PDP-7 accumulator with the binary-coded-decimal (BCD) value of the address to be selected. The alpha-decimal to BCD equivalence is shown in Table I. The format used, and an example for addressing are shown in Table II. Alpha-decimal to BCD conversion subroutines are used to facilitate addressing.

The instruction Analog Address Load (AALD) clears a 16 bit buffer register and loads it with the contents of the accumulator (See engineering drawing H-11-2170 listed in Appendix C). The output of the buffer register is decoded from BCD to decimal. The decimal value is then sent to solenoid drivers which operate the cross-bar selector relays in the Model 2133 analog computer address circuitry.

The instruction Analog Address Load also sets a flip-flop which operates control relays in the analog computer that enable the PDP-7 to have complete control over the Model 2133 analog computer. This action makes it impossible for an operator to enter any operations through the analog console or DO/IT system. The Hybrid Address operation energizes the manual select relay that is used when changing address, energizes a DO/IT disable relay, and energizes the K12B relay which transfers the servo-set pot system to the Hybrid reference divider and disconnects all other reference dividers. After the Analog Address Load instruction is initiated, a solenoid driver is enabled for 25 msec to operate the crossbar release (RLS) relay in the Model 2133 analog computer. This relay momentarily lifts the hold down bars on the crossbar relays to allow them to change address.

TABLE I. *Alpha-Decimal to BCD Conversion*

<u>ALPHA</u>	<u>DECIMAL</u>	<u>BCD</u> <u>8421</u>
A	0	0000
F	1	0001
G	2	0010
K	3	0011
L	4	0100
M	5	0101
P	6	0110
R	7	0111
T	8	1000
U	9	1001

TABLE II. *Accumulator Values for 8421 BCD Used for Analog Address*

ACC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
			8	4	2	1			2	1	8	4	2	1	8	4	2	1
	<u> </u>		<u> </u>				<u> </u>		<u> </u>		<u> </u>				<u> </u>			
	SPARE		ALPHA				SPARE		HUNDREDS		TENS				UNITS			

ADDRESSING EXAMPLE

XX	<u>0110</u>	XX	<u>01</u>	<u>0010</u>	<u>0110</u>	BCD ADDRESS
	P		1	2	6	ALPHA-DECIMAL ADDRESS

Since the relays in the crossbar selector require approximately 10 msec to operate, digital computer operations must be regulated by flags that are timed in relationship to analog control functions. Figure 10 shows the timing circuits that regulate addressing, DVM, and pot coefficient operations.

Referring to the timing diagram in Figure 11, the instruction Analog Address Load triggers an integrating single shot. This single shot is also integrated by Pot Coefficient Load and DVM Read operations. The total time required to perform

FIGURE 10. Control Interface Timing Circuits

FIGURE 11. Timing Diagram of Addressing Functions

two or three of these operations may be decreased if they occur simultaneously. A single flag (Relay Flag) serves as the integrating indicator for all three functions. This flag will not be set until 22 msec after AALD or PCLD is executed, or 22 msec after the DVM relay buffer is loaded. This delay provides time for relays to operate and for registers to be loaded before additional operations are executed.

Another integrating single shot is used to regulate the length of time the PDP-7 has control of the Model 2133 analog computer. The operations Analog Address Load, Relay Flag, and Servo Flag all integrate a three second single shot.

The purpose of this delay is to allow the DVM time to read the value of the last function executed. At the completion of this delay, a clear signal (AUTO CLEAR) decouples the digital computer control circuits from the analog computer. This enables the user to manually operate any of the controls on the analog console.

Pot Coefficient

The pot coefficient circuit (See engineering drawing H-11-2171 listed in Appendix C) enables the digital computer to automatically set pots in the analog computer. Previously, the pots were set using the DO/IT system of the Model 2133 analog computer. Setting the pot coefficients using the digital computer affords several advantages over the DO/IT system.

1. Setting a pot from the PDP-7 requires about 2.5 sec as compared to 5 sec required by the DO/IT.
2. Using the digital computer enables the user to employ sub-routines that calculate coefficients prior to setting the pot. This eliminates time consuming manual calculations.
3. The pot set routine (program) will make three attempts to set a pot to within ± 2 parts in 1000. If the pot will not set within this tolerance, a message will indicate the

error and proceed to the next pot. When the pot set routine has been completed, the user may then treat all exceptions manually.

The BCD value of the pot coefficient is loaded into the accumulator in the format shown in Table III.

TABLE III. Accumulator Values for 8421 BCD Used for Pot Coefficient

ACC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	<u> </u>		<u>8 4 2 1</u>				<u>8 4 2 1</u>				<u>8 4 2 1</u>				<u>8 4 2 1</u>			
	SPARE		THOUSANDS				HUNDREDS				TENS				UNITS			

The pot coefficient 16 bit buffer register is cleared and loaded with the contents of the accumulator using the instruction Pot Coefficient Load (PCLD). The output of the buffer register is decoded from 8421 BCD to 2421 BCD. The 2421 BCD is sent to solenoid drivers that operate the hybrid relay-set reference divider in the interface. The output of the hybrid reference divider is used in the servo-set pot system just as the DO/IT reference divider, or manual reference divider, provides a reference voltage. The relay set reference divider is a commercial unit purchased from Beckman. The relays switch precision resistors to obtain a fraction of the 100 volt reference for the servo amplifier to null against. The relays also have contacts that are used to operate indicator lamps.

DVM Readback

The DVM Readback circuits enable the user to command the DVM in the Model 2133 analog computer to convert the addressed value from an analog voltage to a digital data word. This digital data is then input to the PDP-7.

The PDP-7 executes a DVM read operation while having control of the analog console. The circuits that control the DVM readback are shown on Engineering Drawing H-11-2172 (Appendix C). The DVM Read (DVMR) instruction initiates a pulse that

is delayed and sent to an indicator driver to operate a relay. The relay operation causes the DVM to track once and load its relay buffer register. A gating network decodes the decimal data held in the relay buffer to 8421 BCD. When the DVM has completed loading its relay buffer, it generates a contact closure indicating that the buffer contents may be read. This contact closure is the input to a Schmitt trigger which triggers a pulse amplifier. The pulse amplifier clears and loads the DVM readback 18 bit flip-flop buffer register in the interface with the BCD value of the DVM voltage. The contents of the buffer register may then be read into the accumulator at any time using the instruction DVM Load (DVML). The format of the DVM data is shown in Table IV.

TABLE IV. Accumulator Values for 8421 BCD DVM Readback

ACC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	┌	└	<u>8 4 2 1</u>				<u>8 4 2 1</u>				<u>8 4 2 1</u>				<u>8 4 2 1</u>			
			TENS				UNITS				TENTHS				HUNDREDTHS			
			OR HUNDREDS				TENS				UNITS				TENTHS			
			DECIMAL (=XXX.X WHEN ONE XX.XX WHEN ZERO)															
			SIGN (MINUS = ONE) (PLUS = ZERO)															

Model 2133 Analog Computer Mode Control and Set Lines

The hybrid control interface contains 12 set lines, five of which are used to set analog computer modes, one to operate the servo-set pot system, and six for general purpose use. Engineering Drawing H-11-2173 (Appendix C) shows the circuitry used for the mode control and set lines.

All mode set operations are generated by PDP-7 IOT instructions. Each IOT pulse goes to a delay which operates an indicator driver. The indicator drivers switch solid state circuitry in the analog computer mode control, and operate a relay that initiates a servo operation. All other set lines

go directly to the Digital Logic System in the analog computer. Each has a unique instruction associated with it, so that the programmer has flexibility in patching the desired function at the DLS.

Sense and Program Interrupt Lines

A total of 12 sense lines and 12 program interrupt lines are included in the interface. The servo and each of the five analog computer modes has a sense line associated with it. Six other sense lines are available at the DLS in the analog computer. These lines have general purpose use and are terminated at the Skip facility in the PDP-7. They may be patched in any desired manner on the DLS patchboard. The 12 program interrupt lines are terminated on the DLS panel. In the PDP-7, the lines are terminated at either the Program Interrupt (PI) facility, or the Automatic Priority Interrupt (API) facility.

The signals sensed at the DLS must be standard "Flip-Chip" voltage levels (as would normally be the case using the DLS logic). The signals going to the PDP-7 are buffered by inverters or line drivers. The analog computer mode and servo sense signals are converted from nonstandard signals to "Flip-Chip" logic levels, sent through a floating digital driver (Refer to Appendix A), buffered by inverters, and wired to the Skip facility in the PDP-7.

HYBRID DATA INTERFACE

The data interface between the PDP-7 digital computer and Model 2133 analog computer (shown in Figure 12) consists of a multiplexer, an analog-to-digital (A/D) converter, and digital-to-analog (D/A) converters. The converters are high quality, of the fastest and most accurate available.

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FIGURE 12. *Hybrid Data Interface*

Multiplexer and Analog-to-Digital Converter

Table V lists the salient performance characteristics of the multiplexer/analog-to-digital converter system.

TABLE V. Multiplexer and Analog-to-Digital Converter Performance Characteristics

Adage Model VMX-24B-64 Multiplexer

Number of channels	24 (expandable to 64 by addition of logic cards)
Input impedance	100 k Ω
Analog input	± 100 V full scale 100% overload for short duration
Analog output	± 20 V full scale
Addressing modes	Sequential Repetitive Random Manual
Setting time to system accuracy	8 μ sec

Adage Model VT 13-AB Analog-to-Digital Converter

Analog input	± 20 V full scale
Digital output	13 bits plus sign, one's complement binary
Conversion period to system accuracy	4 μ sec
Control indicators	Busy Overload

Multiplexer and Analog-to-Digital Converter System

Accuracy	$\pm 0.025\%$ of full scale + 1/2 LSB at 25 °C
Resolution	12.2 mV
Throughput rate	85 kHz
Digital logic levels	"0" = 0 V "1" = -3 V

Functional block diagrams of the multiplexer and A/D converter are shown in Figures 13 and 14.

Operation and instruction manuals describing the multiplexer and A/D converter have been supplied with the equipment.⁽⁶⁾ A calibration procedure and automated PDP-7 calibration program have been written for the multiplexer and A/D converter.

An interface (See Engineering Drawing H-11-2177, Appendix C) was developed to allow the PDP-7 to control the multiplexer and A/D converter. Two flip-flops (mode select) are used as memory elements to indicate to the multiplexer whether random, sequential, or repetitive addressing is to be used. These flip-flops are set by the instructions Multiplexer Random (MXRN), and Multiplexer Repetitive (MSRP), and cleared by Multiplexer Sequential (MXSE).

The overload signal from the A/D converter is in the output buffer register along with the output data. An overload occurs whenever the input to the multiplexer channel being converted is greater than ± 100 V. An interface was required to provide better PDP-7 program use of the overload data. The overload bit is sampled by the digital computer at the same time as the contents of the A/D converter output register are loaded into the accumulator using instruction A/D Read Buffer (ADRB). Tables showing the binary-to-voltage conversion relationship are given in Appendix D. The additive voltage weighting of each accumulator bit is the same for the A/D converter output and the D/A converter input; to determine the voltage equivalent of a binary word it is necessary to add the voltage value of each of the 13 bits.

If the overload bit is set, meaning that the data in the A/D converter buffer register is not valid, a flip-flop (OVL D) in the interface is set. The output of this flip-flop is wired to Automatic Priority Interrupt (API) Channel No. 4. If

FIGURE 13. Multiplexer Functional Block Diagram

FIGURE 14. A/D Converter Functional Block Diagram

the API is enabled and channel No. 4 is "ON," an interrupt will occur. The computer will automatically clear the OVLD flip-flop at the beginning of the interrupt service routine. The overload flag is also wired to the Skip facility of the PDP-7 where it may be used in a flag search mode. The instructions Skip if Overload Flag is Set (ADOV), and Clear All Flags (CAF) will clear the overload flag. An indicator lamp on the control interface indicator panel, shown in Figure 9, indicates when the A/D converter is overloaded.

Digital-to-Analog Converters

The data interface contains 24 channels of D/A converters. Table VI shows the salient performance characteristics of the D/A converter system.

TABLE VI. Digital-to-Analog Converter Performance Characteristics

Adage Model 8Y15 Digital-to-Analog Converter Specifications

Number of channels	24 (expandable to 64)
Conversion rate	500 kHz maximum exclusive of output amplifiers
Accuracy	$\pm 0.01\%$ of full scale $\pm 1/2$ LSB at 25 °C (FS = 200 V)
Settling time to accuracy of the system	50 μ sec to 0.01% of final value with 2000 pF load.
Analog output	± 100 V full scale
Current output	15 mA
Maximum capacitive load	50,000 pF
Digital input	13 bits plus sign, one's complement binary, single buffered
Logic levels	"0" = 0 V "1" = -3 V

Operation and maintenance manuals describing the D/A converters were supplied with the equipment.⁽⁷⁾ A PDP-7 calibration program has been written for the D/A converter subsystem.

The D/A subsystem (See Figure 15) includes a distributor which fans out data and decoded address information for 64 channels of single buffered D/A converters whose analog outputs can vary within ± 100 V at ± 15 mA. Each output is provided with a "zero order hold," i.e., when changed, the output goes to its new value and is held constant until subsequently changed.

The D/A converter interface (See Engineering Drawing H-11-2178, listed in Appendix C) consists of high fan out inverters between the information distributor of the PDP-7 and the data input of the converters. The instructions used to randomly address, load the input buffer, and initiate a conversion for each D/A channel have been microcoded so that a single instruction will perform all three operations. The D/A convert command is an IOT instruction. The IOT pulse that loads data into the D/A input register is delayed, and then used to load the channel address and supply a convert pulse.

HYBRID SOFTWARE

Eighty-four instructions were added to the PDP-7 library with the addition of the hybrid interface. These instructions are all input/output transfer (IOT) operations. A description of all hybrid instructions is given in Appendix E. The hybrid mnemonic instructions have been added to the standard extended assembler of the PDP-7 to form the hybrid assembler. This assembler is available on both Dectape and paper tape (binary). The hybrid assembler has been modified to recognize voltage and ratio inputs and convert them to the binary equivalent (Refer to Appendix D). For example, in normal program assembly the number 76.39 would be interpreted by the assembler to be 76.39 V. It would automatically convert this voltage to the binary number 000 001 100 001 110 010.

FIGURE 15. D/A Converter Subsystem Functional Block Diagram

Analog Computer Control Routines

The mode function instructions enable the PDP-7 to control the Model 2133 analog computer in the hold, initial condition, pot set, standby, compute, and servo modes. Additional control instructions enable digital control of the address, pot coefficient, and DVM circuits. Sample subroutines showing how these instructions may be used are given in Appendix F. Analog Computer mode controls enable the hybrid programmer to use the system in any type of iterative operation. This function was previously performed (with limitations) in the analog computer by the IDACAS unit.

Analog-to-Digital Conversion Routines

Sample subroutines that may be used to initiate an A/D conversion are shown in Appendix G. There are two basic methods by which an analog input to the multiplexer may be converted to a digital equivalent, described below.

Method I

The multiplexer is first set to the random address mode by executing the instruction MXRN. Thereafter, the instruction $MX\alpha$, where α is the channel number (0-23), is executed. The $MX\alpha$ instruction is microcoded to include the multiplexer channel number to be converted, e.g. $MX12$. The address bits of the IOT instruction (bits 4,5,12,13) are gated into a flip-flop register, the output of which goes to the multiplexer address circuitry via line drivers. The A/D convert signal is delayed from the loading of the multiplexer address so that the addressing and the convert signals originate from one instruction and require only one machine cycle (1.75 μ sec) for execution.

Method II

Repetitive or sequential multiplexer mode is chosen using instructions MXRP or MXSE respectively, and then the conversion

is made using the instruction A/D Convert (ADCV). If repetitive mode is chosen, the multiplexer will convert the same channel each time the ADCV instruction is executed. If sequential mode is chosen the multiplexer will advance one channel before the ADCV instruction is executed.

When the PDP-7 commands the A/D converter to convert, it takes the multiplexer 8 μ sec to settle, and the A/D converter 4 μ sec to convert. Since 12 μ sec is not enough time for the PDP-7 to jump out and execute other operations while waiting for the A/D conversion to be completed, the program calls for a flag check using the instruction A/D SKIP FLAG (ADSF), and waits until the conversion is complete. The convert instruction initiates the Busy flag by means of a delay which covers the duration of both the multiplexer settling time and the Busy signal from the A/D converter. This composite Busy signal is wired to the PDP-7 Skip facility where it functions as a flag.

Digital-to-Analog Conversion Routine

The procedure used to effect a D/A conversion is very simple. The signed one's complement binary data word to be converted is loaded into the accumulator of the PDP-7. The instruction DA β , where β is the channel number (0-23), is then executed. This instruction is microcoded to specify the D/A channel address and initiate a convert command. The D/A Distributor decodes the address word and provides the gating required to send the digital data to the correct D/A converter. The DA β instruction utilizes the PDP-7 slow cycle which requires 3.36 μ sec for execution. If all D/A channels are to be set to the same output voltage (e.g. for initial condition), the accumulator would be loaded with the digital data word; then the instructions DA0, DA1, ... DA β , where β is the last channel to be used, would be executed in sequence.

Automatic Priority Interrupt Service Routines

There are three interrupt modes in the PDP-7 having the following priority:

1. Data Break (used for magnetic drum data transfers)
2. Automatic Priority Interrupt
3. Program Interrupt Control

The Data Break (DB) facility allows the magnetic drum memory to operate independently of the computer program (after a short initializing sequence). It transfers data with core memory at drum-determined times on a cycle-stealing basis. A data break request is granted at the completion of the current instruction (within three machine cycles, maximum). The program is suspended for one cycle while the data is transferred between the drum and the memory buffer register; then the program is resumed.

The Program Interrupt Control (PIC) facility allows the control of input/output operations without the necessity of constantly monitoring program flags. When the PIC is enabled (under program control), and a peripheral device becomes available, the PIC automatically interrupts the program sequence and causes a program interrupt break to occur. A subroutine beginning at the break location may then search program flags to determine which device caused the interrupt. After the device is serviced, the control returns to the main program.

The Automatic Priority Interrupt (API) facility of the PDP-7 identifies an interrupting device directly without the need for flag searching. Multilevel interrupts are permissible where a device on a channel having higher priority supersedes an interrupt already in process. These functions increase the speed and efficiency of the input/output system and simplify programming.

The PDP-7 contains 16 automatic interrupt channels arranged in a priority chain so that channel 0 has the highest priority and channel 17₈ has the lowest priority. Each channel is assigned a unique, fixed, memory location in the range of 40₈ through 57₈ beginning with channel 0. When establishing priority, each I/O device is assigned a unique interrupt channel (See Appendix H). The priority chain guarantees that if two or more I/O devices request an interrupt concurrently, the system grants the interrupt to the device with the highest priority. The other interrupt requests will be serviced afterward in priority order. In general, the faster devices are assigned to higher priority channels, and the slower devices, to lower priority channels.

The priority interrupt system operates in either the multi-instruction subroutine mode or the single-instruction subroutine mode. The mode is determined by the instruction in the memory location assigned to the channel.

The Multi-Instruction Subroutine Mode

This mode is generally used to service an I/O device that requires control information from the PDP-7. Such devices in the hybrid system include the servo and interface relay flags, the A/D converter (overload), and other slow electromechanical devices such as the teleprinter, card reader, and high speed paper tape reader and punch. Each device requires a servicing subroutine that includes instructions to manipulate data and give further instructions, such as continue, halt, etc., to the interrupting device.

An interrupt request from a device is granted if the following conditions are met:

1. The API is in the enabled condition by program control.
2. There is no data break request present.
3. The requesting channel is in the enabled condition by program control.

4. There is no interrupt in progress on a channel of higher priority.
5. There is no interrupt in progress on the requesting channel.
6. Neither of the instructions CAS nor JMS is being executed.
7. None of the IOT or EAE instructions is being executed.

When an interrupt is granted, the content of the channel memory location is transferred to the memory buffer and executed. If the instruction executed is Jump Subroutine Y (JMS Y), the system operates in the multi-instruction subroutine mode. The interrupt flag of the device is lowered when the service routine is entered. An example illustrating the multi-instruction subroutine mode is given in Appendix I.

The Single Instruction Subroutine Mode

In some instances, it is desirable for the PDP-7 to receive information from an external device but not desirable to send control information to the device. Such an application would be the counting of clock pulses to determine elapsed time. The single instruction subroutine mode simplifies programming a counter. It is entered if the channel memory location does not contain a Jump to Subroutine Y (JMS Y) instruction. Normally the instruction is Increment and Skip (ISZ), however, others may be used. In any case, the single instruction constitutes the entire subroutine, and the interrupt system automatically clears the interrupt flag, debreaks the interrupting channel, and returns the channel to the receptive condition. An example illustrating the single instruction subroutine mode is given in Appendix I. An example showing how the clock may be used to initiate a periodic A/D conversion is given in Appendix J.

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APPENDICES

APPENDIX A

DYNAMICS MODEL 601 MV FLOATING DIGITAL DRIVER

The Model 601 MV Floating Digital Driver is a digital component that provides digital-to-digital isolation between the analog computer ground and the digital computer ground.

Specifications

Negative true input:	"0" = 0 V "1" = -6 V
Negative true output:	"0" = 0 V "1" = -6 V
Output logic current	"0" = 120 mA
Frequency range	dc to 500 kHz
Rise time	"1" = 800 nsec maximum "0" = 900 nsec maximum
Common-mode voltage	300 V maximum
Input/output isolation	Infinite resistive 5 pF capacitive
Supply voltages	Input -12 V Output +12 V -6.5 V

APPENDIX B

INPUT/OUTPUT TRANSFER INSTRUCTIONS

Input/Output Transfer (IOT) instructions are used to control peripheral devices, to sense their status, and to transfer information between them and the processor. Three instructions initiate generation of time-sequenced IOT pulses and a device-select code, both of which are applied to the device selector interface circuits. Upon receipt of these signals, the device selector generates input/output pulses (IOP's) that effect the operations specified by the IOT instruction. The three event times of the IOT instruction are identified with an IOP. The generation of the IOP's is determined by the content of bits 15, 16, and 17 of the IOT instruction. IOP1 is used to check the status of a device. IOP2 and IOP4 are normally used to cause a transfer of information to and from the information collector and the information distributor. The relationship between pulses, event times, and instruction bits is as follows:

<u>Instruction Bit</u>	<u>IOT Pulse</u>	<u>Processor Time</u>	<u>Event Time</u>
17	IOP1	T5	1
16	IOP2	T7	2
15	IOP4	T1 of next cycle	3

The IOT instruction format is shown below in Figure B-1. Bits 0-3 carry the IOT instruction code (70); bits 6-11 determine the external device selected; bits 4-5 and 12-13 are used to select a subdevice or microcoding, and bits 15-17 initiate transmission of electrical pulses to the device for direct control of the information transfer or device operation.

FIGURE B-1. IOT Instruction Bit Assignments

The PDP-7 Device Selector is diagrammed in Figure B-2.

FIGURE B-2. PDP-7 Device Selector

APPENDIX C

HYBRID COMPUTER INTERFACE SCHEMATICS

H-11-2167	Linkage System and Block Diagram
H-11-2168	Cable Interconnection Diagram
H-11-2169	Module Map
H-11-2170	Analog Computer Address Control
H-11-2171	Automatic Hybrid Pot Set Coefficient
H-11-2172	DVM Control & Readback
H-11-2173	Mode Control, Set Lines, & Program Interrupt Lines
H-11-2174	Sense & Program Interrupt Lines
H-11-2175	Relay Flag and Automatic Address Clear
H-11-2176	Controls of Analog Computer
H-11-2177	Analog-to-Digital Converter Control Interface
H-11-2178	Digital-to-Analog Converter Control Interface
	Hybrid Interface Cable Manual (No File No.)

APPENDIX D

BINARY-TO-VOLTAGE CONVERSION

Data Word is 13 Bits Plus Sign* One's Complement Binary

* $2^{13} = 8192$ Therefore Resolution = $1/8192$ or 12.207 Millivolts

OCTAL--BINARY--VOLTAGE CONVERSION

<u>Octal No.</u>	<u>Binary No.</u>	<u>Voltage</u>
00000	0 000 000 000 000	0.0
00001	0 000 000 000 001	0.0122
00002	0 000 000 000 010	0.0244
00003	0 000 000 000 011	0.0366
00004	0 000 000 000 100	0.0488
00005	0 000 000 000 101	0.0610
00006	0 000 000 000 110	0.0732
00007	0 000 000 000 111	0.0854
00010	0 000 000 001 000	0.0977
00020	0 000 000 010 000	0.1953
00030	0 000 000 011 000	0.2930
00040	0 000 000 100 000	0.3906
00050	0 000 000 101 000	0.4883
00060	0 000 000 110 000	0.5859
00070	0 000 000 111 000	0.6836
00100	0 000 001 000 000	0.7812
00200	0 000 010 000 000	1.5625
00300	0 000 011 000 000	2.3437
00400	0 000 100 000 000	3.1250
00500	0 000 101 000 000	3.9062
00600	0 000 110 000 000	4.6875
00700	0 000 111 000 000	5.4687
01000	0 001 000 000 000	6.25
02000	0 010 000 000 000	12.5
03000	0 011 000 000 000	18.75
04000	0 100 000 000 000	25.0
05000	0 101 000 000 000	31.25
06000	0 110 000 000 000	37.5
07000	0 111 000 000 000	43.75
10000	1 000 000 000 000	50.0
07777	0 111 111 111 111	49.9878
17777	1 111 111 111 111	99.9878

APPENDIX E-1 HYBRID INSTRUCTIONS

Mnemonic	Code	Function	Operation Executed	Cycles
SBSF	702001	MODE	SKIP IF STANDBY FLAG IS SET	1
SDBY	702004	MODE	SELECT STANDBY MODE	1
ICSF	705001	MODE	SKIP IF IC MODE IS SET	1
IC	705004	MODE	SELECT IC MODE	1
HDSF	705101	MODE	SKIP IF HOLD MODE IS SET	1
HOLD	705104	MODE	SELECT HOLD MODE	1
CSF	705201	MODE	SKIP IF COMPUTE MODE IS SET	1
COMP	705204	MODE	SELECT COMPUTE MODE	1
PTSF	705301	MODE	SKIP IF POT SET MODE IS SET	1
PSET	705304	MODE	SELECT POT SET MODE	1
SVSF	701501	SERVO	SKIP IF SERVO FLAG IS SET	1
SERV	701504	SERVO	POT SERVO OPERATE	1
AALD*	705002	ADDRESS	LOAD ADDRESS BUFFER REGISTER	1
RYSF*	701401	ADDRESS	SKIP IF ADDRESS FLAG = 1	1
		POT COEF	SKIP IF POT COEF FLAG = 1	1
		DVM RDBK	SKIP IF DVM RDBK FLAG = 1	1
PCLD*	705102	POT COEF	LOAD POT COEF BUFFER REGISTER	1
DVMR	701404	DVM RDBK	DVM READ AND LOAD BUFFER REGISTER	1
DVML	701402	DVM RDBK	LOAD DVM BUFFER REG INTO AC	1
MIST	705302	MOD INST	SET MOD INSTRUCTION FF	1
MICL	705202	MOD INST	CLEAR MOD INSTRUCTION FF	1
SET1	702104	DLS	DLS SET LINE 1	1
SET2	704504	DLS	DLS SET LINE 2	1
SET3	704602	DLS	DLS SET LINE 3	1
SET4	704604	DLS	DLS SET LINE 4	1
SEN1	702101	DLS	SKIP IF SENSE LINE 1 IS SET	1
SEN2	704501	DLS	SKIP IF SENSE LINE 2 IS SET	1
SEN3	704601	DLS	SKIP IF SENSE LINE 3 IS SET	1
SEN4	70XX01	DLS	SKIP IF SENSE LINE 4 IS SET	1

* Address is auto load.

Pot coefficient (COEF) is auto load.

Relay flag serves address, DVM readback, and pot set coefficient, i.e., its action will be integrating; several operations may be done while waiting for the relay flag to be set.

APPENDIX E-2 HYBRID INSTRUCTIONS

Mnemonic	Code	Function	Operation Executed	Cycles
MXRN	701101	MUX	RANDOMLY SELECT MUX CHANNEL	1
MXRP	701104	MUX	REPETITIVELY SELECT MUX CHANNEL	1
MXSE	701102	MUX	SEQUENTIALLY SELECT MUX CHANNEL	1
ADOV	701201	ADC	SKIP IF OVERLOAD FLAG IS SET	1
ADSF	701301	ADC	SKIP IF A/D FLAG IS SET	1
ADCV	701304	ADC	CONVERT	1
ADRB	701312	ADC	READ IN A/D OUTPUT REGISTER	1
MX0	701202	MUX	LOAD ADDRESS 0 INTO MUX AND CONVERT	1
MX1	701222	MUX	1	1
MX2	701242	MUX	2	1
MX3	701262	MUX	3	1
MX4	711202	MUX	4	1
MX5	711222	MUX	5	1
MX6	711242	MUX	6	1
MX7	711262	MUX	7	1
MX8	721202	MUX	8	1
MX9	721222	MUX	9	1
MX10	721242	MUX	10	1
MX11	721262	MUX	11	1
MX12	731202	MUX	12	1
MX13	731222	MUX	13	1
MX14	731242	MUX	14	1
MX15	731262	MUX	15	1
MX16	704502	MUX	16	1
MX17	704522	MUX	17	1
MX18	704542	MUX	18	1
MX19	704562	MUX	19	1
MX20	714502	MUX	20	1
MX21	714522	MUX	21	1
MX22	714542	MUX	22	1
MX23	714562	MUX	23	1

APPENDIX E-3 HYBRID INSTRUCTIONS

Mnemonic	Code	Function	Operation Executed	Cycles (Slow Cycle = 3.36 μ sec)
DA0	702002	DAC	SELECT D/A CHANNEL 0 AND CONVERT	1
DA1	702022	DAC	1	1
DA2	702042	DAC	2	1
DA3	702062	DAC	3	1
DA4	712002	DAC	4	1
DA5	712022	DAC	5	1
DA6	712042	DAC	6	1
DA7	712062	DAC	7	1
DA8	722002	DAC	8	1
DA9	722022	DAC	9	1
DA10	722042	DAC	10	1
DA11	722062	DAC	11	1
DA12	732002	DAC	12	1
DA13	732022	DAC	13	1
DA14	732042	DAC	14	1
DA15	732062	DAC	15	1
DA16	702102	DAC	16	1
DA17	702122	DAC	17	1
DA18	702142	DAC	18	1
DA19	702162	DAC	19	1
DA20	712102	DAC	20	1
DA21	712122	DAC	21	1
DA22	712142	DAC	22	1
DA23	712162	DAC	23	1

APPENDIX F

HYBRID CONTROL SUBROUTINES

SELECT AN ANALOG ADDRESS FROM THE PDP-7

LAC ADDRESS /LOAD ACC WITH BCD VALUE OF ANALOG ADDRESS
/TO BE SELECTED
AALD /LOAD ADDRESS BUFFER REGISTER AND SELECT ADDRESS
RYSF /SKIP IF ADDRESS FLAG = 1 (TAKES 9 MILLISECONDS)
JMP .-1 /WAIT FOR FLAG TO SET
CONTINUE /AT THIS POINT THE 2133 WILL REMAIN ADDRESSED
/BY THE PDP-7 FOR 3 SECONDS. UNLESS READDRESSED
/WITHIN 20 MILLISECONDS, THE INTERFACE CIRCUIT
/TIMES OUT AFTER 3 SECONDS, AND THE ANALOG COMPUTER
/ADDRESSING CONTROLS ARE ENABLED.

SET THE HYBRID POT COEFFICIENT REFERENCE DIVIDER

LAC /LOAD ACC WITH 1248 BCD VALUE OF COEFFICIENT
PCLD /LOAD POT COEFFICIENT BUFFER REGISTER AND
/SELECT HYBRID COEFFICIENT
RYSF /SKIP IF ADDRESS FLAG = 1 (TAKES 9 MILLISECONDS)
JMP .-1 /WAIT FOR FLAG TO SET
CONTINUE /AT THIS POINT A POT WOULD NORMALLY BE SET.
/THE HYBRID REFERENCE DIVIDER WILL KEEP THE LAST
/VALUE THAT WAS SET ON THE POT COEF BUFFER REGISTER.

READ AN ANALOG VALUE INTO THE PDP-7 USING THE DVM

LAC /LOAD ACC WITH BCD VALUE OF POINT TO BE ADDRESSED
AALD /LOAD ADDRESS BUFFER REGISTER AND SELECT
DVMR /DVM READ AND LOAD BUFFER REGISTER
RYSF /SKIP IF DVM READBACK FLAG = 1
JMP .-1 /WAIT FOR FLAG TO SET
CLA /CLEAR THE ACCUMULATOR
DVML /LOAD DVM BUFFER REGISTER INTO THE ACC
CONTINUE

SET A POT

PSET /SELECT POT SET MODE
PTSF /SKIP IF POT SET MODE IS SET
JMP .-1 /WAIT FOR POT SET FLAG TO SET
LAC ADD 1 /LOAD ACC WITH BCD VALUE OF ANALOG ADDRESS
/(P MUST BE SELECTED)


```
AALD          /SELECT ADDRESS ON 2133
LAC COEF 1    /LOAD ACC WITH BCD VALUE OF POT COEFFICIENT
PCLD          /LOAD POT COEF BUFFER REGISTER AND SELECT COEF
RYSF          /SKIP IF RELAY FLAG = 1
JMP .-1       /WAIT FOR FLAG TO SET
SERV          /SERVO OPERATE
SVSF          /SKIP IF SERVO FLAG = 1 (TAKES 2.5 SECONDS)
JMP .-1       /WAIT FOR SERVO COMPLETION
CONTINUE
```

APPENDIX G

ANALOG-TO-DIGITAL CONVERSION SUBROUTINES

RANDOMLY SELECT AND CONVERT MUX CHANNEL 3

```
MXRN      /RANDOMLY SELECT (USED ONCE TO INITIALIZE)
MX3       /ADDRESS AND CONVERT MUX CHANNEL 3
ADSF      /SKIP IF A/D FLAG IS SET
JMP .-1   /WAIT FOR CONVERSION COMPLETION
ADRB      /READ A/D OUTPUT REGISTER INTO ACCUMULATOR
```

REPETITIVELY SELECT AND CONVERT MUX CHANNEL 7

```
MXRN      /RANDOMLY SELECT
MX7       /ADDRESS MUX CHANNEL 7 AND CONVERT
MXRP      /REPETITIVELY SELECT
```

FOLLOWING THIS SERIES OF COMMANDS, AND UNTIL A NEW SELECT MODE IS ENTERED, THE FOLLOWING COMMANDS WILL CONVERT CHANNEL 7 AND ENTER IT INTO THE ACCUMULATOR.

```
ADCV      /CONVERT
ADSF      /SKIP IF A/D FLAG IS SET
JMP .-1   /WAIT FOR CONVERSION COMPLETION
ADRB      /READ ADC OUTPUT REGISTER INTO ACCUMULATOR
```

SEQUENTIALLY SELECT AND CONVERT MUX CHANNELS

```
MXRN      /RANDOMLY SELECT
MX23      /ADDRESS MUX CHANNEL 23 IF DESIRED
           /STARTING LOCATION IS CHANNEL 0
ADSF      /SKIP IF A/D FLAG IS SET
JMP .-1   /WAIT FOR CONVERSION COMPLETION
MXSE      /SEQUENTIALLY SELECT
```

FOLLOWING THIS SERIES OF COMMANDS, AND UNTIL A NEW SELECT MODE IS ENTERED, THE FOLLOWING COMMANDS WILL ADDRESS AND CONVERT THE NEXT CHANNEL IN SEQUENCE. THE RESULT WILL BE ENTERED INTO THE ACCUMULATOR. THE ADDRESS IN THE SEQUENCE FOLLOWING 23 BEING 0.

```
ADCV      /CONVERT A/D
ADSF      /SKIP IF FLAG IS SET
JMP .-1   /WAIT FOR CONVERSION COMPLETION
ADRB      /READ A/D OUTPUT REGISTER INTO ACCUMULATOR
```

APPENDIX H

API CHANNEL FLAG ASSIGNMENTS

<u>API Channel</u>	<u>AC BIT</u>	<u>Speed (max)</u>	<u>Flag</u>	<u>Memory Location</u>
0	2	50 kHz	DRUM (DRDN)	40
1	3	5 kHz	CLOCK 1	41
2	4	5 kHz	CLOCK 2	42
3	5	5 kHz	DECTAPE (MMDF) (MMBF) (MMEF) } OR GATE	43
4	6	85 kHz	A/D OVERLOAD (ADOV)	44
5	7	VARIABLE	DLS PI 1	45
6	8	300 Hz	PT READER (RSF)	46
7	9	63.3 Hz	PT PUNCH (PSF)	47
10	10	5 kHz	CLK OVERFLOW	50
11	11	10 Hz	TTY PRINT (TSF)	51
12	12	10 Hz	TTY READ (KSF)	52
13	13	VARIABLE	DLS PI 2	53
14	14	VARIABLE	PLS PI 3	54
15	15	2 Hz	CARD READER (CRSF) (CBSF) (CRDN) } OR GATE	55
16	16	50 Hz	INTERFACE RELAY (RYSF)	56
17	17	20 CPM	SERVO (SVSF)	57

APPENDIX I

API SERVICING SUBROUTINES

<u>Memory Location</u>	<u>Instruction</u>	<u>Operation</u>
<u>Single Instruction Subroutine Mode</u>		
1200	DAC 1600	Operation being executed when interrupt occurs.
0046	ISZ 3200	Instruction executed as a result of break on channel 06. If overflow, flag is set, PC not changed.
1201	LAC 1620	Next instruction in sequence of main program.
<u>Multi-Instruction Subroutine Mode</u>		
1000	ADD 2650	Instruction being executed when interrupt request occurs.
0043	JMS 3000	Instruction executed as a result of interrupt on channel 03. The JMS determines multi-instruction mode.
3000	--	The link and the PC are stored in location 3000.
3001	DAC 3050	First instruction of servicing routines stores AC.
3002	--	Instructions servicing the interrupting in/out device.
3003	--	
3004	--	
3005	--	
3006	--	
3007	LAC 3050	Restores AC for main program.
3010	DBR	Debreaking IOT releases channel.
3011	JMP I 3000	Return to main program sequence.
1001	--	Next instruction executed from here unless another priority interrupt is waiting.

APPENDIX J

PERIODIC A/D CONVERSION OF CHANNEL 14USING THE API AND 5 kHz CLOCK

<u>Memory Location</u>	<u>Instruction</u>	<u>Operation</u>
41	ISZ 4000	Instruction executed as a result of a break on API Channel 1 which is a 5 kHz clock. Each time the 5 kHz clock pulses, this instruction will be executed.
100	LAC (777755	Load AC with initial clock count value so that an overflow occurs every 3.8 msec.
101	DAC 4000	Deposit initial value in clock location 4000.
102	CAC	Clear all API Channels.
103	LAC (040200	Load AC with API Channels to be enabled.
104	ASC	Enable selected channels.
105	EPI	Enable API.
106	Continue	
--	--	
--	--	
301	--	Instruction being executed when clock location 4000 overflows.
50	JMS 600	Instruction executed as a result of clock overflow on API channel 10.
600	0	The link and the PC are stored in location 600.
601	DAC 4050	Save AC in location 4050.
602	LACQ	Load AC with contents of MQ.
603	DAC 4051	Save MQ in location 4051.
604	MX14	Convert MX channel 14 from analog voltage to digital word.
605	ADSF	Skip if A/D converter flag is set.
606	JMP .-1	Jump back.
607	ADRB	Read A/D converter output register into the AC.

<u>Memory Location</u>	<u>Instruction</u>	<u>Operation</u>
610	DAC 6600	Deposit AC in memory location 6600.
611	LAC (777762	Reinitialize clock counter.
612	DAC 4000	Deposit initial value in clock location 4000
613	LAC 600	Load AC with Link and PC
614	RAL	Restore Link
615	LAC 4051	Load AC with contents of MQ before interrupt occurred.
616	LMQ	Restore MQ
617	LAC 4050	Restore AC with value it had before interrupt occurred.
620	DBR	Debreak
621	JMP I 600	Return to main program sequence.
302	--	Next instruction in main program executed.

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