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THE LASL TANDEM ACCELERATOR FACILITY DATA SYSTEM*

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SUMMARY

An on-line data processing system has recently been placed in operation in conjunction with two electrostatic accelerators at the Los Alamos Scientific Laboratory. The system consists of a Scientific Data Systems Model 930 computer and an experiment-computer interface unit designed and fabricated at LASL. The system provides for time-shared operation of three separate experiments. Up to nine fast analog-to-digital converters may be utilized by these three experiments. These ADCs may be connected and fanned-in to the computer in a variety of ways ranging from nine simultaneously operating separate devices to a combination for a nine parameter coincidence experiment.

The system design places considerable emphasis upon rapid set-up to facilitate change from one experiment to another. Provision has been made for computer control of experimental apparatus, and for data input to the computer from other sources such as scalers, clocks and

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voltmeters. The interface portion of the system has been implemented entirely with integrated circuits and is modular to the extent that future expansion can easily be accomplished.

Introduction

The use of general purpose digital computers for real-time data acquisition and reduction in the physics laboratory has been well covered in the literature.¹⁻⁴ The emergence of ever faster, more versatile computers at constantly decreasing prices has made the competitiveness of this approach as opposed to conventional equipment increasingly obvious.

The outstanding feature of a computer-based system as opposed to conventional analyzers is its versatility. This paper will describe the Los Alamos Tandem Accelerator Facility Data System (LATAFDS) and the features that have been incorporated to allow flexibility of experimental configuration, and facilitate communication and control.

A brief description of the Los Alamos Tandem Accelerator Facility (LATAF) is in order to better define the data system requirements. The LATAF consists of an 8 MeV vertical electrostatic accelerator and a 15 MeV tandem Van de Graaff accelerator. These two can be used together as a single 23 MeV accelerator or they can be used as two separate sources of accelerated particles, each requiring its own experimental facilities. If equipment for the set-up of experiments is included, at least three separate data handling facilities are required. These installations must provide for rapid change from one experiment to another in order to best serve the large number of physicists using the accelerators. It was our opinion that a computer operating in a time-shared mode could accomplish these requirements at a reasonable cost and provide additional capability as a bonus.

We have been engaged since mid-1963 in various aspects of the system specifications and design. Our first task was that of specifying and purchasing a computer. The desirable characteristics of a computer for this application have been described⁵, and will not be covered in this paper. There are several computers that meet these requirements and that

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would serve well in the real-time data acquisition and reduction field. We chose the Scientific Data Systems Model 930. Others would be equally applicable.

The next element of the system that needed to be specified and acquired was the Analog-to-Digital Converters (ADC). The requirements dictated by the proposed experiments were a resolution of 4096 channels, a differential linearity of 1% and a conversion time of approximately 10 microseconds. To the best of our knowledge no such unit is commercially available. It is likely that a unit approaching these specifications will become available within the lifetime of the system. The design was completed with this in mind. To place the system in operation we have acquired a very satisfactory interim ADC. It is a Victoreen Model S16ADC-2 P-A with 2048 channel resolution, a differential linearity of $\pm 1\%$ and a conversion time of $0.125 \mu\text{s}/\text{channel} + 8 \mu\text{s}$. Three of these units containing two ADCs each are presently incorporated in the system.

The selection of amplifiers, linear gates, coincidence units, etc., is not considered a part of the data system and is left to the individual experimenter.

The operation of general purpose digital computers is well understood, as is the operation of the various digitizers used in the physics laboratory (ADC, time encoders, scalers, etc). This report, therefore, will be concerned with the method of interconnecting the various digitizers, with the processing of the digitized data prior to its input to the computer, and with the routing of the data into the computer.

System Description

Before starting the main description we should emphasize one aspect of the computer which is of fundamental importance to time-share operation. This is the computer priority interrupt system. This system allows an external device such as an ADC to request the attention of the

computer and, if the interrupt request has been assigned a higher priority than the program then in progress, to force the computer to temporarily put aside that program and to service the interrupt request. The computer has the ability to impose a predetermined order on its recognition of simultaneously occurring interrupt requests and it will proceed with the processing of those requests in that order.

Figure 1 shows the front panel of the computer-experiment interface unit. The left hand rack contains the Victoreen ADCs. The center rack contains three identical Experiment Control Panels. One of these is shown in detail in Fig. 2. The right hand rack contains nine sets of twelve digital comparison switches on the upper panel and a cable patch panel below. These panels will be described in detail later.

A simplified block diagram of the system, which emphasizes the input-output, is shown in Fig. 3. The real time data inputs should be particularly noted. These include 9 fast analog inputs, 16 digital inputs of 24 bits each, 108 single condition sampling inputs, 32 interrupt lines, and a cathode ray tube light pen. In addition, the conventional computer inputs are available for program input or for input of non-real-time data. The outputs are the conventional computer output devices, as well as 220 individual control lines which can be actuated by the computer program. These lines may be used to control various experimental devices (typically, to set binaries, actuate relays or stepping motors, turn valves ON or OFF, etc.). Some of these lines may be used in the future for closed loop control of the accelerator.

It will be noted from Fig. 3 that nine fast pulse ADCs are provided. These may be grouped in a variety of ways for different experimental configurations. To set up an experiment on the LATAFDS one of the three identical Experiment Control Panels is selected by the experimenter. Any of the ADCs that are not in use by the other two experiments may be used and are selected by switches on this panel. The selection of an ADC on one control panel prohibits its use on either of the other two. The lower of

the two switches shown in Fig. 2 will be discussed later. The upper row of switches labeled "Finish Combinations" determines the way that the Finish-Analysis signals from the selected ADCs will be combined. The Finish-Analysis signal originates in an ADC and indicates that the particular ADC has completed the analysis of a pulse. The ADC, having completed an analysis, will wait until the system accepts its data and sends a signal back to the ADC instructing it to accept the next input pulse. It was necessary to modify the Victoreen ADCs slightly to achieve this type of operation. In coincidence work the Finish Analysis signals would be ANDed to insure that all of the ADCs involved in the experiment had completed their analysis before a signal, requesting input, was sent to the computer. Other conditions may be desirable for particular experimental configurations. Each of the three experiment controls contains two nine-term AND gates and an eleven term OR gate for making these combinations. This gating structure is shown in Fig. 4a.

When the finish conditions set up by the experimenter have been satisfied, a request for computer action is sent to the interrupt system of the computer. All interrupt requests are routed through a 64 x 64 matrix pin board which is located on the rear of the interface unit and is not shown in the accompanying figures. These requests may be from the Experiment Control Panels or from sources which will be described later. A matrix pin board consists of two separate planes containing continuous contact strips running at 90° to each other. Insertion of a pin at a given intersection connects a strip on the vertical axis with another on the horizontal axis. In the LATAFDS the computer interrupt lines are connected to the vertical busses and the interrupt request lines are connected to the horizontal busses. By inserting appropriate pins a given request can be connected to any one of the interrupt lines. Since each of these interrupts has a fixed rank in the computer priority structure, the matrix pin board provides a flexible means of assigning priorities among the requests.

The data bits from the ADCs follow three routes. Two of these are to the computer and will be described under "Modes of Operation." The third route is to a set of twelve comparison switches, shown in Fig. 5. The three positions of each switch are 1, 0, and ignore (X on the panel.) The comparison circuits compare each bit from a given ADC with the setting of the corresponding switch. The results are ANDed in a 12-term AND gate. An output from this gate will result only if the ADC bit pattern corresponds with the switches. By appropriately setting the switches the experimenter can define an area of interest in the output of a given ADC. By combining the comparisons resulting from several ADCs, the boundaries of a multi-dimensional subset of the total data from a large multi-parameter experiment may be defined. In many cases the entire set would be too extensive for a real-time analysis. The purpose of the comparison circuits is to allow a real-time analysis of this subset simultaneously with the event recording of the entire set of data. The method in which the comparison signals may be combined is determined by the lower set of switches in Fig. 2, entitled "Compare Combinations". The logic diagram of this is shown in Fig. 4b. It is seen that the combinations logic is similar to that employed for the Finish-Analysis signals.

Modes of Operation

The experimenter may select one of four modes of operation by means of a switch located on each Experiment Control Panel. The "Raw Data" position is an "event recording" mode. In this mode an interrupt line to the computer is actuated when the conditions imposed by the "Finish Combination" switches have been satisfied. The computer response to this is to input the data from one or more ADCs employed. The computer may now perform various operations on this data. For "event recording" a block of address (events) is formed in memory. When this block has been filled it is transferred to IBM compatible magnetic tape via a buffered input-output channel. While

this transfer is taking place the computer can fill another block of memory with incoming events. The two blocks then alternate between filling and dumping. The maximum event rate for this mode is limited by the capability of the magnetic tape.

The second mode of operation is denoted "Analyze Only". In this mode the data from each ADC is compared with a set of comparison switches as described earlier. In addition to being routed to the comparison switches, the data bits from an ADC are also routed to twelve of the fifty vertical busses on a 50 x 14 pin board matrix which is located on the Experiment Control Panels. Four ADCs may be routed to this matrix board. They are chosen by the experimenter by making appropriate connections on the Cable Patch Panel. The remaining two vertical busses are wired to voltages corresponding to 1 and 0 logic levels.

The bits that will appear on the fourteen horizontal busses are selected by the insertion of pins in the matrix board. These fourteen bits are used to address the computer's 16K memory (12K at present.) It is intended that the normal analysis will be no more than 4K channels. In this case twelve bits are selected from the 48 ADC bits and the remaining two are used to select the block in memory in which the 4K channels are to be located. The resulting 14 bits is called the "composite word" and is used as the address for a real-time multiparameter analysis. This analysis is performed by computer hardware in the following manner. As an option, the SDS 930 computer may be equipped with a direct route to memory which has priority over the computer itself regarding memory accesses. This device

is called the Data Multiplex Channel (DMC). It also incorporates an automatic incrementing feature. When an increment request is presented to the DMC along with an address, the word located at the specified address is fetched, incremented by one, and restored at the original location. Thus with the DMC the computer serves as a conventional analyzer. The requests for increment to the DMC from the Experiment Control Panels are controlled by a priority scheme. Thus all three Experiment Control Panels may be set to the "Analyze Only" mode and be engaged in an analysis through the DMC with each one having its own section of memory.

The action of the comparison circuits in the "Analyze Only" mode is as follows. If all of the ADC's outputs fall within the areas defined for them by the experimenter and if their combination satisfies the imposed conditions, then the request for increment proceeds as outlined above. If the conditions are not met, the increment request will still be sent to the DMC, but it will be accompanied by a special address utilized by the experiment to keep count of the rejected events. Including logic and comparison delays, the maximum rate in the "Analyze Only" mode is about 100 Kc, exclusive of the ADC conversion times.

The third mode of operation is a combination of the first two. In this mode a real-time analysis may be made on a subset of data while an event recording of all data is made on magnetic tape. All of the previously described features of the "Raw Data" and "Analyze Only" modes apply to this mode. It is particularly applicable to multi-parameter experiments, where the total data is too extensive for a real-time analysis. By doing a real-time

analysis of a subset of the data, the experimenter can keep track of the progress of the experiment and make such changes of experimental parameters as seem appropriate from the observations of the analyzed portions of the data.

The last mode of operation is the "Analyze Tape" mode. This is a natural extension of the mode last described. In the last mode it is noted that all data is recorded on tape while only a subset is analyzed. In the "Analyze Tape" mode the magnetic tape containing all of the data is played back through the computer and then routed through the interface until the data appear in the same ADC buffer register through which it was routed during the original data acquisition. The data now is returned to the computer via the same route as would be followed in the "Analyze Only" mode. The experimenter may set the comparison switches so that the analysis covers a different region of interest than was covered during the original data acquisition. Successive passes will allow an analysis of all of the data, should this prove desirable. This mode of operation proceeds at a rate that is limited only by the magnetic tape. Since only two tape decks are presently available, only two Experiment Control Panels can be set to time-share the "Analyze Tape" mode. The addition of another tape deck would allow three "Analyze Tape" operations to proceed concurrently.

Additional Features

The basic modes of operation have been described. A brief mention of some of the ancillary features will suffice to complete the outline of the system.

Each Experimental Control Panel has associated with it a bistable circuit with a large output driving capability. This bistable is called the Master Experiment Inhibit-Allow Flip Flop. It may be controlled by the computer, by a switch on the Experiment Control Panel, or by external equipment. Its function is to provide control signals to the external apparatus, such as ADCs, scalars, etc., which will allow the synchronization of all data-taking equipment for a given experiment. In addition to the Master Experiment Inhibit-Allow circuits, there are eighteen other similar bistables that may be used to control other functions that are not necessarily synchronized with the data taking. Switches are provided on the Cable Patch Panel to facilitate the routing of these signals to the external equipment.

As mentioned earlier, all interrupt requests are routed through a matrix pin board to the computer interrupt lines. The matrix pin board is a 64×64 array. At present, the computer contains 32 interrupts so 32 lines on the vertical axis are available for expansion. The request line busses are fully implemented. Twelve request lines are associated with the three Experimental Control Panels. Six of these are utilized by the logic involved with the various modes of operation. The other six are connected

to push button switches, two on each panel. These switches provide a means for manual control of the computer operation. The other 52 request lines are wired to connectors and are available to the experimenter for various uses. The matrix pin board allows insertion of pins containing components. The insertion of the pin causes the component to be placed in series with the two busses at the particular intersection. The circuits associated with the matrix board are constructed so that if pins containing diodes are used it is possible to OR two or more interrupt requests into one interrupt.

The 220 output control lines may be used in a variety of ways. As addressed by the computer, these lines provide a unique output of a $\sim 1 \mu s$ pulse. This can control external equipment or can be connected back into an interrupt request line to allow the computer program to initiate interrupts.

There are 108 lines provided for the interrogation of the state of external devices. Here a pulse is set out on a line that is specified by the computer program. Depending on the state of the external device, the pulse is returned or not returned. The computer then takes two courses of action depending upon the presence or absence of the returned pulse.

A very important capability of the system is that of reading in digital data from sources other than the pulse ADCs. This is accomplished by providing inputs for sixteen 24-bit words. These inputs are located on sixteen 61-pin connectors on the cable patch panel on the front of the interface unit. Twenty-four pins are assigned to the data inputs. Other functions such as interrupt inputs, inhibit-allow, test condition, and

control pulses, are also located on each connector. The data at a given connector is read into the computer by a pair of computer instructions. The first instruction specifies the desired input and the second instruction reads the data into computer memory. Typical inputs would be scalars, digital clocks, digital voltmeters, and slow ADCs. It is now felt that it will be necessary to increase the number of these auxiliary inputs in the near future. In particular, the number of scalars that will need to be read in has increased beyond our early expectations.

During the course of an experiment it is most important that the experimenter be able to observe the experimental data. A live display of the real-time analysis will be added to the LATAFDS in the near future. This will be in the form of a cathode ray tube display. It will provide plane, isometric, and contour displays on a 17" rectangular CRT. A light pen will be provided to facilitate man-machine communication. This unit is being fabricated at our laboratory.

Implementation of the Interface Unit

A system study was made to determine the lowest cost method of building the interface circuits. Several approaches were considered.

The use of commercially available logic modules appeared attractive from the viewpoint of requiring little engineering, however, the cost of these units is relatively high. The other extreme, design from the transistor level up, requires extensive engineering which is undesirable on a single unit,

non-production system such as this. An intermediate approach became feasible with the availability of inexpensive integrated circuit elements. With these, only one additional step is required over commercial modules, that is, the layout and placement of the elements on printed circuit boards. This can be accomplished with relative ease. Some of the boards for LATAFDS were fabricated by our own printed circuit facility while others were contracted. In either case the cost was quite reasonable.

Fairchild industrial grade micro-logic in TO-5 cans was used. The cans were placed on double-sided printed circuit cards that measure $5\frac{3}{4}$ " x 4", exclusive of connector. A typical board is shown in Fig. 6. An average of 24 cans are located on a card. This card size and resulting number of cans was chosen as a compromise between the very small single logic module approach that necessitates a large number of wire interconnections and the very large cards that limit flexibility and ease of expansion. The number of cans on a card varies so that, when possible, a card represents a meaningful block of logic in itself. As mentioned earlier, the fan-in gate structure will soon be expanded. This can be accomplished by the addition of the same gating cards that are presently used. Extra card locations are provided in various parts of the system to facilitate expansion.

The temperature range on the industrial micro-logic of + 15 to + 55°C is somewhat restrictive but has presented no problems in our laboratory environment. The LATAFDS utilizes approximately 4500 micrologic cans. There was no pre-testing of these elements. Five units were found to be defective

during initial check-out. Since that time there has been one failure and it occurred quite soon after the system was placed in operation. Insufficient time has elapsed to give meaningful reliability figures, but we are very encouraged by the results to date.

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RESULTS

The system is complete with the exception of the CRT display and some additions to the computer. It has been fully checked out. The unit has been, and is currently being, used for data accumulation and reduction in conjunction with the accelerators. Figure 7 shows the data from a recent experiment. This pulse height spectrum was produced by 15 Mev tritons scattered from Ni^{62} . The Xs indicate the experimental points and the Os show a least-squares fit of skewed Gaussian distributions to three of the peaks. The fitting was done in real time, as soon as data accumulation ended. The figure was produced on the incremental plotter on-line to the computer.

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We would like to thank James D. Gallagher of our Laboratory for his many contributions, particularly regarding the operation of the ADCs. Our appreciation is also extended to the several technicians whose excellent work has been obvious in the ease of check-out and excellent running experience.

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CAPTIONS

- Fig. 1 EXPERIMENT-COMPUTER INTERFACE UNIT
- Fig. 2 EXPERIMENT CONTROL PANEL
- Fig. 3 SIMPLIFIED BLOCK DIAGRAM EMPHASIZING INPUT-OUTPUT
- Fig. 4a LOGIC DIAGRAM SHOWING HOW "FINISH ANALYSIS" SIGNALS
4b FROM THE ADCS MAY BE COMBINED. b SHOWS A SIMILAR
 ARRANGEMENT FOR THE "COMPARE" SIGNALS.
- Fig. 5 COMPARISON SWITCH PANEL. TWELVE SWITCHES ARE PROVIDED
 FOR EACH OF THE NINE ADCS
- Fig. 6 TYPICAL PRINTED CIRCUIT CARD CONTAINING MICRO-LOGIC
 ELEMENTS
- Fig. 7 PULSE HEIGHT SPECTRUM PRODUCED BY 15-Mev TRITONS SCATTERED
 FROM Ni^{62} AND PLOTTED BY INCREMENTAL PLOTTER ON-LINE TO THE
 COMPUTER.

Fig 1

EXPERIMENT O CONTROL PANEL

Fig 3

Fig 5

Fig 6