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A SLOW TIME BASE READOUT SYSTEM
FOR NON-REPETITIVE PULSE ANALYSIS

MAY 17 1965 By
Carl E. Thomson

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A SLOW TIME BASE READOUT SYSTEM FOR
NON-REPETITIVE PULSE ANALYSIS

by

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CHAPTER I

INTRODUCTION

Waveform analysis of non-repetitive pulses possessing frequency components beyond the range of conventional laboratory recording devices (X-Y recorders, oscillographs, etc.) poses a problem. Oscilloscope analysis of such waveforms is difficult due to the non-recurring nature of the pulse. It is the purpose of this study to develop a system which will effectively "stretch" a single, fast pulse waveform (with duration in microseconds), to a slow time base (with the pulse waveform expanded to a duration of several seconds).

Time base expansion of a fast (microseconds duration), non-repetitive pulse is accomplished in this study by storing voltage amplitudes sampled at several points along the pulse duration. All sampling operations are performed at the time of pulse occurrence since the pulse is non-recurring. The stored voltage bits corresponding to the pulse waveform at the sampling points may then be "read out" at a much slower time rate. The output of the system is then a series of "spikes", each of about 3 milliseconds duration. The amplitude of each spike is the average of the amplitudes of the pulse waveform at a pair of consecutive sampling points. In order to record this output on a conventional X-Y recorder, a linear plotting device would be required which would sense amplitude differences between consecutive output spikes, and generate linear transitions between peak amplitudes of successive spikes

(the design of such a device was not undertaken in this study). The system developed in this study is capable of "stretching" a pulse of approximately one microsecond duration to a maximum expanded duration of ten seconds.

Currently, "Memo Scope" oscilloscopes are available which retain a waveform image on the cathode-ray tube face for an extended time, permitting analysis of the waveform. However, to retain the waveform indefinitely a photograph of the oscilloscope trace must be made. The slow time base readout system eliminates this operation in that a direct readout plot may be made.

A description of composite circuit operation, followed by individual circuit requirements, will first be undertaken. Following this, details of theory and design principles will be discussed. Then, experimental results and design modifications evolving from experimental evaluation will be presented. A final section will be devoted to conclusions and recommendations for further study.

CHAPTER II

DESCRIPTION OF CIRCUIT OPERATION

Composite Circuit Requirements

Analysis of fast pulse waveforms by means of sampling techniques first requires that the pulse waveform be divided into a number of equal, discrete time intervals (the degree of resolution obtainable in the final resultant waveform display is contingent upon the number of sampling intervals used). Figure 1 illustrates a pulse waveform divided into ten equal sampling increments. Each increment is shown designated as Δt , where T is the pulse width.

Energy from each sampling interval of the pulse waveform is integrated to obtain a voltage proportional to the average peak voltage of the pulse waveform during that sampling interval. This voltage is then amplified and retained in a storage capacitor for later readout. Each storage capacitor is charged to a voltage level proportional to the average input pulse amplitude during a particular sampling interval. Thus, a string of ten storage capacitors contains information defining the input pulse waveform at ten points.

The ten storage capacitors are then discharged consecutively through diode OR gates into an emitter follower output circuit. The rate at which the storage elements are triggered can be varied. This rate then determines the readout time base. An emitter follower output is used to provide a low impedance output to the readout device, while maintaining maximum pulse stretching by its high input impedance.

FIGURE 1

PULSE DIVIDED INTO SAMPLING INTERVALS

A block diagram of the circuitry comprising the sampling and expanded time base readout functions is given in Figure 2. It should be noted that only two complete channels are shown. Additional circuit blocks would be cascaded with those shown to increase the number of sampling output channels to any desired level. For the purposes of evaluating and verifying circuit operation in this study, two complete channels were assembled.

Operational Limitations

As is the case with most electronic apparatus, limits of normal operation must be specified. Design work and circuit evaluation undertaken in this study was performed within the two following limitations:

(1) input pulse amplitude shall not exceed 10 volts, and (2) input pulse duration shall be not greater than 1.0 microseconds. In addition, the triggering rate for capacitor storage elements was arbitrarily set at 1.0 second (a one microsecond pulse width sampled in ten intervals would be transformed into a ten second pulse width in readout).

Input impedance was made large to minimize loading distortion of the input pulse. An emitter follower was used as the input element for this reason, and to provide a low impedance driver for successive circuit elements. The output circuit element was also made an emitter follower for similar reasons, which were discussed in an earlier paragraph.

Individual Circuit Requirements

The system developed in this study for analysis of non-repetitive

FIGURE 2

BLOCK DIAGRAM OF SAMPLING AND READOUT SYSTEM

pulses consists of an interconnection of eleven basic circuits, as was shown previously in Figure 2, page 6. Table I lists each type of circuit used, along with the number of individual circuits required to assemble a ten-interval sampling, storage and readout system. In this chapter, only a general description of circuit requirements will be given. Operational theory and design principles utilized in developing these circuits will be discussed in Chapter III, in detail.

Trigger circuit. A trigger circuit is used to generate a constant amplitude, constant duration trigger pulse synchronized with an input pulse varying in both amplitude and duration. Figure 3 is a schematic of the trigger circuit used, which consists of a hybrid monostable multivibrator using a transistor and a tunnel diode.¹ The multivibrator is driven by a conventional common emitter amplifier.

The input impedance of the amplifier is approximately 5K ohms. In instances where this impedance causes objectional loading of the input pulse, an intermediate emitter follower buffer should be used to increase circuit input impedance. The circuit generates a constant 10 volt, 1 microsecond trigger pulse when driven by an input pulse between 1.0 and 10 volts in amplitude, and 0.1 microsecond or longer in duration.

Buffer. A buffer circuit is used to isolate the input pulse from the operating circuits. Its primary purpose is to transform a high impedance input pulse to a low impedance pulse capable of driving the sampling circuits. An emitter follower is used for this purpose

TABLE I
INDIVIDUAL CIRCUIT REQUIREMENTS FOR TEN CHANNEL SAMPLING SYSTEM

Item No.	Circuit Identification	Number Required
1	Trigger Circuit	1
2	Buffer Input	1
3	Delay	10
4	Sampling Circuit	11
5	Differential Amplifier	10
6	Amplifier	10
7	Slow Time Base Trigger	1
8	Storage Drive Clock	1
9	Storage and Sequential Driver	10
10	OR Gate	1
11	Buffer Output	1

FIGURE 3

TRIGGER CIRCUIT

Since the impedance requirements are most easily met, and the unity gain is also desirable at this stage of operation. Figure 4 is a schematic of the input emitter follower buffer amplifier used in this study.

Delay. Delayed triggers for switching the sampling circuits are obtained from a cascaded delay line string. Trigger outputs are derived from emitter follower buffers which tap the delay line string between sections. Figure 5 shows the method used in generating step delayed trigger pulses.

The delay line string is terminated by the line characteristic impedance to eliminate pulse reflections. The trigger amplifier driving the string is also designed to match the line impedance. Lumped-constant delay sections, with matching characteristic impedances, were cascaded to form the delay string. The input impedance of the emitter follower buffers used to tap off trigger pulses between delay sections was made as large as possible to minimize pulse distortion and reflections along the line resulting from line impedance mis-match.

Sampling circuit. Pulse sampling is accomplished by a specially designed circuit, shown schematically in Figure 6. The circuit is basically an RC integrator, with the integrating capacitor clamped by a tunnel diode clamping circuit.

Switching is accomplished by a delayed trigger pulse. Biasing and triggering characteristics for the tunnel diode are shown in Figure 7.

FIGURE 4

INPUT BUFFER

FIGURE 5

DELAY CIRCUIT

FIGURE 6

SAMPLING (COINCIDENCE) CIRCUIT

HOFFMAN IN2931 TUNNEL DIODE, TD2

FIGURE 7

TUNNEL DIODE BIASING AND TRIGGERING

The tunnel diode is biased in the low voltage state. Negative bias voltage applied to the tunnel diode cathode is of such value that, allowing for drops across the tunnel diode and the capacitor clamping diode, the DC level at the integrating capacitor output is approximately zero. This bias arrangement eliminates the need for a special bias current circuit for the clamping diode, since this current is derived from the input buffer.

In operation, the pulse applied to the sampling circuit is clamped to zero at the integrating capacitor until such time as a delayed trigger pulse is applied to the tunnel diode. The tunnel diode is biased in its low voltage state just below the peak current switching point. Application of the trigger pulse causes the forward tunnel diode current to exceed the peak point, and switching to the high voltage state occurs (switching is accomplished in a matter of nanoseconds, which permits the application of this circuit to sampling of fast pulses). With the tunnel diode in its high voltage state, the integrating capacitor clamp is removed and energy from the remaining portion of the input pulse is integrated.

Each individual sampling circuit then contains in the integrating capacitor energy representing that portion of the input pulse following the time the delayed trigger was applied.

Differential amplifier. Voltage output pulses from two consecutive sampling circuits are applied to a differential amplifier to arrive at a voltage pulse which represents a sampling interval of the

input pulse. Since each sampling circuit output represents that portion of the input pulse occurring after application of the delayed trigger, then the differential output of two sampling circuits--the output of a circuit minus the output of the following circuit--represents one sampling interval of the input pulse.

The differential amplifier serves a second useful purpose, which is amplification of the differential pulse. Since integration of the basic input pulse produces a sampling output smaller than the original input by a factor of about 20, amplification at this stage of operation is highly desirable. Figure 8 is a schematic of the differential amplifier circuitry.

Amplifier. Rise time limitations in the differential amplifier previously discussed made necessary a reduction in gain in order to provide sufficiently fast rise time to follow the output pulse from the sampling circuit. Since one of the objectives of this study was to provide an overall unity voltage gain for the system, the addition of a separate amplification section in each channel was required.

The amplifier was designed with variable emitter degeneration to provide voltage gain adjustment. This provided a separate calibration adjustment for each sampling and storage channel. A single-stage, conventional common-emitter amplifier design was used. Phase reversal was overcome by driving the amplifier from the negative-going side of the differential amplifier. An emitter follower buffer was used between

FIGURE 8

DIFFERENTIAL AMPLIFIER

the differential amplifier and this amplifier to obtain improved rise time response. A schematic of the amplifier design used is shown in Figure 9.

Slow time base trigger. Storage of pulse information is performed by a capacitor. Since such a storage device is subject to dielectric and other losses, stored energy cannot be maintained for long periods of time. For this reason, readout from the storage circuit is initiated simultaneously with the occurrence of the input pulse. To accomplish this simultaneous triggering a relay closure was used, since precise timing was not of importance. The relay closure current was supplied by a silicon-controlled switch (SCS) driven by the trigger circuit. Figure 10 is a schematic of the circuit used.

Two sets of relay contacts were available. One set is used to apply supply voltage to the storage drive clock. The second contact set is not used in the system, but is intended for use as a trigger source for an external readout device, such as an X-Y plotter, oscillograph or oscilloscope.

Storage drive clock. The storage drive clock is a unijunction relaxation oscillator used to supply trigger pulses to the storage circuit sequential drivers. Operation of the clock is initiated by closure of the slow time base trigger relay, which applied DC supply voltage to the clock circuit.

$$A = \frac{e_o}{e_i} \approx 20$$

FIGURE 9

AMPLIFIER

Figure 11 is a schematic of the clock circuit. Timing is accomplished by means of an R-C circuit. A repetition rate of one pulse per second was used for this study; however, a variable resistance was included to permit timing variations.

Storage and sequential driver. Pulse information is stored in a capacitive element. The capacitor is charged with pulse information energy from a low impedance, parallel transistor driver circuit. A charging diode is used to retain pulse information in the capacitor for readout.

A transistor and SCS sequential driver circuit is used to block the storage capacitor output diode, holding pulse information energy in the storage capacitor. Ten such circuits are cascaded in a ten interval sampling system; however, only two were used in this study. The first circuit in the string is triggered by the first clock pulse, the second circuit by the second pulse and on down the line, until the tenth circuit is triggered by the tenth clock pulse. In this manner, pulse information is read out sequentially at a slow time rate for the ten sampling intervals. The complete storage and sequential driver circuit is shown in Figure 12.

OR gate. An OR gate is used to couple the output energy from each storage capacitor to a common output circuit. A conventional diode gating system, as shown by Figure 13, is used for this purpose.

FIGURE 10

SLOW TIME BASE TRIGGER

FIGURE 11

STORAGE DRIVE CLOCK

FIGURE 12

STORAGE AND SEQUENTIAL DRIVER

Buffer output. It was desirable to provide a low impedance output circuit to facilitate operation of the system with conventional readout devices. However, to obtain maximum output pulse width from the individual storage circuits, outputs from these circuits required a high value of load impedance. An emitter follower output circuit satisfied both requirements. The circuit used in this study is shown in Figure 14.

Input-Output Relationships

The output waveform generated by this system in response to an input pulse is not a smooth, continuous reproduction of the input waveform. Instead, the output is a series of voltage "spikes", whose peak amplitudes outline the envelope of the input waveform. It remains, then, to trace in the waveform manually from this information. Figure 15 shows the output response that would be obtained for a variety of input pulse waveforms.

FIGURE 13

OR GATE

FIGURE 14

EMITTER FOLLOWER OUTPUT

FIGURE 15

INPUT-OUTPUT RELATIONSHIPS

CHAPTER III

CIRCUIT DESIGN THEORY AND PRINCIPLES

Design of the individual circuits making up the pulse sampling and storage readout system was performed making use of conventional circuit techniques wherever possible. Due to the number of circuits involved a detailed discussion of conventional designs, other than gain, impedance or other critical requirements, will not be presented. Three of the circuits used, the sampling circuit, differential amplifier, and the storage and sequential driver, are of sufficiently specialized design to require a more complete discussion of design theory and principles.

In the following paragraphs, design theory and principles as applied to the individual circuits will be discussed as the design of each circuit is evolved. Expected system overall response is defined at the close of the chapter.

Individual Circuit Design

The design of each circuit described in Chapter II will be considered in the following paragraphs. Emphasis will be placed only on those circuits of specialized nature.

Trigger circuit. The trigger circuit used in this study is a conventional transistor, tunnel diode monostable multivibrator.¹ This circuit is driven by a high-gain switching amplifier, as shown in

Figure 3, page 9. Q_1 and Q_2 are 2N1613 NPN transistors. The tunnel diode, designated as TDL, is a silicon Hoffman 1N2930. In order to accomplish switching of Q_2 by TDL, it was necessary to add diode D2 for added bias voltage. D2 is a germanium diode with about 0.3 volt forward drop.

Normally, TDL is in its high voltage condition causing Q_2 to be saturated. An input pulse of 1 volt or more generates a 14 volt negative pulse at D1 cathode. This reduces current through TDL to below i_v , causing TDL to switch to its low voltage state and Q_2 to become unsaturated. This condition persists until the current through inductor L_1 increases to a level allowing TDL current to exceed i_p (duration is determined by R_6 - L_1 time constant), at which time TDL switches and Q_2 again saturates.

The pulse generated by Q_2 is coupled to an emitter follower output to provide a low impedance output for driving the delay circuits. An output pulse of about 10 volts in amplitude, and 1 microsecond in duration is generated by this circuit in response to an input pulse of at least 0.1 microsecond duration, and between 1 and 10 volts in amplitude.

Buffer. The input buffer circuit is a conventional emitter follower circuit used to provide a low impedance source for driving the sampling circuits, yet presenting a large input impedance to the input pulse. Figure 4, page 11, is the circuit schematic. Q_1 is a 2N1613.

Output impedance of this circuit is given by equation 3.1.

$$R_o \cong R_{12} \parallel \frac{h_{ie} + R_{11}}{1 + h_{fe}} \quad (3.1)$$

Since for 2N1613 used for Q_4 , $h_{ie} = 2200$ (for $I_E = 1\text{ma}$) and $h_{fe} \cong 80$, then

$$R_o \cong 1000 \parallel \frac{2200 + 10K}{80 + 1} = 130 \Omega$$

Delay. Trigger pulse delay was accomplished by conventional 500 ohm, lumped constant delay lines with open terminations. The experimental circuit used is shown in Figure 5. From the figure, it may be seen that the individual 0.3 microsecond delay sections are connected in series, and at each interconnection an emitter follower buffer is used to tap off a delayed trigger pulse. The three sections used in this study provide trigger pulses delayed 0.3, 0.6 and 0.9 microsecond.

Emitter follower buffers (Q_5 , Q_6 and Q_7) are used to minimize line loading, since each delay section is impedance matched into the following section. Any mismatch caused by external loading would cause pulse reflections and distortion along the complete line. Loading due to the buffer stages is determined by equation 3.2.

$$R_i = R_{14} \parallel \left[h_{ie} + (1 + h_{fe}) \frac{R_{15} R_t}{R_{15} + R_t} \right] \quad (3.2)$$

R_t is the trigger load impedance of the sampling circuit, 1800 ohms.

Q_5 is a 2N1613, for which $h_{fe} \cong 80$, and $h_{ie} \cong 7100$ ohms for $I_E = 0.3\text{ma}$.

Using these values in equation 3.2, it was determined that R_i , the

buffer input impedance, is $58K\Omega$. This impedance, paralleling the 500Ω characteristic line impedance, lowers the matching impedance to 495Ω , a mismatch of only 1.0%. This low degree of mismatch will cause no significant delayed trigger problems.

Assuming no delay line losses, and an emitter follower gain of 0.9, for a 10 volt, 1 microsecond driving pulse, trigger pulses of 9 volts amplitude and 1 microsecond duration will be available with delays of 0.3, 0.6, and 0.9 microsecond.

A practical system consisting of ten or more sampling channels would use this same method for obtaining delayed triggers. Ten commercial delay lines, each having 0.1 microsecond delay would be used, with a buffer output stage at each interconnection. The value of the driver impedance and of R_{13} would be adjusted to match the characteristic impedance of the delay section used.

Sampling (coincidence). The sampling (or coincidence) circuit used in this study is of special design. Since this is not a conventional circuit, the design evolution will be discussed in detail.

An RC integrator switched by a diode, tunnel diode clamp forms the basic sampling circuit, which may be seen in Figure 6, page 13. $R_{19}C_4$ forms the basic integrator, while the switching and clamping function is performed by D3 in series with TD2. Bias current for TD2 is derived from a 24 volt source through R_{20} . R_{21} couples the delayed trigger from a delay section to TD2. D3 is a Fairchild FSD 200, while TD2 is a Hoffman 1N2931.

For optimum integration, the time constant of the integrating circuit must be at least fifteen times greater than the duration of the waveform to be integrated.² Since a waveform of 1.0 microsecond duration is to be sampled then

$$R_{19} C_4 \geq 15 (1.0) \times 10^{-6} \quad (3.3)$$

$R_{19} C_4$ must then have a minimum value of 15 microseconds.

Operating characteristics for the 1N2931 are shown in Figure 16.

From these characteristics it is seen that

$$\begin{aligned} I_p &\cong 10 \text{ ma} & I_v &\cong 3 \text{ ma} & V_p &\cong 0.1 \text{ V} \\ V_v &\cong 0.5 \text{ V} & V_F &\cong 0.8 \text{ V} \end{aligned}$$

Bias current for TD2, I_b , is first arbitrarily set at 4 ma. From this,

$$R_{20} = \frac{E_{s1} - E_B - V_p}{I_b} = \frac{24 - (-0.7) - 0.1}{4 \times 10^{-3}} \quad (3.4)$$

$R_{20} = 6100 \Omega$. A value of $5.6 \text{ K}\Omega$ was selected, which provides 4.4 ma bias current with TD1 in the low voltage state and 4.2 ma in the high voltage state. Since this level is greater than the I_v value of 3 ma, TD2 will remain in the high voltage state after triggering until the 24 volt supply is interrupted, at which time it will reset to its low voltage state.

The current, I_c , which may be clamped by TD2 without causing switching is determined by equation 3.5:

V-I CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (25°C)

EIA TYPE NO.	PEAK CURRENT ¹ I_p (mA)	MINIMUM PEAK-TO-VALLEY CURRENT RATIO I_p/I_v	TYPICAL VALLEY-TO-PEAK VOLTAGE RATIO ² V_v/V_p	TYPICAL NEGATIVE RESISTANCE $-R$ (OHMS)	MAXIMUM SERIES RESISTANCE R_s (OHMS)	TYPICAL SERIES INDUCTANCE ³ L_s mμH	TYPICAL RESISTIVE CUTOFF FREQUENCY (mc)
1N2928	.47	3.5	6.8	470	1	4	350
1N2929	1.0	3.5	6.8	220	1	4	380
1N2930	4.7	3.5	6.8	47	1	4	300
1N2931	10.0	3.5	6.8	22	1	4	150
1N2932	22.0	3.5	6.8	10	1	4	115
1N2933	47.0	3.5	6.8	4.7	1	4	100
1N2934	100.0	3.5	6.8	2.2	1	4	115

FIGURE 16

1N2931 OPERATING CHARACTERISTICS

$$I_c < (I_p - I_b) = 10.0 - 4.4 \times 10^{-3} \quad (3.5)$$

$$I_c < 4.6 \text{ ma}$$

Input pulse current not exceeding 4.6 ma can be clamped by TD2. For a maximum input pulse of 10V, R_{19} may be determined using equation 3.6.

$$R_{19} = \frac{e_{in} - V_{D1} - V_P - E_B}{I_c}$$

$$R_{19} = \frac{10 - 0.6 - 0.1 - (-0.7)}{4.6 \times 10^{-3}} \quad (3.6)$$

$$R_{19} = 2200 \Omega$$

From (3.3), $R_{19}C_4 \geq 15$ microseconds. C_4 may then be determined as equation 3.7.

$$C_4 \geq \frac{15 \times 10^{-6}}{R_{19}} = \frac{15 \times 10^{-6}}{2.2 \times 10^3} \quad (3.7)$$

From (3.7), C_4 can be no smaller than 6800 picofarads. Since further increase in the time constant would reduce voltage gain, the value of C_4 was established at 6800 picofarads.

R_{21} must provide adequate trigger current, I_t , from the delayed trigger source (Figure 5, page 12) to assure driving TD2 to its high voltage state. A current value of 6 ma was arbitrarily selected which, in conjunction with I_b , will supply 10.4 ma to TD2. The value of R_{21} is determined from equation 3.8. It is assumed that a 10 volt trigger pulse, E_T , is sufficient to trigger TD2.

$$\begin{aligned}
 R_{21} &= \frac{E_T - V_P - E_B}{I_T} \\
 &= \frac{10 - 0.1 - (-0.7)}{6 \times 10^{-3}} \\
 &= 1770 \Omega
 \end{aligned} \tag{3.8}$$

R_{21} was established as 1500Ω .

The voltage swing of TD2 is $0.7V$ ($V_f - V_p$). To prevent clipping of the integrated output pulse, maximum integrator output must not exceed $0.7V$. Integrator operation is described by equation 3.9.

$$e_i = i_1 R_{19} + \frac{1}{C_4} \times \int i_1 dt \tag{3.9}$$

Since $R_{19}C_4 > 15T$, the voltage developed across C_4 during the period of integration, T , is negligible compared with that across R_{19} , i_1 may be expressed as equation 3.10.

$$i_1 \cong \frac{e_i}{R_{19}} \tag{3.10}$$

Substituting (3.10) into (3.9), equation 3.11 is obtained.

$$e_i \cong i_1 R_{19} + \frac{1}{R_{19}C_4} \times \int e_i dt \tag{3.11}$$

It is seen that $e_o = e_i - i_1 R_{19}$. Using this relationship, (3.11) may be reduced to equation 3.12.

$$e_o \cong \frac{1}{R_{19}C_4} \int e_i dt \tag{3.12}$$

Assuming a maximum square pulse of $10V$ amplitude and an integration time of 1.0 microsecond, maximum e_o is determined in equation 3.13.

$$e_{oMAX} = \frac{1}{R_{i9}C_{14}} \int_0^{1 \times 10^{-6}} 10 dt$$

$$e_{oMAX} = \frac{1}{15 \times 10^{-6}} \left[10t \right]_0^{1 \times 10^{-6}} \quad (3.13)$$

$$e_{oMAX} = 0.67V$$

Since e_{oMAX} is less than the 0.7V swing of TD2, the sampling circuit will function properly for input pulses not exceeding 10 volts in amplitude, and 1 microsecond in duration.

E_B was selected to establish the DC level of the sampling circuit output at near zero. The -0.7V value offsets the series diode and tunnel diode drops of approximately 0.6V for D1 and 0.1V for V_p of TD2, as is seen in equation 3.14.

$$E_B + V_p + V_{D1} = 0 \quad (3.14)$$

Response of the circuit may be considered using the input pulse shown in Figure 1, page 4. Assume that the delayed trigger pulse occurs coincident in time with t_4 . e_o may be written in two steps, as equations 3.15 and 3.16.

$$e_o = 0 \quad (t \leq t_4) \quad (3.15)$$

$$e_o \cong \frac{1}{R_{i9}C_4} \int_{t_4}^{t_{10}} e_i dt \quad (t_4 < t \leq t_{10}) \quad (3.16)$$

For $t \leq t_4$, C_4 is clamped by D3 and TD2. For $t \geq t_4$, TD2 is triggered to its high voltage state, lifting the clamp on C_4 . For the pulse of Figure 1, page 4, (3.16) may be solved to obtain

$$e_o \cong \frac{1}{15 \times 10^{-6}} [10t] \frac{1.0 \times 10^{-6}}{0.4 \times 10^{-6}}$$

$$e_o = \frac{(10-4)}{(15)} \times 10^{-6} = 0.4 V$$

A similar calculation could be performed for any other delayed triggering point between t_0 and t_{10} . Figure 17 shows e_o as a function of triggering point for trigger application at t_0 , t_4 and t_8 .

Differential amplifier. The differential amplifier used in this study is of sufficiently specialized design to justify a comprehensive treatment. Figure 8, page 17, is a schematic of this design. Q_8 and Q_{11} are buffer amplifiers used to provide low impedance driving sources for the differential amplifier, with minimal loading on the sampling integrator. Input impedance of each buffer is approximately $30K \Omega$, while output impedance is about 380Ω .

Q_9 and Q_{10} make up the differential amplifier. The sum of the collector currents flowing in Q_9 and Q_{10} is at all times constant, and is determined by Q_{12} , which functions as a constant current generator.³ Q_8 through Q_{11} are 2N1613 transistors ($h_{ie} = 4300$ for $I_E = 0.5ma$, and $h_{fe} \cong 80$).

For the configuration used, differential amplifier gain may be approximated as shown in equation 3.17.

$$A \cong \frac{R_L}{2R_e} = \frac{R_{25}}{2R_{27}} \quad (3.17)$$

This expression represents gain of the differential pulse at either Q_9 or Q_{10} collector with respect to ground.

FIGURE 17

OUTPUT CHARACTERISTICS OF SAMPLING
CIRCUIT AT VARIOUS TRIGGER POINTS

Constant current generator Q_{12} is designed to regulate total current flow at 1 ma. Under balanced conditions ($e_1 = e_2$), Q_9 and Q_{10} each carry 0.5 ma. A value of $1K \Omega$ was arbitrarily selected for R_{27} and R_{28} . A maximum shift of 0.5 ma in $Q_9 - Q_{10}$ current division will cause an emitter voltage change of only 0.5V using this value. Q_9 and Q_{10} base voltages are approximately zero. V_{BE} is assumed to be 0.5V. Q_9 or Q_{10} must not saturate when carrying 1 ma collector current, which limits the maximum value of R_{25} and R_{26} . Equation 3.18 defines maximum collector load resistance, R_{25} and R_{26} , which will result in a V_{CE} value of 2.5V for Q_9 or Q_{10} when $I_C = 1$ ma.

$$R_{25MAX} = R_{26MAX} = \frac{E_{S1} - V_{CE} + V_{BE}}{1 \times 10^{-3}}$$

$$R_{25MAX} = R_{26MAX} = \frac{24 - 2.5 + 0.5}{1 \times 10^{-3}} \quad (3.18)$$

$$R_{25MAX} = R_{26MAX} = 22K \Omega$$

R_{25} and R_{26} should be established at this value for maximum voltage gain. It was determined during the study, however, that amplifier response time was not adequate using this value. For this reason, R_{25} and R_{26} were decreased to $10K \Omega$. Although voltage gain was reduced, the required frequency response was obtained. Using (3.17), voltage gain for the differential amplifier may now be determined as

$$A \cong \frac{10K}{(2)(1K)} = 5$$

Under balanced conditions, Q_9 and Q_{10} collector voltage is 19V. A collector voltage swing of 5V is therefore possible. AC coupling is used to eliminate DC drift effects.

A DC amplifier is used as the constant current generator. A resistance divider applies a constant -1.5V bias to the base of Q_{12} . Assuming that $V_{BE} \cong 0.5V$, then the value of R_{29} yielding a constant current, I_C , of 1 ma is determined by equation 3.19.

$$R_{29} = \frac{V_B - V_{BE} - E_C}{I_C} \quad (3.19)$$

$$R_{29} = \frac{-1.5 - 0.5 + 12}{1 \times 10^{-3}} = 10K\Omega$$

Amplifier. One of the system requirements was to have an over-all voltage gain of unity. The integrating function of the sampling circuits results in a drastic loss, and in the differential amplifier compensating voltage gain could not be attained without sacrificing response time. An amplifier stage was added to provide the added gain needed.

The amplifier used in the study is of conventional design, so a detailed design evolution will not be given. Figure 9, page 19, is a schematic of the circuit used. Q_{13} and Q_{14} are 2N1613 transistors. Q_{13} serves as an emitter follower buffer to minimize loading on the differential amplifier, and to speed up amplifier response. The buffer presents a load of $33K\Omega$ to the differential amplifier, and a source impedance of 115Ω to amplifier Q_{14} .

Biasing is accomplished by R_{35} and R_{36} such that Q_{14} operates with a quiescent collector voltage of approximately 8V, giving the amplifier a maximum positive output swing of about 15V.

Amplifier gain is expressed approximately in equation 3.20.

$$A = \frac{e_o}{e_i} \cong \frac{R_{39}}{R_{38}} \cong 20 \quad (3.20)$$

R_{38} in (3.20) is the value unbypassed by C_8 . A gain adjustment is provided by using a 500 Ω trimpot for R_{38} coupled to a 4.7 μ f bypass capacitor C_8 .

Slow time base trigger. An SCS (silicon controlled switch) is used to pull in a relay to provide clock supply voltage and a contact closure for an external time base. The circuit used is a simple one, as shown in Figure 10, page 21, so no detailed discussion is necessary. SCS1 is turned on by a trigger circuit output pulse, pulling in relay K1. A set of relay contacts supplies clock drive power, E_{S1S} , while the second contact set may be used to actuate a readout device time base. D1 is an FSD 200 diode used to prevent application of excess voltage to SCS1 anode from K1 back emf. SCS1 remains in conduction until E_{S1} is interrupted.

Storage drive clock. A unijunction relaxation oscillator is used to provide clock triggers to drive the storage shift register. The standard circuit used is shown in Figure 11, page 21. PRF is determined by $R_{42}C_9$. Values for R_{42} and C_9 were selected from a unijunction oscillator nomograph.⁴ For a 24V supply voltage, output clock pulses of about 10V amplitude and 10 microseconds duration are generated. R_{43} was established at 560 Ω to provide low source impedance for driving the storage shift register string.

Storage and sequential driver. It is the function of the storage and sequential driver circuit to store amplified differential pulse sampling information, and to drive out this stored pulse energy in response to a storage drive clock trigger. The circuit is of special design, and is shown in schematic form in Figure 12, page 22.

Capacity coupling (C_{10}) is used to avoid allowing for the amplifier (Figure 9, page 19) output DC level. Q_{16} is an emitter follower used to transform from a relatively high impedance amplifier output to a lower driving impedance. Q_{17} and Q_{18} are paralleled to provide adequate charging current for storage capacitor C_{11} . Output impedance of Q_{16} is determined by equation 3.21.

$$R_o \cong R_{46} \parallel \frac{h_{ie} + R_g}{1 + h_{fe}} \quad (3.21)$$

R_g is the source impedance driving Q_{16} , and has a value of about $8.4K\Omega$. Q_{16} through Q_{19} are 2N1613 transistors ($h_{fe} \cong 80$, and $h_{ie} = 2200$ at $I_E = 1$ ma for Q_{16} , Q_{17} and Q_{18} , and $h_{ie} = 240$ at $I_E = 15$ ma for Q_{19}). Solving (3.21) yields a value of R_o of 116Ω . Using R_o from (3.21), source impedance of the parallel driver may now be determined from equation 3.22.

$$R_s \cong R_{47} \parallel \frac{\frac{h_{ie}}{2} + R_o}{1 + h_{fe}} \quad (3.22)$$

Solving (3.22) indicates that the source impedance, R_s , of the Q_{17} and Q_{18} parallel driver circuit is about 15Ω . R_s must be as small as is practical to provide adequate drive for charging storage capacitor C_{11} . Since this value was determined using small signal characteristics, it

may be used only as a guide in evaluating C_{11} . C_{11} was determined experimentally to be 0.2 microfarad. Using this value, the circuit responds to an input pulse with rise time of 2 microseconds. Assuming four $R_S C_{11}$ time constants will charge C_{11} to the input pulse amplitude, the actual value of R_S is determined in equation 3.23.

$$4R_S C_{11} = 2 \times 10^{-6} \text{ Sec} \quad (3.23)$$

$$R_S = \frac{(2)(10^{-6})}{(4)(0.2)(10^{-6})} = 2.5 \Omega$$

Assuming emitter follower voltage gains of 0.9, the voltage level of the energy stored in C_{11} , e_s , is related to input pulse e_i by equation 3.24.

$$e_s = A(Q_{16}) \times A(Q_{17}, Q_{18}) \times e_i \quad (3.24)$$

$$e_s = (0.9)(0.9) e_i = (0.81) e_i$$

Diodes D5 and D6 are holding diodes used to hold stored pulse sampling energy in C_{11} until time for readout. FSD 200 diodes, which exhibit a leakage impedance, R_R , of 1500 megohms, are used. C_{11} is a low-loss mylar dielectric metal foil capacitor. Discharge time constant of C_{11} through D5 is then 300 seconds. Decrease of e_s as a function of storage time is expressed by equation 3.25.

$$e_s f(t) = e_s(i) e^{-\frac{t}{R_R C_{11}}} \quad (3.25)$$

This equation indicates that the stored voltage level decreases exponentially from the initial voltage value. After 10 seconds of storage,

$$e_s(t = 10 \text{ sec}) = e_s(i) \frac{1}{e^{\frac{10}{300}}} = \frac{e_s(i)}{0.033}$$

or
$$e_s(t = 10 \text{ sec}) = 0.97 e_s(1 \text{ sec})$$

This relationship indicates that error due to storage losses will not exceed 3%.

Holding voltage V_H is applied to the cathode of D6 to hold stored pulse energy in C_{11} . This voltage is clamped through R_{48} and D8 by Q_{19} such that the DC output level is approximately zero. V_H is determined by equation 3.26.

$$V_H = E_{S2} - I_H R_{50} - V_{D7} \quad (3.26)$$

D7 is an FSD 200, and V_{D7} is assumed to be 0.5V. Neglecting Q_{19} drive current, I_H is determined from equation 3.27.

$$I_H = \frac{E_{S2} - V_{D7} - V_{D8} - V_{CE(Q19)} - E_B}{R_{50} + R_{48}} \quad (3.27)$$

V_H is established at approximately 12.5V in order to prevent diode limiting of storage pulses by D6. It is also desired to limit SCS2 current to 100 ma. Setting R_{50} at 150 Ω satisfies this requirement. R_{48} must be as small as possible to minimize output voltage division losses, yet must be large enough to maintain V_H at 12.5V with Q_{19} saturated. Solving (3.26) and (3.27) simultaneously yields a value of 915 Ω for R_{48} . 1000 Ω is the value used.

R_{49} provides added collector current for Q_{19} to speed switching. D8 (an FSD 200) blocks Q_{19} unsaturated collector voltage from the output line. Q_{19} saturated collector current, I_C , is expressed by equation 3.28.

$$I_C(Q19) = I_H + \frac{E_{S1} - V_{CE(SAT)} - E_B}{R_{49}} \quad (3.28)$$

From (3.26), $I_H = 13.4$ ma. Solving (3.28), $I_c = 37.5$ ma. Base drive for Q_{19} is determined using equation 3.29, assuming $V_{BE} = 0.5V$.

$$I_b = \frac{(V_H - V_{D7}) - V_{BE(Q19)} - E_B}{R_{54}} - \frac{V_{BE}}{R_{55}} \quad (3.29)$$

Since Q_{19} has a current gain of approximately 80, a base drive of $470 \mu a$ is required to sustain a collector current of 37.5 ma. Setting R_{55} at $10K \Omega$ in (3.29), R_{54} is determined to be $23.5K$ to just saturate Q_{19} . R_{54} is established at $10K \Omega$ to assure saturation.

SCS2 is triggered by a clock trigger pulse at input (c). D9, C14 and R52 provide trigger steering. Input (d) is connected to input (b) of the preceding shift register in the string. If the DC level at this point is high (preceding circuit has not been triggered), then D9 is reverse biased, blocking the clock trigger pulse. If the preceding circuit has been triggered, this point is low, permitting the clock trigger pulse to trigger SCS2, lowering the DC level at point (b). Point (b) is connected to input (d) of the following stage, permitting the next clock pulse to trigger the following stage, etc. R_{51} is established at 2700Ω to provide adequate SCS trigger current (3 ma), and to minimize clock loading when a number of shift register circuits are connected in parallel (ten circuits place a load of about 270Ω on the clock).

With SCS2 in conduction, assuming an anode to cathode drop of 1V, about $100 \mu a$ base current is supplied to Q_{19} . This results in a collector current of 8 ma drawn through R_{49} . Reverse bias on D8 is then

16V which will prevent clipping of output pulses of less than 16V amplitude.

Triggering of SCS2 performs two functions: (1) V_H is removed, allowing C_{11} to discharge through R_{48} into the output circuit, and (2) the output clamp is lifted allowing the output pulse to pass into the OR gate output circuit.

OR gate. The OR gate consists only of a diode gating system, as shown in Figure 13, page 24, made up of FSD 200 diodes. The circuit used is conventional and uncomplicated, so further discussion is unnecessary. The OR gate is used to drive a common output circuit, without causing interaction between storage circuits.

Emitter follower output. The emitter follower output is used to provide a low output impedance for connection to a readout device. Q_{20} is a 2N1613. R_{56} is established at 22K to obtain adequate OR gate loading while holding voltage division losses across R_{48} (Figure 12, page 22) to about 5%. Input impedance of this circuit is about 17K Ω . Output impedance is determined using equation 3.30.

$$R_o \cong R_{57} \parallel \frac{h_{ie} + R_{56}}{1 + h_{fe}} \quad (3.30)$$

From (3.30), R_o is determined to be approximately 230 Ω . This output impedance value is compatible with input requirements for most commercial readout devices.

Overall Circuit Response

System operation must be concerned with interrelationships between the individual circuits. Voltage gain, circuit response times, pulse fall times and impedance matching are characteristics which must be considered. The following paragraphs serve to relate individual circuit performance to overall system requirements.

Differential coincidence output. Principles of operation for the single sampling circuit (Figure 6, page 13) were developed in earlier paragraphs. However, it is the differential output of two consecutive sampling circuits which is of prime importance.

In (3.12), it was established that

$$e_o \cong \frac{1}{R_{19}C_4} \int e_i dt$$

for the individual sampling circuit. Equation 3.31 is obtained from substitution of (3.10) into (3.12).

$$e_o \cong \frac{1}{R_{19}C_4} \int i_1 R_{19} dt = \frac{1}{C_4} \int i_1 dt \quad (3.31)$$

Consider the input voltage pulse of Figure 18A, applied to two consecutive sampling circuits; the first triggered at time t_1 , and the second at t_2 . Figure 18B shows the C_4 current waveforms for these two circuits, with that of the second circuit shown in dashed lines.

Equation 3.32 expresses the output voltage for the first circuit, while 3.33 describes the second circuit response.

$$e_{o_1} \cong \frac{1}{C_4} \int_{t_1}^T i_1 dt \quad (3.32)$$

$$e_{o2} \cong \frac{1}{C_4} \int_{t_2}^T i_1 dt. \quad (3.33)$$

Differential output voltage for the two circuits may then be written as equation 3.34, by subtracting (3.33) from (3.32)

$$e_{o1} - e_{o2} \cong \frac{1}{C_4} \left[\int_{t_1}^T i_1 dt - \int_{t_2}^T i_1 dt \right] = \frac{1}{C_4} \int_{t_1}^{t_2} i_1 dt \quad (3.34)$$

For small Δt , $\frac{di_1}{dt}$ is approximately linear and the integral portion of (3.34) is the area shown in Figure 18C. If the difference between t_1 and t_2 , Δt , is small, then (3.34) may be written as equation 3.35.

$$e_{o1} - e_{o2} \cong \frac{1}{C_4} \frac{\Delta t}{R_{19}} e_i \left(t_1 + \frac{\Delta t}{2} \right) \quad (3.35)$$

It is seen from (3.35), then, that the differential output from two consecutive sampling circuits is proportional to the average peak amplitude of the input pulse during the sampling interval.

A sampling interval, Δt , of 0.3 microsecond was used in this study. From this, and from the values established for R_{19} and C_4 (Figure 6, page 13), it was determined using (3.35) that

$$e_{o1} - e_{o2} \cong (.02) e_i \left(t_1 + \frac{\Delta t}{2} \right) \quad (3.36)$$

The differential gain of two consecutive sampling circuits, for a 0.3 microsecond sampling interval, is 0.02. The use of smaller sampling intervals would result in a decrease in differential gain.

FIGURE 18A. INPUT VOLTAGE

FIGURE 18B. CAPACITOR CURRENT

FIGURE 18C. DIFFERENTIAL OUTPUT

FIGURE 18

SAMPLING CIRCUIT VOLTAGE AND CURRENT CHARACTERISTICS

Rise times and pulse stretching. Rise times of the input buffer (Figure 4, page 11), sampling circuit (Figure 6, page 13) and delay (Figure 5, page 12), must be sufficiently fast to follow the input pulse rise time. Circuit components available for this study limited possible rise time response to about 50 nanoseconds. Much improved response could be attained using higher speed components. The differential amplifier, amplifier, and storage circuits need respond only to the sampling time interval, which is 0.3 microsecond for this study. The output circuit is required only to follow the rise of C_{11} discharge into this circuit.

Pulse stretching is desirable and is derived from slow discharge of C_4 in the sampling circuit into the differential amplifier input impedance ($30K \Omega$), giving a discharge time constant of about 200 microseconds. Frequency response of the differential amplifier and subsequent circuits is then less critical.

Overall gain figure. Gain figures for each of the circuits in the system are combined in a flow chart shown in Figure 19. The voltage amplitude transfer for the system, G_S , is written in equation 3.37, using information from Figure 19.

$$G_S = (A_1)(A_2)(A_3)(A_4)(A_5)(A_6)(A_7) \quad (3.37)$$

This may be evaluated numerically as

$$\begin{aligned} G_S &= (0.9)(0.02)(0.09)(5.0)(0.9)(20)(0.9)(0.9)(0.95)(1.0)(0.9) \\ &= (.9)^6 (.02)(5.0)(20)(.95) = 1.03 \end{aligned}$$

FIGURE 19

OVERALL SYSTEM GAIN DIAGRAM

Unity gain adjustment. Unity overall system voltage gain was established as a system requirement. A variable gain feature was included in the amplifier design (Figure 9, page 19) to accomplish this objective and provide a compensating adjustment for other circuit variations. Nominal amplifier gain required to obtain unity system gain may be determined by rewriting (3.37) as equation 3.38.

$$G_s = 1.0 = (0.056) A_4 \quad (3.38)$$

From (3.38), it is determined that an amplifier gain of 17.8 is required for unity system gain.

CHAPTER IV

EXPERIMENTAL RESULTS

Experimental results obtained in this study are in acceptable agreement with expected analytic results. A number of design modifications were necessary during the experimental phase of the study in order to obtain desired performance. A major source of difficulty was rise time response. In many instances, notable in the differential amplifier and amplifier circuits, addition of emitter follower buffers was required to reduce source impedance and improve response time. Differential amplifier gain was reduced from 10 to 5 to obtain faster response. Circuits discussed in the text of this thesis represent the final designs developed by analytical and empirical means.

Experimental Set-up

Two complete sampling channels were fabricated for evaluation. Three power sources supplying 24VDC, -12VDC and -0.7VDC were required. An additional 15 VDC requirement was derived from the 24VDC supply by means of a dropping resistor and zener regulator. An oscilloscope was used in checking circuit performance, and input pulses were derived from a manually triggered pulse generator. The experimental set-up is fully described in Appendix A.

Trigger delays for the two experimental channels were set at 0.3, 0.6 and 0.9 microseconds. The initial time delay was included in order to eliminate rise time effects of the input pulse, and to more

fully utilize the tunnel diode switching feature of the sampling circuit. For the experimental phase of this study, then, sampling intervals for the two channels were 0.3 - 0.6 microsecond, and 0.6 - 0.9 microsecond. Rather than vary these delay points during experimental evaluation, it was decided to follow the less troublesome (but equally valid) approach of varying input pulse duration.

Input Waveform Conditions

Several input pulse waveform variations were used in evaluating circuit performance. These included square and exponential waveforms of varying amplitude and duration. System linearity with respect to input pulse amplitude and duration variation was evaluated using a square input pulse. Individual circuit performance was analyzed using a 10V square pulse of 1.5 microseconds duration. After verification of desired performance using square pulses, system response to exponential input pulse waveforms was undertaken.

Comparison of Experimental Results with Design Requirements

Actual performance of individual circuits and the overall system is compared with expected analytical values in the following paragraphs and tabulations.

Response to fixed input pulse. Response of individual circuits and the overall system was observed using an input pulse of 10V amplitude and 1.5 microseconds duration.

A trigger pulse of 10V amplitude and 1.0 microsecond pulse width was obtained from the trigger circuit. Input variation between 1 and 10 volts, with 0.1 microsecond or greater pulse width, had no effect upon the trigger output pulse. However, the pulse obtained exhibited a rise time of 0.15 microsecond between 10% and 90% amplitude points (the pulse reached an 8V level within 0.1 microsecond). For the purposes of this study, performance of the trigger circuit was considered to be adequate.

The times at which sampling circuit switching occurred following application of the input pulse were recorded, and are tabulated in Table II. It is seen that sampling circuit triggering occurs somewhat later than expected. This is due mainly to delay within the trigger circuit (Figure 3, page 9). In a practical system, this inherent trigger delay would be compensated for by treating it as part of the first delay requirement.

Voltage amplitudes at each of the individual circuits are tabulated in Table III, and compared with corresponding analytical values for the fixed input pulse. Analytical values were calculated using switching times of 0.5, 0.8 and 1.1 microseconds for the sampling circuits, taking into account the inherent trigger circuit delay discussed earlier. Low differential sampling circuit gain appears to be caused by nonlinear loading effects of clamp diode D3 (Figure 6, page 13). Low sampling circuit gain was compensated for by emitter follower gains larger than were expected, and by slightly high differential

TABLE II

ACTUAL TRIGGERING TIMES OF EXPERIMENTAL SAMPLING CIRCUITS

Channel	Triggering Time (μ seconds)
1	0.50
2	.82
3	1.20

TABLE III

RESPONSE TO 10V, 1.5 μ SEC FIXED SQUARE INPUT PULSE

Monitor Point	Experimental		Analytical	
	Voltage	Gain	Voltage	Gain
Buffer Out	9.8	0.98	9.0	0.9
Sampler 1	.77		.66	
Sampler 2	.65	.012	.48	.02
Sampler 3	.52	.013	.30	.02
Diff Amp 1	-.70	-5.8	-.81	-4.5
Diff Amp 2	-.70	-5.4	-.81	-4.5
Amplifier 1	13.4	-19.1	14.4	-17.8
Amplifier 2	13.5	-19.3	14.4	-17.8
Storage Cap. 1	13.0	.97	11.7	.81
Storage Cap. 2	13.2	.98	11.7	.81
Storage 1	12.1	.93	11.1	.95
Storage 2	12.4	.94	11.1	.95
Final Output 1	10.0	.83	10.0	.9
Final Output 2	10.0	0.81	10.0	0.9

amplifier gain. For the overall system, unity gain was accomplished by an adjusted amplifier gain value which agreed closely with the calculated value.

Overall system response time to obtain peak charge on C_{11} (see Figure 12, page 22) was measured as 1.9 microseconds. The added 0.4 microsecond following termination of the input pulse may be attributed to inherent circuit delays, and does not degrade performance of the system.

Output pulse duration was measured as about 3 milliseconds at the half-amplitude points. This agrees with the calculated C_{11} discharge time constant of 3.6 milliseconds.

Linearity with varying input pulse amplitude. Response of the amplifier (Figure 9, page 19) and overall system to square, 1.5 microsecond pulses of varying amplitudes is tabulated in Table IV. Experimental results compare favorably with calculated values, although at low input pulse levels the output response falls off somewhat. Response to input pulse amplitudes ranging from 4 to 10 volts agreed closely with calculated output response with unity system gain.

Linearity with varying input pulse duration. The duration of a 10V constant amplitude square input pulse was varied to evaluate system linearity with respect to input pulses of different duration. Amplifier (Figure 9, page 19) and system experimental response is compared with calculated response in Table V. Calculated values presented in this tabulation were developed in Appendix B. It must be noted that the

TABLE IV
RESPONSE TO 1.5 μ SEC SQUARE PULSES OF VARYING AMPLITUDES

Pulse Amplitude	Amplifier Output			Final Output		
	Measured		Calculated	Measured		Calculated
	Ch1	Ch2		Ch1	Ch2	
10	13.4	13.5	14.4	10.0	10.0	10
8	10.4	10.2	11.5	8.3	8.2	8
6	7.5	7.2	8.6	6.0	5.9	6
4	4.5	4.3	5.7	3.8	4.0	4
2	1.6	1.7	2.9	1.3	1.4	2
1	1.1	0.95	1.4	0.9	0.8	1

TABLE V
RESPONSE TO 10V SQUARE PULSE OF VARYING DURATION

Pulse Duration (μ sec)	Amplifier Output				Final Output			
	Channel 1		Channel 2		Channel 1		Channel 2	
	Meas.	Calc.	Meas.	Calc.	Meas.	Calc.	Meas.	Calc.
1.5	13.4V	14.4V	13.6V	14.4V	10.0V	10.0V	10.0V	10.0V
1.2	13.5	14.4	13.8	14.4	10.1	10.0	10.1	10.0
1.0	13.5	14.4	13.8	9.6	10.0	10.0	10.0	6.7
.8	13.4	14.4	11.8	0	10.1	10.0	9.2	0
.6	13.4	4.8	8.8	0	10.1	3.3	6.8	0
.4	12.2	0	6.2	0	9.0	0	4.0	0
0.2	5.5	0	3.5	0	4.0	0	2.0	0

Calculated values are developed in Appendix B.

experimental response did not drop off as sharply with decreasing input pulse duration as was expected. The precise reason for this has not been determined, although it might be attributed to inferior connections in the experimental test set-up or an undesirable undershoot characteristic of the test generator used to supply the input pulse (the experimental test set-up is described in Appendix A).

Response to exponentially rising input pulse. An exponential input pulse, defined by the equation

$$e_{in} = 15.8 \left(1 - e^{\frac{-t}{1.5 \times 10^{-6}}} \right) \quad (4.1)$$

with $0 \leq t \leq 1.5$ microseconds, was used to evaluate system response to an input pulse not having constant voltage amplitude over the pulse duration. Amplifier (Figure 9, page 19) and system response is compared with calculated response in Table VI. Calculated response values used for comparison are determined in Appendix B. Some difference is seen in the comparison. This is in large part due to the assumption of linearity during the 0.3 microsecond sampling interval. Since the sampling interval would normally be much smaller in a practical sampling system, resulting in increased pulse linearity during each interval, error resulting from this assumption would be minimized.

Response to exponentially decaying input pulse. To provide a check on the ability of the system to follow a decreasing input pulse waveform, a pulse defined by equation 4.2 was applied to the system.

$$e_{in} = 10 e^{\frac{-t}{1.5 \times 10^{-6}}} \quad (4.2)$$

This pulse, having an initial value of 10V, drops exponentially to 3.7V at 1.5 microseconds. Response of the amplifier (Figure 9, page 19) and overall system to the input pulse of (4.2) is compared with calculated response in Table VII. Calculated response values are developed in Appendix B. The differences noted between experimental and calculated response values may be attributed largely to the assumption of pulse linearity over the relatively long sampling interval, as was discussed in the preceeding section dealing with an exponentially rising input pulse.

Experimental System Waveforms

Oscilloscope photographs of the response of individual circuits and the overall system to a square input pulse of 10V amplitude and 1.5 microseconds duration are compiled in Appendix C. Experimental waveforms were photographed at the following points in the system: (1) each of the three sampling circuit outputs, (2) the channel 1 differential amplifier and amplifier outputs, (3) C_{11} in the storage circuit, and (4) the final output.

Exponential integration waveforms for the sampling circuits show evidence of some distortion. This is due to the non-linear characteristic of clamping diode D3 (see Figure 6, page 13). Since this effect is common for the three circuits, the differential sampling circuit output is not affected.

TABLE VI

RESPONSE TO INPUT PULSE WITH EXPONENTIAL RISE

Channel No.	Amplifier Output (volts)		Final Output (volts)	
	Measured	Calculated	Measured	Calculated
1	7.2	8.0	6.6	5.6
2	9.5	11.6	8.0	7.4

TABLE VII

RESPONSE TO INPUT PULSE WITH EXPONENTIAL DECAY

Channel No.	Amplifier Output (volts)		Final Output (volts)	
	Measured	Calculated	Measured	Calculated
1	7.5	9.4	6.8	6.5
2	6.4	7.5	5.8	5.3

CHAPTER V

CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER STUDY

Conclusions

The slow time base readout system developed in this study for non-repetitive pulse analysis met, for the most part, design objectives. Within design maximums of 10V amplitude and 1.5 microseconds pulse duration, the experimental system performed satisfactorily, although linearity with respect to varying input pulse duration did not meet analytical expectations.

Performance of individual circuits comprising the system was, on the whole, satisfactory. Voltage gains of the sampling circuits (Figure 6, page 13) were somewhat lower than the theoretical gain of 0.02. The difference in gain is attributed to diode clamping losses. The storage circuit (Figure 12, page 22) appears capable of retaining pulse information for readout delayed by as much as 10 seconds, with no significant losses. The gain adjustment provided in the amplifier (Figure 9, page 19) is adequate to adjust for an overall channel gain of unity.

Performance of the system using a 0.3 microsecond sampling interval would indicate that a shorter sampling interval of 0.1 microsecond, with 10 sampling channels, should result in improved operation. A pulse of 1 microsecond duration would then be sampled at ten points, resulting in improved waveform resolution.

Recommendations for Further Study

Circuit response improvement. In many instances, emitter follower buffers were used to provide low driving impedances as a means of improving circuit response time, notably in the differential amplifier, amplifier and storage circuits. Response of these circuits could be improved through the use of transistors with better high frequency response characteristics than the 2N1613 used throughout the system. Along with this modification, the sampling time interval should be made about 0.1 microsecond to obtain a usable expanded output pulse waveform. Sampling time intervals may be adjusted to operate on pulses of longer duration, although this would require lowering the maximum allowable input voltage of 10 volts. The essential requirement is that the time integral of the input voltage waveform shall not exceed 10 volt-microseconds if saturation is to be avoided.

Final readout plotter. The narrow pulses obtained as outputs from each of the sampling intervals are unsuitable for most readout devices. It is recommended that a point-to-point linear plotter be developed, which would plot a point-to-point approximation of the output pulse envelope depicted by the peak amplitudes of the individual sampling interval output pulses. Such a device could utilize a constant current generator charging a capacitor to obtain the linear ramps, and would have to sense the peak amplitude of each sampling interval output pulse for driving references.

Linearity. Linearity could be most improved by providing constant bias for the sampling circuit clamp diode (Figure 6, page 13). This would reduce the effects of diode non-linearities upon sampling circuit response. Another area in which diode characteristics affect system linearity is the OR gate (Figure 13, page 24). Bias current applied to the individual diode to stabilize forward voltage drops would improve system linearity, but could necessitate altering of other circuit bias levels.

Circuit simplification. The number of components required for a ten channel analysis system is quite large. It is felt that the amount of circuitry required could be significantly reduced if a means of switching a single set of circuits could be developed to perform the functions of a number of identical circuits in separate channels. It might be possible to switch the differential amplifier, amplifier and storage driver functions in this manner; however, the requirement for delay, sampling, and storage output circuits could not be reduced.

Nanosecond sampling system. The concept of pulse sampling should be applicable to analysis of pulses of several nanoseconds duration. Development of a nanosecond sampling and readout system could be undertaken. Such a system would require circuit approaches quite different from those used in this study.

LIST OF REFERENCES

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1. RCA Semiconductor and Materials Division, Tunnel Diodes for Switching and Microwave Application (Somerville: Radio Corporation of America, 1963), p. 57.
2. Jacob Millman, Herbert Taub, Pulse and Digital Circuits (New York: McGraw-Hill Book Company, Inc., 1956), p. 46.
3. Brian H. Bell, "A Low Level Differential Chopper Amplifier", National Semiconductor Corporation, General Engineering Memo no. 10 (October, 1962).
4. J. F. Cleary, Transistor Manual (New York: General Electric Company, 1962), p. 195.

BIBLIOGRAPHY

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A. BOOKS

- Cleary, J. F. Transistor Manual. New York: General Electric Company, 1962.
- Gartner, Wolfgang W. Transistors. Princeton: D. Van Nostrand Company, Inc., 1960.
- LeCroisette, Dennis. Transistors. Englewood Cliffs: Prentice-Hall, Inc., 1963.
- Millman, Jacob, and Herbert Taub. Pulse and Digital Circuits. New York: McGraw-Hill Book Company, Inc., 1956.
- RCA Semiconductor and Materials Division. Tunnel Diodes for Switching and Microwave Application. Somerville: Radio Corporation of America, 1963.

B. TECHNICAL REPORTS

- Bell, Brian H. "A Low Level Differential Chopper Amplifier". National Semiconductor Corporation, General Engineering Memo no. 10 (October, 1962).
- Hilbiber, David F. "A New D-C Transistor Differential Amplifier". Fairchild Semiconductor Corporation, TP-16 (February, 1961).

APPENDIX A

APPENDIX A

EXPERIMENTAL SET-UP

The experimental system used in this study was fabricated on two phenolic breadboards. The first breadboard contained the input buffer, delay, sampling and differential amplifier circuits. Outputs from the two differential amplifiers were interconnected with the second breadboard, containing the remaining system circuits. The block diagram and list of test equipment used for the experimental work are shown in Figure 20.

TEST EQUIPMENT

PULSE GENERATOR: Hewlett-Packard Model 212

POWER SUPPLIES: Power Designs Model 4005

OSCILLOSCOPE: Tektronix Model 531 with Type H Preamplifier

INPUT PULSE SHAPER: R-C Integrator and Differentiator for Exponential Shaping

FIGURE 20

EXPERIMENTAL TEST SET-UP

APPENDIX B

APPENDIX B

CALCULATED SYSTEM RESPONSE VALUES

System response to square input pulses of variable duration, and to exponential rising and decaying input pulses was compared with experimental response in Chapter IV. Analytical response values used for comparison are determined in the following paragraphs.

System Response to Square Input Pulses of Variable Duration

From Table II, page 54, triggering of the three sampling circuits occurs at 0.5, 0.8 and 1.1 microseconds. Differential sampling circuit response as a function of varying input pulse duration is determined using (3.34), where pulse width is designated as T .

$$e_{o_1} - e_{o_2} \cong \frac{1}{C_4} \left[\int_{t_1}^T i_1 dt - \int_{t_1}^T i_1 dt \right] \quad (3.34)$$

For $T < t_2$, it is seen that

$$\Delta e_o = e_{o_1} - e_{o_2} \cong \frac{1}{C_4} \int_{t_1}^{t_2} i_1 dt \quad (B.1)$$

Using (B.1), then (3.35) may be written as

$$\Delta e_o \cong \frac{1}{C_4} \frac{T-t_1}{R_{19}} e_i \left(t_1 + \frac{T-t_1}{2} \right)$$

or

$$\Delta e_o \cong \frac{T-t_1}{C_4 R_{19}} \times e_i \left(\frac{t_1 + T}{2} \right) \quad (B.2)$$

For the two experimental sampling channels, t_1 and t_2 are defined as follows:

Channel	(microseconds)	
	t_1	t_2
1	0.5	0.8
2	0.8	0.11

For a constant 10V square input pulse, (B.2) may be simplified as

$$\Delta e \cong (0.67) (10^6) (T - t_1) \quad (B.3)$$

for

$$t_1 \leq T \leq t_2$$

For $T > t_2$, $\Delta e_0 \cong 0.2V$. Overall system gain is unity for a differential sampling circuit gain of 0.02 (Δe_0 for a 10V square input pulse is 0.2V). From Table III, page 54, it is seen that for unity system gain the output voltage of the amplifier (see Figure 9, page 19) is 1.44 times the input voltage to the system. For differential sampling circuit output as defined by (B.3), amplifier and final output voltages are determined by equations B.4 and B.5, for a 10V square input pulse.

$$e_{O(\text{amplifier})} \cong \frac{e_i (0.67) (10^6) (T - t_1) (1.44)}{(0.2)} = (48.1) (10^6) (T - t_1) \quad (B.4)$$

$$e_{O(\text{FINAL})} \cong \frac{e_i (0.67) (10^6) (T - t_1)}{(0.2)} = (33.4) (10^6) (T - t_1) \quad (B.5)$$

Calculated response values for Table V, page 56, were calculated using (B.4) and (B.5).

Input Pulse Duration, (μ sec)	Channel 1			Channel 2		
	$T-t_1$ (μ sec)	Amp. $e_o(V)$	Final $e_o(V)$	$T-t_1$ (μ sec)	Amp. $e_o(V)$	Final $e_o(V)$
1.5	0.3	14.4	10.0	0.3	14.4	10.0
1.2	.3	14.4	10.0	.3	14.4	10.0
1.0	.3	14.4	10.0	.2	9.6	6.7
.8	.3	14.4	10.0	0	0	0
.6	.1	4.8	3.3	0	0	0
.4	0	0	0	0	0	0
.2	0	0	0	0	0	0

System Response to Exponentially Rising Input Pulse

System response to an exponentially rising pulse was compared with calculated response in Table VI, page 59, for an input pulse defined by (4.1)

$$e_{in} = 15.8 \left(1 - e^{-\frac{t}{1.5 \times 10^{-6}}} \right) \quad 0 \leq t \leq 1.5 \mu \text{sec} \quad (4.1)$$

This pulse will attain a value of 10V in 1.5 microseconds. The system has been designed to achieve a unity gain reflecting the average value of the input pulse during each sampling interval. For channel 1 assuming pulse linearity during the sampling interval, the average value occurs at 0.65 microsecond, and at 0.95 microsecond for channel 2. Average values for the input pulse are determined for channel 1 in equation B.3, and for channel 2 in equation B.4, using (4.1).

$$e_{ave} (Ch 1) = 15.8 \left(1 - e^{-\frac{0.65}{1.5}} \right) = 5.6V \quad (B.3)$$

$$e_{ave} (Ch 2) = 15.8 \left(1 - e^{-\frac{0.95}{1.5}} \right) = 7.4V \quad (B.4)$$

Since amplifier output (see Figure 9, page 19) has been calculated to be 1.44 times the average input level during the sampling interval, amplifier and system response to the input pulse per (4.1) may be written as follows:

	Amplifier Output (volts)	Final Output (volts)
Channel 1	8.0	5.6
Channel 2	11.6	7.4

System Response to Exponentially Decaying Input Pulse

System response to an exponentially decaying input pulse defined by (4.2) was compared with calculated response in Table VII.

$$e_{in} = 10 e^{\frac{-t}{1.5 \times 10^{-6}}} \quad (4.2)$$

Assuming pulse linearity during each sampling interval, the average value of the input pulse occurs at 0.65 microsecond for channel 1, and at 0.95 microsecond for channel 2. Using (4.2), for unity system gain, output voltage for channel 1 is determined by equation B.5, and by equation B.6 for channel 2.

$$e_{ave}(Ch1) = 10 e^{\frac{-0.65}{1.5}} = 6.5 V \quad (B.5)$$

$$e_{ave}(Ch2) = 10 e^{\frac{-0.95}{1.5}} = 5.3 V \quad (B.6)$$

Amplifier and final output amplitudes for channels 1 and 2 may now be written as follows (amplifier output is 1.44 times the final output value):

	Amplifier Output (volts)	Final Output (volts)
Channel 1	9.4	6.5
Channel 2	7.5	5.3

APPENDIX C

APPENDIX C

EXPERIMENTAL WAVEFORMS

Experimental waveforms at several points in the system were recorded, and are shown in Figures 21 through 29. These waveforms are in response to a square input pulse of 10V amplitude and 1.5 micro-seconds duration. Voltage and time scale settings used in photographing the waveforms are given with the individual figures.

Output pulse amplitude exhibited no noticeable degradation when storage times were varied. Constant 10V output pulse amplitudes were observed for storage triggers at 0, 2, 4, 6, 8 and 10 seconds.

2 V / CM

FIGURE 21

INPUT PULSE

0.2 V / CM

FIGURE 22

SAMPLING CIRCUIT 1 OUTPUT

FIGURE 23

SAMPLING CIRCUIT 2 OUTPUT

FIGURE 24

SAMPLING CIRCUIT 3 OUTPUT

FIGURE 25

CHANNEL 1 DIFFERENTIAL AMPLIFIER OUTPUT

FIGURE 26

CHANNEL 1 AMPLIFIER OUTPUT

FIGURE 27

CHANNEL 1 STORAGE CAPACITOR, C_{II}

FIGURE 28

FINAL OUTPUT, FAST TIME BASE

FIGURE 29

FINAL OUTPUT, SLOW TIME BASE