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THE DEVELOPMENT OF A SMALL DATA ACQUISITION
AND CONTROL COMPUTER SYSTEM

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THE DEVELOPMENT OF A SMALL DATA ACQUISITION
AND CONTROL COMPUTER SYSTEM*

by

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I. INTRODUCTION

Early in 1968, investigation into the automation of the Gas Analysis Laboratory of the Radiochemistry Division, Lawrence Livermore Laboratory, was begun. The final goal of the program, provided feasibility could be shown, was to develop a completely automatic gas analysis system, which could select a sample, separate the desired components, perform on-line calculations pertinent to the separation in progress, and recover the purified components.

A description of the separation process is necessary to understand the development of the system. Briefly, the separation process starts by measuring the amount of the sample (ranging in quantity from milliliters to tens of liters) in a known volume with a pressure transducer and thermocouple (PVT relationship). Trace components are then added, and the mixed gases are admitted to the separation system.

The sample is separated into its components by a process known as elution chromatography. In this process, the sample is started on an adsorbent column (activated charcoal and/or a molecular sieve) at liquid nitrogen temperatures, with helium carrier gas flowing through the column. The desired separation is achieved by properly adjusting helium flow rate and column temperature, and by programming one or both of these variables as a function of time. At predictable times, dependent upon sample size, composition, column temperature, and helium flow rate, each component of the sample emerges from the column.

A thermal conductivity detector indicates the presence in the gas stream emerging from the column of a component other than the carrier gas. The time of appearance of this component establishes its identity, while the integrated response of the "TC" detector is proportional to the total volume of that component.

Measurement of the ionization current produced in the gas stream by the decay of radioactive components is performed with an ionization chamber detector whose output is measured with a vibrating reed electrometer. Its integrated response is proportional to the total radioactivity of the component.

When a desired component appears at the detector, the gas flow is switched to a collection trap at liquid nitrogen temperatures. All other components are simply carried to air at the carrier gas vent. The purified component is recovered by vacuum distillation from the collection trap to a measuring manifold where the amount recovered is determined.

II. INITIAL DESIGN REQUIREMENTS

It can be seen from the preceding simplified description, that the required inputs and outputs for an automated separation system can be grouped into four general categories:

- 1) Digital inputs (i.e. -- Switch closures)
- 2) Digital outputs (i.e. -- Valves, Heaters)
- 3) Analog inputs (i.e. -- Detectors, Thermocouples)
- 4) Analog outputs (i.e. -- Temp. control)

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for each separation system, it was evident that 10 digital inputs, 60 digital outputs, 12 analog inputs, and 2 analog outputs were required.

The Gas Analysis Laboratory required the automation of six such gas separation systems operating independently of each other. These requirements, plus a consideration of the data rates and available funds, led to the following choice of equipment: A) 12 bit mini-computer with 12k of core memory, B) a paper tape reader/punch, C) a gain switching ADC with a 100 channel multiplexer, and D) a 262k fixed-head disk. Funding limitations made it necessary to acquire this equipment in phases. As a result, during Phase I an 8k PDP-8/I (manufactured by Digital Equipment Corporation and selected on the basis of competitive bidding) was purchased in 1969.

III. HIGH-LEVEL LANGUAGE

With this limited system, preliminary software studies were begun to determine if a high-level language could be used to control the separation system. Only with a suitable high-level language in which to write the application routines which control the separation process could the effort required to code these routines be minimized. Without the high-level language, the scientific personnel associated with this project would have to become full-time programmers for an extended length of time. At this time, FOCAL was one of the better high-level languages available, and it was used in the studies of bandwidth requirements.

FOCAL (and other similar high-level languages) was inherently slow (relatively speaking, of course), and hence, if the data rate of the process to be controlled was too high, FOCAL could not be used. Likewise, the processing algorithm could become too complex, making the time to process a data point greater than the time between data inputs.

A typical processing algorithm (smoothing digital filter) might be the following:

$$Y=A*(X(I-3))+B*(X(I-2))+C*(X(I-1))+D*(X(I)).$$

This filter was implemented and run with FOCAL to determine the time required to evaluate a Y value. This time was determined to be approximately 50 ms. Assuming that each active separation system requires six such filters, then each separation system would require 300 ms of processing time for every data point. FOCAL, then, could process three sample

points per second. Since the sampling rate generally must be ten times the highest frequency to be sampled, the effective bandwidth of a FOCAL system would be approximately 0.3 Hz.

For six separation systems to be active simultaneously, each system can be sampled once every two seconds (i.e. each system must be frequency limited to 0.05 Hz). Considering that the minimum width peak is 30 seconds wide, a peak will be represented by at least 15 samples, which is adequate definition. Thus, with this preliminary study, FOCAL was judged to be an adequate high-level language.

IV. PHASE II

As Phase II funds became available, a very major item which was yet to be acquired was the ADC. Obviously, the ADC was a very critical part of the overall system. Total failure could result without proper attention to noise, ground loops, and bandwidth requirements. Among the various kinds of transducers in the system were thermocouples, flow meters, pressure transducers, electrometers, and thermal conductivity detectors. Since the signals covered a fairly wide dynamic range, programmable gain changes were required in the front end of the ADC. In addition, because of the electrically noisy environment (from high power heaters and solenoid valves), a fully guarded and integrating ADC seemed most suitable. Since the sample rate requirements were not too severe, an integrating digital voltmeter which was externally programmable would easily meet these requirements. As a result, a Vidar 520 DVM was purchased and mated to the computer system with an LLL designed controller and 100 channel reed-relay scanner.

Phase II also called for the purchase of additional core memory for the PDP-8/I. However, in the intervening period of time from the initial justification (1 year), a more attractive method of providing this increased capacity was formulated. In reviewing the various tasks the computer system must perform in controlling a gas separation, several incidental, yet time consuming ones were apparent. For instance, control of the scanner and DVM required binary data to be converted to BCD control information, and BCD DVM data needed to be converted to binary-floating-point form for use in

the calculation routines. Also, I/O driver routines and certain closed loop digital control processes (such as temperature controllers) could be considered somewhat peripheral to the main processing routines. By executing these tasks in a small I/O processor, system throughput could be increased because of the parallel processing. Another positive factor was that at this point in time, the cost to LLL of a 4k PDP-8/L (including teletype) was just slightly higher than an additional 4k of core memory for the PDP-8/I. Thus, rather than purchase just an additional amount of memory, a processor and memory were added to the system. The new processor (a PDP-8/L) was connected to the PDP-8/I via a memory channel. On a hand-shaking basis (request-acknowledge), the inter-processor communication rate was approximately 50 kc.

The final major item to be acquired in Phase II was a disk memory. Since the software would require the swapping of blocks of code and data to and from core memory, a fixed-head disk with a worst-case access time of 34 ms and an average word transfer rate of at least 50 kc seemed the logical choice. A capacity of 256k words would provide storage for the program overlays and a minimal amount of data. To satisfy these requirements, a 262k word RS08 disk was purchased from DEC.

With the above described major equipment items on hand, and with the completion of the several LLL designed interfaces, the hardware necessary to implement the general system described in the preceding section on "initial design requirements" was complete. To adequately describe the LLL designed equipment, a more detailed description is necessary.

V. PHASE II HARDWARE SYSTEM

As noted previously, the dual processor system allowed parallel, simultaneous processing of I/O tasks and arithmetic tasks (i.e. peak recognition and integration). The arithmetic processor is an 8k PDP-8/I equipped with the hardware multiply/divide option, a positive I/O bus, and a 3-channel data-break multiplexer. One of the data-break channels is level converted to a negative I/O bus to be compatible with the RS08 disk. In addition, the PDP-8/I has the rather standard peripherals of an ASR-33 teletype and high-speed paper tape reader/punch.

The PDP-8/L I/O processor is a minimal machine equipped only with 4k of core memory, an ASR-33

teletype, and a single data break channel.

The analog inputs from each separation system are routed to a fully guarded, reed-relay, 100 channel scanner which can switch any one of the analog inputs to the analog output in one of three modes: random access, consecutive channel access (scan mode), or repetitive sampling of any single channel. The output of the scanner is digitized by a Vidar 520 integrating digital voltmeter. The result is three 12 bit words which are read by the I/O processor.

The digital output, decimal location, polarity, and function of the Vidar 520 IDVM are represented in 1248 BCD code. The DVM has full scale ranges of plus or minus 10 mV to 1000 V in six ranges. Each range can provide five significant digits with an additional over-range digit providing up to 300% over-range capability. A seventh range provides an auto-range capability. Three integration periods of 1.667, 16.67, and 166.7 ms are program selectable. The maximum sampling speed (a function of the resolution required) in a random channel scan is 70 channels/sec for resolution 1 (1.667 ms), 30 channels/sec for resolution 2 (16.67 ms), and 5.4 channels/sec for resolution 3 (166.7 ms). In consecutive conversions on the same channel, the rates are 108, 34, and 5.6 conversions per second. If a range change is required while in the auto-range mode, the conversion speed will be slowed from 6 to 36 ms per sample depending upon the amount of ranging done.

The analog outputs to the gas separation system are used to drive set-point controllers. Ten bit binary values that are derived from a computer program are converted to analog signals by a 7 channel, 10 bit digital to analog converter. Each channel has a 10 bit buffered DAC with a 0 to 10 volt output range and a settling time of 20 μ s to 1/2 LSB.

Digital I/O, which provides control and sensing of on-off functions for the gas separation system, is performed by a single master control interface and several remote stations. Up to eight remote stations can be connected to the master control interface by a daisy-chained data and control bus. Each remote station has eight groups of outputs and eight groups of inputs (each group contains 12 binary control signals). To change one of the binary outputs, one of eight output groups within one of the eight remote stations is selected. A

control bit pattern is then set up to change one or more of the 12 outputs in the selected group.

Remote station outputs can be from various dc drivers (i.e. 1 amp @ 55 VDC, 2.5 amp @ 55 VDC, 1 amp @ 250 VDC, and 4 amp @ 125 VDC) and isolated ac switches with zero-crossing turn on-off (500 VA rating). These various output drivers are modular in groups of four (i.e. each PC card contains four drive circuits).

The input groups of the remote station are addressed in a manner similar to the output groups. Again, eight groups of 12 binary on-off functions can be handled by each remote station. Seven of these groups are entirely passive, supplying status information to the computer only when interrogated. The eighth group of 12 can flag the computer with an interrupt whenever a change in state of one of the 12 inputs takes place. The input groups can monitor contact closures, dc voltage (on-off) and ac voltage (on-off).

Exchange of information between the PDP-8/I and the PDP-8/L is achieved through an asynchronous data link interface. The data link interface is a 3-cycle data-break device allowing bi-directional transfer of blocks of data. Although either machine may request a data transfer, the transfer does not begin until this request is acknowledged by the other computer. Through a hand-shaking (request-acknowledge) procedure, data words are transferred at roughly a 50 kc rate.

To facilitate setting sample rates, a programmable real-time clock was designed for the system. With this real-time clock, time intervals (interrupts) can be programmed to occur at a wide range of rates. Eight basic tick rates can be selected ranging from 1 tick/second to 1,000,000 ticks/second (also includes 60 ticks/second). In addition, interrupts can be programmed to occur at any integer number of ticks from 1 to 4096.

VI. SYSTEM SOFTWARE

The term system software as used in this context will be defined to mean those routines which actually operate the hardware. Useful functions can then be achieved by writing application routines which call these system routines.

The actual software drivers for the various devices are contained in the I/O processor sub-system.

This sub-system acts upon requests from the arithmetic processor to control the hardware. All requests to the I/O processor sub-system, which are in the same general format, and are uniquely identified by a code word, are made over the data link interface.

The DVM driver routine converts binary control information to the BCD format required by the DVM and stores this request in the first-in/first-out stack. As the DVM becomes available, the next request in the stack is executed. In a similar manner, DVM data is converted from raw BCD to binary-floating-point and stored in a stack until a request is made for it. Proper use of this stacking feature allows the arithmetic processor to be processing one sample while the next is being acquired.

The analog output driver is very simple since no stacking is required. Requests to change an analog variable are immediately honored.

For the digital I/O driver, a complete bit pattern representation of each binary function is maintained in the I/O processor. Thus, while certainly not closed loop, the status of both input and output lines may be immediately interrogated at any time. Additionally, the input status is updated periodically so that when a status request is made, a recent state of the digital I/O system is immediately available. In addition, interrupt requests from the remote stations are processed and made available to the arithmetic processor.

Teletype I/O using the I/O processor is also available. Both input and output functions are fully buffered several characters deep to allow for I/O and processing overlap.

Within the arithmetic processor, I/O requests are made to the I/O processor from the particular high-level language in use. Currently, FORTRAN is exclusively used on the gas analysis system for several reasons: 1) it is fast (approximately five times faster than FOCAL), 2) it is widely known by scientific personnel, 3) it can make use of a large sub-routine library, and 4) it is available in a very useful operating system package.

The various requests for tasks to be performed are communicated to the I/O processor by sub-routine calls. Each task has a different call statement. For example, the call to the DVM routine is made as follows:

```
CALL DVMST(IRNGE,NRES,NCHAN).
```

"IRNGE" is an integer from 1 to 7 inclusive representing the desired range of the DVM, "NRES" is an integer from 1 to 3 inclusive representing the desired resolution of the DVM, and "NCHN" is an integer from 0 to 99 inclusive representing the desired channel to be converted. To retrieve the converted data from the I/O processor the following call is made:

CALL DVMGT(IOK,XDATA)

"IOK" is an integer that indicates three status states:

- 1) -1 Error -- Data in "XDATA" not valid
- 2) 0 Data OK
- 3) 1 DVM Over-ranged -- Data in "XDATA" valid.

"XDATA" is a real variable containing the value of the converted channel in volts.

VII. SUMMARY

In the development of this small computer system, several factors were considered. The general types of input-output devices required were identified and the number of functions to be controlled

and/or sensed were estimated. By combining this information with the estimated data rates, processing algorithm, and available funds, specifications were formulated for the computer system. By developing system software along with the hardware, and by providing a well known high-level language, the user is more likely to view the total system as a useful tool rather than as an infinite manpower sink. While this computer system was designed specifically to operate a gas separation facility, it is a small, general process control system and could find applicability in other areas.

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