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A CAMAC SYSTEM FOR REMOTE DATA ACQUISITION

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A CAMAC SYSTEM FOR REMOTE DATA ACQUISITION*

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ABSTRACT

A CAMAC system has been developed at Lawrence Livermore Laboratory to interface with a remotely located computer. Two CAMAC compatible read-only controllers are described - one for single crate and one for multiple crate operation. A data display, serial bit stream generator, serial peak detector, 10 ns TIM, and a parallel input gate were developed for the system and are described.

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SUMMARY

Background

Because of the large number of data channels and high reliability required in the work at Lawrence Livermore Laboratory, instrumentation has always involved much manpower and an extensive support system. Systems involving a hundred wideband oscilloscopes are not uncommon. The resulting setup and turnaround times require a large inventory of equipment. In order to cut back on this costly process there has been a recent effort to replace the oscilloscopes with equipment which could directly input the data into a remotely located computer. The computer can then serve as a setup and calibration tool as well as a data processor. Because of the existing standard and the availability of commercial hardware, CAMAC was chosen as the means for implementing a data acquisition system.

Module Read Out System

The current CAMAC system at LLL operates in a read-only mode. A continuously scanning crate controller is used for single crate operation and a scanning branch driver is used for driving up to seven crates. Both scanners operate similarly except that they conform to the respective CAMAC standards where applicable. The branch driver is packaged in a double width CAMAC module but receives only power from the dataway and interfaces with one or more Type A controllers using a standard branch highway.

Scanner Operational Feature

The two scanners sequentially address each module location and read-out each data register which responds. A switch on the controller selects the reading of function F(0) or F(1). LLL designed modules respond to F(1) with a 16 bit identification word which indicates module type and the current status of operation. The 24 bit parallel data word is combined with crate, module number and address information into a 36 bit word and

converted to a serial PCM bit stream for transmission to a central computer. The parallel-to-serial converter is driven by a pseudo-random sequence generator which adds in an 11 bit alternating complement frame sync pattern every four data words. At the end of a complete system read-out, a special identification word is sent from the scanner which includes function information and the number of data words sent in the scan.

Parallel-To-Serial Encoder

A printed circuit board which is used in both scanners for parallel-to-serial conversion is also packaged in a single width CAMAC module. This module requests data using a Look-At-Me request and accepts 24 bits of data on the WRITE lines. The data is then converted to the bit stream described earlier. The bit stream rate is selectable from 19.2 KBPS to 1.228 MBPS.

CAMAC Data Reader

For maximum flexibility of operation, a data reader was designed to read the serial bit stream. A word to be displayed is selected from the bit stream either by the crate, module, and sub-address (CNA) information or by its position relative to the scanner word. The display contains the CNA in decimal form and 24 bits of data in a selectable representation - octal, 2421 BCD, 4221 BCD, and BINARY-TO-DECIMAL.

Serial Peak Detector

This module measures the peak amplitude for up to four consecutive high amplitude pulses. The amplitude values are logarithmically compressed and input to an A/D converter. A pulse is also generated at the peak time for input into a time interval meter.

Quad Gated 10 ns TIM

This module combines a commercially available time digitizer board with an LLL designed board using a 100 MHz gated clock to give four 10 ns time interval measurement circuits. The timing can be started by a common start or individually. Lacking a common start, each TIM is triggered from the first stop pulse received.

Dual High-Logic-Level-To-CAMAC Converter

This Parallel Input Gate accepts 16 bit words from devices such as digital counters or waveform digitizers. It has no buffer storage, so that data presented to the read lines is a continuous representation of the input. The input circuitry works over a wide range of binary logic levels.

Conclusion

The CAMAC concept is used at LLL to obtain high speed readout of a high density system. The initial system described is planned for minimum setup time and minimum human intervention. Several modules and controllers were designed to obtain the maximum flexibility of operation needed.