MASTER

Control System for 90° Analyzing Magnet

Clark Bergman and R. K. Hobbie

November, 1968

LEGAL NOTICE

This report was prepared as an account of Government sponsored work. Neither the United States, nor the Commission, nor any person acting on behalf of the Commission:

A. Makes any warranty or representation, expressed or implied, with respect to the accuracy, completeness, or usefulness of the information contained in this report, or that the use of any information, apparatus, method, or process disclosed in this report may not infringe privately owned rights; or

B. Assumes any liabilities with respect to the use of, or for damages resulting from the use of any information, apparatus, method, or process disclosed in this report.

As used in the above, "person acting on behalf of the Commission" includes any employee or contractor of the Commission, or employee of such contractor, to the extent that such employee or contractor of the Commission, or employee of such contractor prepares, disseminates, or provides access to, any information pursuant to his employment or contract with the Commission, or his employment with such contractor.

This report is Appendix I of a Ph.D. Thesis by Clark Bergman.

fy

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

PAGES 2 to 59
WERE INTENTIONALLY
LEFT BLANK

APPENDIX 1. ANALYZING MAGNET CONTROL SYSTEM

A. Introduction and General Description

High Voltage Engineering Corporation (HVEC) provided the analyzing magnet, its power supply, and an NMR fluxmeter and frequency counter for field measurement. To manually set the magnetic field for a particular energy, one first tunes the oscillator to the corresponding frequency and then adjusts the magnetic field until the NMR resonance occurs at that frequency. The Analyzing Magnet Control System consists of two subsystems which perform these tasks. They were designed to require minimum modification of the HVEC equipment and to allow one to select either a manual or automatic mode of operation. The resonance frequency corresponding to the desired beam energy is normally calculated by the CDC 3100 on-line computer and fed directly to the frequency control system. The frequency may be set to ± 100 Hz and the magnetic field to approximately ± 0.03 Gauss, which corresponds to ± 0.2 keV for a 20 MeV proton beam.

1. Frequency Control

The NMR oscillator has three remote tuning controls.

The first is a six-position range switch. The second is a coarse frequency control consisting of a motor-driven variable air capacitor. The capacitor is remotely set by a 25-turn potentiometer in the control room. The third is a fine tuning control provided by a voltage-variable capacitor diode, whose bias is normally adjusted with a ten-turn potentiometer. The frequency is measured approximately once a second and displayed to an accuracy of 10 Hz by a commercial gated counter.

A block diagram of the frequency control system is shown in Figure A1. The voltages provided by the control potentiometers just mentioned are obtained instead from digital to analog converters (DAC) by setting the fluxmeter MODE switch to AUTOMATIC. These DAC's are coupled to holding registers RC and RF (for coarse and fine control, respectively). Each time the frequency is measured, the difference between the desired and actual frequency is determined and the contents of RC or RF is modified by an amount proportional to this difference. The 20-bit register, F, contains the desired frequency to the nearest 100 Hz.

FREQUENCY CONTROL BLOCK DIAGRAM

Figure A1.

This information is gated to F from the computer whenever the energy is to be changed. The frequency difference is obtained in the following way: each time a frequency measurement cycle begins, the content of F is gated into a 21-bit register, D. The pulse train from the input to the 100 Hz decade of the frequency counter is then fed to D, which functions as a down-counter. Thus, at the end of the measurement cycle, D contains the difference between the desired and actual frequencies. If this difference is negative, D is modified so that the most significant bit represents the sign, and the remaining bits the magnitude, of the frequency difference.

In order to correct the oscillator frequency with this difference, the D register is divided into upper (coarse) and lower (fine) parts, DC and DF, whose contents are used to correct RC and RF respectively. If $(DC) \neq 0$, then DC is counted to zero while RC is incremented or decremented the same number of times. After the motor which drives the variable capacitor stops rotating, a new cycle is begun. If $(DC) = 0$ and $(DF) \neq 0$, then the content of DF is used to modify the

content of RF in a like manner. Any borrow or carry generated in RF is transmitted to RC.

Rotary switches are used to select the division between DF and DC (RANGE), the least significant bit of DF (ACCURACY), and the number of bits associated with RF (Fine DAC Resolution). These switches effectively set the gain of the feedback system. In practice, they have optimal positions which remain fixed over frequency intervals exceeding 3 MHz for all but the lowest frequencies. There is a one-to-one correspondence between the RANGE switch and the range the NMR Fluxmeter is on. The ACCURACY switch can be set to 0.1 kHz except above 35 MHz. The Fine DAC resolution is adjusted so that the fine step size is slightly less than the accuracy set by the ACCURACY switch. Too coarse a resolution results in "hunting", while a resolution much finer than needed increases the settling time of the system.

2. Field Control

The magnet power supply provided by HVEC is controlled by the voltage from a forty-turn potentiometer

connected across a stable reference voltage. This is shown schematically in Figure A2. The feedback loop adjusts the magnet current so that the voltage developed across the 32 milliohm series resistor just cancels the voltage output of the potentiometer. This single control was intended to provide a monotonic field variation in order to minimize the effects of differential hysteresis in the magnet. The potentiometer is driven by a 10:1 gear reduction unit, and some backlash and mechanical instability were present. It was finally decided that it was not worth the expense to try to make an automatic unit with a single stage of control having the necessary stability. The motor which originally drove the potentiometer for rapid field changes was replaced by a digital stepping motor. Each step corresponds to about 2 Gauss (40 mA). For finer control of the magnet current, an auxiliary current of up to 70 mA is driven through the reference resistor in the opposite direction to the desired change in magnet current. This is a most convenient way to introduce the control signal while minimizing noise and stability problems. This current is controlled by a 7-bit counter, C, and a DAC. With this

Figure A2.

scheme the field can be set to approximately ± 0.03 Gauss.

The field control system requires four external signals:

- 1) The NMR resonance signal from the oscillator;
- 2) The 60 Hz signal which modulates the magnetic field at the NMR probe;
- 3) A signal from the frequency control system to activate the field control system when the frequency is correct; and
- 4) A signal from the frequency control system giving the direction of the last frequency change which occurred.

Initially, one must manually locate the resonance; thereafter the field control system is capable of following any arbitrary frequency change. With the analyzing magnet MODE switch set to AUTOMATIC, power is applied to the stepping motor and the DAC is connected to the reference resistor as shown in Figure A2. The system works best with the amplitude of the modulating field at a maximum.

To understand the operation of the field control system, assume first that the NMR resonance occurs within the range of the 60 Hz modulating field, and that the frequency is correct. Logical decisions are made and fine corrections initiated only during the rising portion of the modulating field. Now, if the resonance occurs before the modulating signal crosses zero, the DC field is high and C is decremented at a preset rate (approximately 250 μ sec per step) until the zero crossing is reached. If the resonance occurs after the zero crossing, the counter is incremented at the same rate from the time of the zero crossing until resonance is reached. After each correction, further corrections are inhibited for 90 milliseconds to allow the field to settle. Should the frequency be changed deliberately, the sign of the frequency error is stored and the field control loop disabled until the frequency is again correct. At that time, if the resonance is no longer present, the stepping motor steps at 0.7 Hz in the direction determined by the sign of the original frequency error. This continues until the resonance is found, when the system reverts to the procedure described above. Borrows

or carries generated by the C register are used to step the motor once in the appropriate direction. Should the frequency drift once it has been set, the magnetic field will not be altered until the frequency is again correct.

B. Operation

The following is a step-by-step procedure which may be followed to get the Analyzing Magnet Control System into operation:

- 1) Depress the START switch on the left side of the Oscillator Controller chassis. One has to pull the chassis out slightly to do this.
- 2) Set the RANGE switch on the Oscillator Controller to correspond to the position of the range switch on the NMR fluxmeter.
- 3) The ACCURACY switch may normally be set to $\pm .1$ kHz below 35 MHz.
- 4) Set the Fine DAC resolution to the value given in Table A1. The switch which controls this is located at the rear of the computer racks, directly behind the Oscillator

Controller chassis.

- 5) Call the computer program ENERGY(E,A,Z).
E is the desired energy in MeV, A is the mass of the projectile in amu, and Z is the charge in units of e. Any variable given as zero in a later call to ENERGY is assumed to take on the last nonzero value given.
- 6) Switch the frequency control system to AUTOMATIC (switch on the NMR fluxmeter).
- 7) When the frequency has settled to the proper value, locate the NMR resonance manually.
- 8) Switch the 90 degree magnet controller to AUTOMATIC. Power for the Magnet Controller, located just below the frequency counter, is turned on with the switch located on its front panel.

The signal-to-noise ratio of the NMR signal presently limits the usefulness of the field control system to the frequency range 12.4 to 38.3 MHz (6.5 to 65 MeV protons or alpha particles). Table A1 gives

the optimal Fine DAC resolution over this range. The frequency control system can be used by itself to set the frequency in the range 6.4 to 80 MHz.

TABLE A1.

Optimal Fine DAC Resolution

NMR fluxmeter range	RANGE switch	Freq. interval	Fine DAC res.
2.9 - 5.0 kG	12.4 - 21.3 MHz	12.4 - 14.8 MHz	6 bits
		14.8 - 17.6	7
		17.6 - 21.3	8
5.0 - 9.0	21.3 - 38.3	21.3 - 26.0	7
		26.0 - 31.5	8
		31.5 - 38.3	9

C. Detailed Description

Table A2 lists the title and drawing number of all drawings associated with the Analyzing Magnet Control System. The system is constructed with a mixture of Computer Control Corporation (CCC) digital circuits, Digital Equipment Corporation (DEC) analog and digital

TABLE A2.

Analyzing Magnet Control System Drawings

<u>Dwg. No.</u>	<u>Title</u>
*84-0501	System Block Diagram
*84-6020	Oscillator Controller - Chassis Schematic
*84-6021	Oscillator Controller - Power Connections
*84-6022	Oscillator Controller - Interfacing
*84-6023	Oscillator Controller - Frequency and Difference Reg. - 1
*84-6024	Oscillator Controller - Frequency and Difference Reg. - 2
*84-6025	Oscillator Controller - Control Logic - 1
*84-6026	Oscillator Controller - Control Logic - 2
*84-6027	Oscillator Controller - RANGE and ACCURACY sw., Indic. Lamps
84-6028	Oscillator Controller - + 6 Volt (4 Amp) Regulator
84-6029	Oscillator Controller - - 6 Volt (1 Amp) Regulator
84-6030	Oscillator Controller - Trnsmters and Rcvrs with ± 6V Supp.
84-6031	Oscillator Controller - Two Monostables
*84-6032	Coarse and Fine Cont. DAC's - DAC's
*84-6033	Coarse and Fine Cont. DAC's - Up/Down Counting Registers
*84-6034	Coarse and Fine Cont. DAC's - Fine DAC Res. and Gates
*84-6035	Isolation Amplifiers
84-6036	Oscillator Tuning Motor Status Indicator
*84-6037	Frequency Counter Interface - Block Diagram
84-6038	Frequency Counter Interface - Special Circuits
*84-6039	Modification of NMR Fluxmeter
*84-6041	Magnet Controller - Power, Indic. Lamps, Circ. Card Loc.
*84-6042	Magnet Controller - Logic - 1
*84-6043	Magnet Controller - Logic - 2
*84-6044	Magnet Controller - 7 Bit DAC with Up/Down Register
*84-6045	Magnet Controller - Modification of Analyz. Mag. System
84-6046	Magnet Controller - STM 1800 SloSyn Translator
84-6047	Magnet Controller - 90 Degree Phase Shift and Em. Foll.
84-6048	Magnet Controller - Emitter Follower
84-6049	Magnet Controller - 3 Schmitt Triggers
84-6050	Magnet Controller - 2 Multivibrators

* Drawings which appear at the end of Appendix 1.

circuits, and some homemade circuits. The operation of the CCC and DEC circuits are described in References 24 and 25 respectively.

Logic level conventions followed are given in Table A3. One observes that except for the Digital Output Connector (DOC), logical "zero" is always ground potential, and logical "one" is either a positive or negative voltage.

TABLE A3.

Logic Level Conventions

	Logical 0	Logical 1
CCC	0 Volts	+ 6 Volts
DEC	0	- 3
DOC	- 3	0

Some of the basic logic symbols which appear in the drawings are illustrated in Figure A3. An attempt has been made to conform to Military Standard (MIL-STD-806) logic symbols as much as possible. A notable exception to this is that DEC circuits employing the "DCD" gate have been drawn similar to the way they appear

BASIC LOGIC SYMBOLS

Figure A3.

in the DEC manual.²⁵⁾ In the interest of clarity, the function of the circle in the diagrams should be discussed. The large circle with a bar over it represents both logical and electrical inversion: the input signal to the inverter is transformed to its logical and electrical complement at the output. The small circle used at the input or output of more complex circuits represents a logical inversion. These circles are used to enable one to consider the basic logic components as operating with logically true inputs and outputs. For example, the basic "NAND" gate has a false output when all inputs are logically true; otherwise the output is true. Schematically this is represented as an "AND" gate, whose output is true only when all inputs are true followed by a logical inversion. The same electrical gate functions as a "NOR" gate for complementary logic. Within the framework of the logic conventions adopted here, the "NOR" function is represented by an "OR" gate with logical inversion at the inputs. One may then think of the OR gate in terms of true logic levels. Another example of the use of the small circle is provided by the direct set inputs of

CCC flip flops. Electrical ground (logical "zero") activates these inputs. By placing a logical inversion at these inputs, one may think of the flip flops as being activated by logically true signals.

1. Frequency Control Logic

Figure A4 shows the timing relationships of the most important signals used in this system. True signals are high (+6V) and false ones low (ground). The basic timing cycle is shown at the top, and important signals related to coarse and fine frequency corrections are shown below. Breaks in the time axis occur during the 1.3 second DELAY (M061) and the 90 μ sec RESET (M071) pulses.

In order to start the discussion, assume that the frequency counter is in a measurement cycle. M081 generates a 100 nanosecond pulse each time the frequency counter increments by one in the 0.1 kHz decade. These pulses are used to scale the D register backwards. Approximately 17 μ sec after the measurement is completed the PRINT COMMAND (X006) pulse appears. This initiates the frequency correction cycle by clearing Frequency

Counter Running (FCR, K061). This in turn triggers M011. During the time that M011 is true, the sign of the contents of the D register is inspected. A PRINT COMMAND pulse will be generated by RESET if the frequency counter is running when RESET occurs. If this happens, both K060 and K061 are forced to be logical "one" during the overlap of RESET and PRINT COMMAND (2 μ sec). To avoid starting the correction cycle in this situation, M011 is triggered by $K061 \otimes T006$. (The logical product of A and B is denoted by $A \otimes B$ and the logical sum by $A \oplus B$.)

If the content of the D register is negative (D211 set), then D021 to D201 are complemented at the trailing edge of M011. COUNT ENABLE (P001) is required to prevent the propagation of borrow pulses when D is complemented. The combination T001, T002, and C022 delay the triggering of M021 by about 100 nanoseconds, insuring that levels changed on the trailing edge of M011 will have settled to their proper values before they are sampled. M021 triggers M061, initiating a 1.3 sec delay. During the time that M021 is true, the system determines whether or not a frequency correction is necessary.

The FREQUENCY SET (K041) flip flop is set if CZERO (X) FZERO is true, and cleared if either CZERO or FZERO is false. If CZERO (T027) is true, the Coarse Correction (CC, K071) flip flop is set on the trailing edge of the CLOCK (M041) pulse. If CZERO and FZERO (T041) are true, the Fine Correction (FC, K081) flip flop will be set on the trailing edge of the clock pulse. In either of these cases the appropriate part of the D register (DC of DF) is Counted To Zero (CTZ), starting with the next CLOCK pulse. T016 and T031 drive the Coarse and Fine DAC registers respectively during the CTZ part of the correction cycle. When the content of this subregister reaches zero the corresponding correction flip flop, CC or FC, is immediately cleared and the correction is terminated.

When M061 again becomes false, K051 is set as soon as MOTOR RUNNING (X007) is true. The inputs to T003 (M060 and K051) are then true and the RESET monostable is triggered. K051 is used to buffer information about the status of the motor driving the variable air capacitor, because the circuit which detects the status sometimes oscillates when the motor is nearly stopped.

This would cause multiple RESET pulses if X007 were fed directly to T003. RESET transfers the content of the F register to D and resets the frequency counter. When RESET is completed, the frequency counter immediately begins a measurement cycle.

In order to change the frequency, the computer transfers the new frequency to the Display Driver along with the proper Route Line connect code (Route line 2 = -3 V, Route line 3 = 0 V). A ready to Transfer (RTT) accompanied by the proper connect code is honored immediately, except when RESET is true. In the latter case a delay of up to 90 μ sec occurs. When RTT is accepted, M091 fires, causing the information on the DOC data lines to be transferred to F. Transfer Accepted (TA, L024) is a 3 μ sec pulse generated 2 μ sec later which releases the Display Driver. The capacitor C021 attenuates transients caused by TA which otherwise trigger M091 a second time, causing false information to be transferred.

The START switch is used to start the CLOCK and to trigger RESET when power has just been turned on.

2. Field Control Logic

Figure A5 is a timing diagram for the most important signals used to control the field of the analyzing magnet. True signals are low ($-3V$) and false ones high (ground). A source of possible confusion is a 180 degree phase difference between the modulation field, $B(t)$, and the 60 Hz voltage used to provide this field. To avoid confusion, the following discussion refers exclusively to $B(t)$, even though it is the 60 Hz signal which is used in the system.

The operation of this system depends upon a knowledge of the sign of both $B(t)$ and $B'(t)$. The circuit E001 generates $B'(t)$ by phase shifting $B(t)$ by 90 degrees. Trigger circuits T001 and T002 provide the signs of $B(t)$ and $B'(t)$ respectively. Noise often causes T001 and T002 to multiple pulse when the input signals cross the trigger thresholds. Flip flops K151 (POSITIVE) and K161 (ANALYZE) eliminate this jitter. Gates R027 to R030 insure that K150 and K161 follow the sequence of states given in Table A4. Corrections to the magnetic field, other than a search for the NMR resonance, are made only when ANALYZE is true.

TIME, IN SIXTIETHS OF ONE SECOND

FIELD CONTROL TIMING DIAGRAM

SHOWS THE SIGNALS RELATED TO A MAGNETIC
FIELD CORRECTION IN WHICH THE FIELD IS INCREASED.

Figure A5.

TABLE A4.

Truth Table for POSITIVE and ANALYZE

B(t)	B'(t)	POSITIVE (K150)	ANALYZE (K161)
-	+	false	true
+	+	true	true
+	-	true	false
-	-	false	false

Positive oscillations of the NMR resonance signal are detected by the trigger circuit T003, whose threshold is set above the noise level. The flip flop K081 (RESONANCE) is set during each cycle at the leading edge of ANALYZE. The next positive going pulse from T003 clears K081 if ANALYZE is still true. If the resonance does not occur during ANALYZE, K081 remains set and K091 (OUT of resonance) is set on the leading edge of ANALYZE. K081 may not be cleared except during ANALYZE, while K091 is cleared as soon as the resonance occurs.

The state of the magnetic field is given by K131 (BSET). If W001 (Frequency SET) is true, K091 (OUT of resonance) is false, and no corrections to the field

were made during the last ANALYZE cycle (R026 false during this period), then BSET is true. A change in any one of these conditions immediately clears BSET. The direction of changes in the resonance frequency are stored by K101 (B field LOW). The magnet is stepped in the direction given by K101 if FSET (X) OUT is true. One is therefore cautioned to allow time for the field to settle after each frequency change before making a further change.

The details of a field correction in which the DC field is above the resonance frequency will now be discussed. The timing relationships of pertinent signals is shown in Figure A5. The resonance is assumed to occur at some point during each modulation cycle (K081 cleared). Corrections are made only when ANALYZE is true. When the field is high, K081 is cleared before POSITIVE becomes true. This opens R020 which sets K141, disabling R023. R026 opens and, if R033 is enabled by R031, the gated clock (C001) steps the DAC register at a rate of 4 kHz. The effect of jitter in the time of the zero crossing of $B(t)$ is eliminated by the .022 μ f capacitor on the output of

R026. No correction is made if the resonance occurs within 10 μ sec of the zero crossing. C001 is stopped when POSITIVE becomes true. C001 triggers the monostable M003, which in turn triggers M004 8 milliseconds later. M004 causes R031 to close R033 for approximately 80 milliseconds. This inhibits further corrections while the field is settling.

A correction of the opposite sign is very similar. In this case, K141 is not set during ANALYZE (X) POSITIVE and R023 opens when POSITIVE becomes true. C001 then steps the DAC register forward until K081 is cleared by the resonance.

ANALYZING MAGNET CONTROL SYSTEM
BLOCK DIAGRAM
SYSTEM INTERCONNECTIONS
84-0501

ANALYZING MAGNET CONTROL SYSTEM
OSC. CONTROLLER PWR. CONNECTIONS
±6V RECTIFIERS & REGULATORS
84-6021

[illegible]

NOTE: M09H, M1G1 HOMEMADE
SEE DWG. 84-6031

TRANSMITTERS

(FREQ. SET) → K041 → X001 (119, 18, 20) → J906-4, J902-14, J906-7, J902-7

(RESET) → M071 → X002 (119, 2, 4) → J906-12, J902-12, J906-5, J902-5

(FREQ. INC.) → K030 → X003 (119, 8, 10) → J906-13, J902-13, J906-6, J902-6

RECEIVERS

J902-4, J906-4, J902-11, J906-11 → X004 (118, 24, 28) → T014 (20) → J905-25 → L025 (405B) → J905-26, J907-30 → J908 BNC ON FRONT PANEL → SCALE FREQUENCY

J902-1, J906-1, J902-8, J906-8 → X005 (118, 14, 12) → J905-26, J907-30 → J908 BNC ON FRONT PANEL → SCALE FREQUENCY

J902-2, J906-2, J902-9, J906-9 → X006 (118, 6, 4) → PRINT COMMAND

J902-3, J906-3, J902-10, J906-10 → X007 (118, 22, 20) → MOTOR RUNNING

SET F

(RESET) M070 → T054 (216, 13, 16, 9) → T055 (220, 3, 4) → T053 (218, 10, 16) → T052 (218, 9, 16) → T054

25 2.0 C021

M091 (120, 16, 14) → M090 (2μs) → P005 (109, 24, 13) → P006 (109, 28, 25) → SET F

M101 (20, 31) → M100 (3μs) → SET F

CONNECT CODE:
R.L. 2 = 0
R.L. 3 = 1

TRANSFER ACCEPTED

30

[illegible]

DIFFERENCE REGISTER
BIT 21 (SIGN)

-90-

FREQUENCY REGISTER										DIFFERENCE REGISTER									
BIT	FXXI	FXXO			DXXI	DXXO					R1XX	R2XX		R3XX					
XX	LOC.	LOC.	SET	CLEAR	LOC.	LOC.	SET	CLEAR	BORROW	CNT. ENAB.	LOC.	LEV. CTVR.	LOC.	SET F	R1XX	LOC.	SET F	LEV. CTVR.	
01	107-22	107-20	R201-18	R301-24	215-6	215-8	R801-10	R901-32	R701-28	P001-26,30	105-21	L001-22	108-26	P005-23	R101-24	108-20	P005-23	L001-22	
02	107-30	107-28	R202-26	R302-32	215-12	215-14	R802-16	R902-24	R702-20	* -18,22	105-27	L002-28	108-31	* -29	R102-27	108-19	* -23	L002-21	
03	107-6	107-4	R203-2	R303-8	215-5	215-3	R803-1	R903-23	R703-27	* -29,25	105-32	L003-29	108-30	* -29	R103-32	108-28	* -29	L003-25	
04	107-14	107-12	R204-10	R304-16	215-11	215-9	R804-7	R904-13	R704-17	* -19,15	105-26	L004-25	106-10	* -6	R104-8	106-2	* -6	L004-4	
05	104-22	104-20	R205-18	R305-24	211-6	211-8	R805-10	R905-32	R705-28	* -26,30	105-9	L005-10	106-3	* -6	R105-1	106-7	* -6	L005-5	
06	104-30	104-28	R206-26	R306-32	211-12	211-14	R806-16	R906-24	R706-20	* -18,22	105-15	L006-16	106-18	* -13	R106-16	106-12	* -13	L006-14	
07	104-6	104-4	R207-2	R307-8	211-5	211-3	R807-1	R907-23	R707-27	* -29,25	105-20	L007-17	106-9	* -13	R107-11	106-17	* -13	L007-15	
08	104-14	104-12	R208-10	R308-16	211-11	211-9	R808-7	R908-13	R708-17	* -19,15	105-14	L008-13	106-26	* -25	R108-24	106-20	* -23	L008-22	
09	104-11	104-13	R209-15	R309-9	206-6	206-8	R809-10	R909-32	R709-28	* -26,30	105-6	L009-7	106-31	* -29	R109-27	106-19	* -23	L009-21	
10	104-3	104-5	R210-7	R310-1	206-12	206-14	R810-16	R910-24	R710-20	* -18,22	105-4	L010-3	106-30	* -29	R110-32	106-28	* -29	L010-25	
11	104-27	104-29	R211-31	R311-25	206-5	206-3	R811-1	R911-23	R711-27	* -29,25	102-21	L011-22	103-10	P006-6	R111-8	103-2	P006-6	L011-4	
12	104-19	104-21	R212-23	R312-17	206-11	206-9	R812-7	R912-13	R712-17	* -19,15	102-27	L012-28	103-3	* -6	R112-1	103-7	* -6	L012-5	
13	101-22	101-20	R213-18	R313-24	204-6	204-8	R813-10	R913-32	R713-28	* -26,30	102-32	L013-29	103-18	* -13	R113-16	103-12	* -13	L013-14	
14	101-30	101-28	R214-26	R314-32	204-12	204-14	R814-16	R914-24	R714-20	* -18,22	102-26	L014-25	103-9	* -13	R114-11	103-17	* -13	L014-15	
15	101-6	101-4	R215-2	R315-8	204-5	204-3	R815-1	R915-23	R715-27	* -29,25	102-9	L015-10	103-26	* -23	R115-24	103-20	* -23	L015-22	
16	101-14	101-12	R216-10	R316-16	204-11	204-9	R816-7	R916-13	R716-17	* -19,15	102-15	L016-16	103-31	* -29	R116-27	103-19	* -23	L016-21	
17	101-11	101-13	R217-15	R317-9	301-6	301-8	R817-10	R917-32	R717-28	* -26,30	102-20	L017-17	103-30	* -29	R117-32	103-28	* -29	L017-25	
18	101-3	101-5	R218-7	R318-1	301-12	301-14	R818-16	R918-24	R718-20	* -18,22	102-14	L018-13	202-26	* -23	R118-24	202-20	* -23	L018-22	
19	101-27	101-29	R219-31	R319-25	301-5	301-3	R819-1	R919-23	R719-27	* -29,25	102-6	L019-7	202-31	* -29	R119-27	202-19	* -23	L019-21	
20	101-19	101-21	R220-23	R320-17	301-11	301-9	R820-7	R920-13	R720-17	* -19,15	102-4	L020-3	202-30	* -29	R120-32	202-28	* -29	L020-25	

BIT	R4XX		R5XX		C0XX		R6XX		R7XX				R8XX			R9XX		
XX	LOC.	DYYO	LOC.	R4XX	LOC.	LOC.	DYYI	R5XX	LOC.	R6XX	COMPL.	CTZ	LOC.	SET D	FXXI	LOC.	SET D	FXXO
01								SEE DWG.					214-2	P003-6	F011-4	214-10	P003-6	F010-8
02	218-6	D010-7	218-4	R402-3	210-4	212-21	D011-22	R502-24	113-31	R602-27	P002-29	T048-28	214-7	" -6	F021-5	214-3	" -6	F020-1
03	212-27	D020-28	212-32	R403-29	210-3	212-26	D021-23	R503-25	113-25	R603-24	" -22	T049-23	214-12	" -13	F031-14	214-18	" -13	F030-16
04	212-9	D030-10	212-15	R404-16	210-6	212-20	D031-19	R504-17	213-31	R604-27	" -29	T050-28	214-17	" -13	F041-15	214-9	" -13	F040-11
05	212-14	D040-13	212-6	R405-7	210-5	212-4	D041-1	R505-3	213-25	R605-24	" -22	T051-23	214-20	" -23	F051-22	214-26	" -23	F050-24
06	208-21	D050-22	208-27	R406-28	210-8	208-32	D051-31	R506-29	213-20	R606-19	" -17	T043-18	214-19	" -23	F061-21	214-31	" -29	F060-27
07	208-26	D060-25	208-9	R407-12	210-7	208-15	D061-18	R507-16	213-15	R607-14	" -12	T044-13	214-28	" -29	F071-25	214-30	" -29	F070-32
08	208-20	D070-17	208-14	R408-13	210-10	208-6	D071-5	R508-7	213-10	R608-9	" -7	T045-8	209-20	" -23	F081-22	209-26	" -23	F080-24
09	208-4	D080-3	207-21	R409-22	210-9	207-27	D081-30	R509-28	213-5	R609-4	" -2	T046-3	209-19	" -23	F091-21	209-31	" -29	F090-27
10	207-32	D090-29	207-26	R410-25	210-12	207-9	D091-12	R510-10	207-15	R610-16	" -18		209-28	" -29	F101-25	209-30	" -29	F100-32
11	207-20	D100-17	207-14	R411-13	210-11	207-6	D101-5	R511-7	207-4	R611-3	" -1		209-2	P004-6	F111-4	209-10	P004-6	F110-8
12	205-21	D110-22	205-27	R412-28	210-14	205-32	D111-31	R512-29	205-26	R612-25	" -23		209-7	" -6	F121-5	209-3	" -6	F120-1
13	205-9	D120-10	205-15	R413-16	210-13	205-20	D121-19	R513-17	205-14	R613-13	" -11		209-12	" -13	F131-14	209-18	" -13	F130-16
14	205-6	D130-7	205-4	R414-3	210-16	203-21	D131-24	R514-22	203-27	R614-28	" -30		209-17	" -13	F141-15	209-9	" -13	F140-11
15	203-32	D140-29	203-26	R415-23	210-15	203-9	D141-12	R515-10	203-15	R615-16	" -18		108-12	" -13	F151-14	108-18	" -13	F150-16
16	203-20	D150-17	203-14	R416-13	210-18	203-6	D151-5	R516-7	203-4	R616-3	" -1		108-17	" -13	F161-15	108-9	" -13	F160-11
17	201-21	D160-22	201-27	R417-28	210-17	201-32	D161-31	R517-29	201-26	R617-25	" -23		202-2	" -6	F171-4	202-10	" -6	F170-8
18	201-9	D170-10	201-15	R418-16	210-20	201-20	D171-19	R518-17	201-14	R618-13	" -11		202-7	" -6	F181-5	202-3	" -6	F180-1
19	201-6	D180-7	201-4	R419-3	210-19	302-21	D181-24	R519-22	302-27	R619-28	" -30		202-12	" -13	F191-14	202-18	" -13	F190-16
20	302-32	D190-29	302-26	R420-25	210-22	302-9	D191-12	R520-10	302-15	R620-16	" -18		202-17	" -13	F201-15	202-9	" -13	F200-11

NOTE: SEE DWG. 84-6023 FOR SCHEMATIC.

TERM LOCATIONS LISTED AS "SOCKET-PIN".

INPUTS LISTED AS "TERM-PIN".

ANALYZING MAGNET CONTROL SYSTEM
OSCILLATOR CONTROLLER
FREQUENCY & DIFFERENCE REGISTERS-2
84-6024

The diagram illustrates the logic for setting the frequency. It includes the following components and connections:

- Inputs:** (RESET) MO71, (SET F) TO54, TO58, KO25, MO11, D210, D211, and FREQ. INCREASED.
- Logic Gates:**
 - AND gate T056: Inputs 19 (from (RESET) MO71) and 17 (from KO11 pin 12). Output 20 (pin 302) connects to T057 pin 13.
 - AND gate T057: Inputs 13 (from T056) and 11 (from MO11). Output 5 (pin 302) connects to T058 pin 14.
 - AND gate T058: Inputs 14 (from T057) and 15 (from D211). Output 21 (pin 302) connects to KO31 pin 21.
 - AND gate T059: Inputs 21 (from T058) and 17 (from KO31 pin 17). Output 19 (pin 302) connects to KO30 pin 19.
- Flip-Flops:**
 - T056: Inputs 16 (from (SET F) TO54) and 18 (from KO11 pin 18). Output 12 (pin 303) connects to T056 pin 17.
 - T057: Inputs 1 (from T056 pin 20) and 3 (from KO20 pin 3). Output 5 (pin 302) connects to T058 pin 14.
 - T058: Inputs 14 (from T057) and 15 (from D211). Output 21 (pin 302) connects to KO31 pin 21.
- Counters:**
 - KO11: Inputs 16 (from (SET F) TO54) and 18 (from KO11 pin 18). Output 12 (pin 303) connects to T056 pin 17.
 - KO21: Inputs 31 (from T056 pin 20) and 27 (from TO58). Output 5 (pin 303) connects to T057 pin 13.
 - KO20: Inputs 25 (from KO25) and 3 (from T057 pin 5). Output 3 (pin 303) connects to T057 pin 13.
 - KO31: Inputs 21 (from T058) and 17 (from KO31 pin 17). Output 11 (pin 303) connects to T058 pin 14.
 - KO30: Inputs 19 (from T059) and 15 (from D211). Output 9 (pin 303) connects to T059 pin 17.

CONTROL LOGIC-1
84-6025

ANALYZING MAGNET CONTROL SYSTEM

OSCILLATOR CONTROLLER

CONTROL LOGIC-2

84-6026

RANGE SWITCH

POSITION RANGE

1	6.4 - 12.4 mHz
2	12.4 - 21.3
3	21.3 - 38.3
4	38.3 - 80.9

ACCURACY SWITCH

POSITION

ACCURACY

1	0.1 kHz
2	0.2
3	0.4
4	0.8
5	1.6

INDICATOR LAMPS

ANALYZING MAGNET CONTROL SYSTEM

OSCILLATOR CONTROLLER

RANGE AND ACCURACY SWITCHES, INDICATOR LAMPS

84-6027

NOTE: 250Ω, 5W, 5% RESISTOR MOUNTED BETWEEN PINS AB & AE ON A704 REGULATED SUPPLY CARD.

ANALYZING MAGNET CONTROL SYSTEM
COARSE & FINE CONTROL DAC'S

84-6032

B → UP ENABLE
D → DOWN ENABLE

COARSE CONTROL REGISTER

BIT	LOC.	OUTPUT		INPUTS			
		O	I	A	B	C	D
1	202	C010	C011	R011	GND.	OPEN	OPEN
2	203	C020	C021	C011	R005	C010	R001
3	204	C030	C031	C021	R005	C020	R001
4	205	C040	C041	C031	R005	C030	R001
5	206	C050	C051	C041	R005	C041	R001
6	207	C060	C061	C051	R005	C050	R001
7	208	C070	C071	C061	R005	C060	R001
8	209	C080	C081	C071	R006	C070	R002
9	210	C090	C091	C081	R006	C080	R002
10	211	C100	C101	C091	R006	C090	R002
11	212	C110	C111	C101	R006	C100	R002

FINE CONTROL REGISTER

BIT	LOC.	OUTPUT		INPUTS			
		O	I	A	B	C	D
1	223	F010	F011	S001	GND.	OPEN	OPEN
2	222	F020	F021	S003	R007	S002	R003
3	221	F030	F031	S005	R007	S004	R003
4	220	F040	F041	S007	R007	S006	R003
5	219	F050	F051	F041	R007	F040	R003
6	218	F060	F061	F051	R007	F050	R003
7	217	F070	F071	F061	R007	F060	R003
8	216	F080	F081	F071	R006	F070	R002
9	215	F090	F091	F081	R006	F080	R002

ANALYZING MAGNET CONTROL SYSTEM
COARSE & FINE CONTROL DAC'S
UP/DOWN COUNTING REGISTERS

84-6033

(COUNT FINE) L002

POSITION	RESOLUTION, * BITS
1	6
2	7
3	8
4	9

The schematic diagram illustrates the control logic for the 122 channel selector. It features a 123-pin connector at the top with the following inputs:

- J910-D: D211 FROM OSC. CONT.
- J912A: +10V (1/4 A.)
- J912B: -15V (1 1/2 A.)
- J912C: Ground

These inputs are connected to a logic unit (L001) and a series of relays (R001-R007). The 122-pin connector has two sets of outputs:

- DOWN ENABLE: M, E, H, K
- UP ENABLE: P, S, U

The timing diagram for the coarse counter section shows the following components and signals:

- Counters:** L002 (R), L003 (K), M001 (M), M002 (V), RO08 (D), RO09 (H), RO10 (R), and RO11 (L).
- Inputs:** J910-A (V), J910-B (P), F091 (E), F090 (N), and R002 (P).
- Outputs/Connections:** L002 (R) to L003 (K), L003 (K) to RO10 (R), M001 (M) to RO08 (D), M002 (V) to RO09 (H), RO08 (D) to RO10 (R), RO09 (H) to RO10 (R), RO10 (R) to RO11 (L).
- Timing Elements:** M001 and M002 are labeled with $1\mu s$ and have internal timing diagrams (J-K and S-T respectively).
- Counters:** RO10 and RO11 are labeled "COUNT COARSE".

84-6034

NOTE: J107 & J117 ARE LOCATED IN THE FREQUENCY COUNTER (CMC MOD 738A)

CIRCUIT SCHEMATICS:

J1003-SEE DWG. 84-6038
J1004- " " "
J1005- " " 84-6030
J1006- " " "

**ANALYZING MAGNET CONTROL SYSTEM
FREQUENCY COUNTER INTERFACE
BLOCK DIAGRAM
84-6037**

■ NMR FLUXMETER
SEE D-CON - 351-1

RELAY LOCATED
FREQ. COUNTER
INTERFACE
DWG. 84-6037

ANALYZING MAGNET CONTROL SYSTEM MODIFICATION OF NMR FLUXMETER 84-6039

INDICATOR LAMPS

CIRCUIT CARD ASSIGNMENTS

LOC.	CARD TYPE	LOC.	CARD TYPE
201	A702	101	A702
202	R201	102	A601
203	R201	103	A601
204	R201	104	A601
205	R201	105	EMIT. FOLL.
206	R201	106	SPARE
207	R201	107	SPARE
208	R202	108	R401
209	R113	109	R302
210	R203	110	R113
211	R107	111	SCHMITT TRIG.
212	R111	112	EM. FOLL.
213	R001	113	W510
214	MULTIVIB.	114	R302
215	R202	115	R107
216	R203	116	R111
217	SPARE	117	R001
218	SPARE	118	R111
219	W050	119	R113
220	W700	120	W601

STM 1800 - SLOSIN TRANSLATOR
(SUP. ELEC. CO.)

ANALYZING MAGNET CONTROL SYSTEM
MAGNET CONTROLLER
POWER, INDICATOR LAMPS, CIRCUIT CARD LOCATIONS
84-6041

INDICATOR LAMPS

FORMATION OF LOGIC SIGNALS

EXTERNAL SIGNALS

MAGNETIC FIELD SET

SWITCH FILTERS

ANALYZING MAGNET CONTROL SYSTEM
MAGNET CONTROLLER
LOGIC - I
84-6042

DAC STEPPING

MOTOR STEPPING

ANALYZING MAGNET CONTROL SYSTEM MAGNET CONTROLLER LOGIC-2 84-6043

DIGITAL TO ANALOG CONVERTER

UP/ DOWN REGISTER

BIT	LOC	OUTPUT		INPUT	
		O	I	H-S	E-P
2	207	K020	K021	K011	K010
3	206	K030	K031	K021	K020
4	205	K040	K041	K031	K030
5	204	K050	K051	K041	K040
6	203	K060	K061	K051	K050
7	202	K070	K071	K061	K060

ANALYZING MAGNET CONTROL SYSTEM
MAGNET CONTROLLER
7-BIT DAC WITH UP/DOWN REGISTER
84-6C44

ANALYZING MAGNET CONTROL SYSTEM
MODIFICATION OF HVEC ANALYZING MAGNET
SYSTEM

84-6045