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MASTER

A SENSITIVE, HIGH-SPEED, DC

VOLTAGE COMPARATOR

by

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ABSTRACT

Factors which are important in the design and application of a sensitive, high-speed, DC voltage comparator are examined. A specific transistor comparator design, suitable for use in many practical applications, is presented and considered in terms of these design factors.

A detailed investigation of this design is made to determine what static and dynamic performance can be provided by the design and to determine what factors limit various phases of the overall performance and how these factors are inter-related. An experimental comparator was constructed to verify some of the assumptions and results which are presented.

The comparator circuit cannot be optimized simultaneously for the best sensitivity, accuracy, and dynamic response because of conflicting design requirements. The compromise in the experimental comparator circuit provided a static sensitivity of 0.385 Mv. The application of a 20 Mv input signal caused the output to change states in approximately 10 ns. Under certain conditions a maximum error of about 4.3 Mv can occur.

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CHAPTER I

INTRODUCTION

Definition of a Comparator

For purposes of this thesis, a comparator is defined as an electrical device which provides an output that indicates at every instant of time which of two input potentials is the more positive.

The input may be considered as one signal which is the difference in voltage between the two input voltages or, as two separate signals which are both measured with respect to a third common or ground terminal and which are applied separately to the two input terminals. The input is regarded in either of these two ways depending upon which is the most convenient.

In many applications it is convenient to regard one of the two terminals as a reference terminal and the binary output as indicating whether the input voltage applied to the other terminal is positive or negative with respect to this reference. In this case the reference terminal voltage is usually a constant or known function of time. However, in the general case, the input to both terminals is an unknown function of time.

It is noted that the comparator, as defined above, is supplied with analog input information and it provides binary output information.

Types and Uses of Comparators

There are many different types of devices and circuits that are often used as comparators depending upon application. Comparators are

usually thought of as either current or voltage sensing depending upon the impedance of the comparator and of the source. For example, a galvanometer used as a null indicating device in an instrument may be regarded as a current sensing comparator. Other devices often used as comparators include relays, saturating transformers, vacuum tubes, and semiconductor devices.

Various types of comparators are found in digital voltmeters, telemetry systems, analog to digital converters, analog data processing equipment, pulse height analyzers, go-no go indicators, off-on servo systems, trigger circuits in various types of test equipment, and sweep delay generators in oscilloscopes.

Since a comparator is to provide only two output states, comparators usually contain positive feedback so that the output will be switched quickly from one state to the other. The introduction of positive feedback also causes hysteresis which results in the output signal not always indicating the actual input condition. If the feedback is not included, output conditions between the two desired states can occur.

Most comparator circuits utilizing vacuum tubes or transistors in the input use two devices in a balanced circuit, as in a differential amplifier, in order to reduce the effects of temperature and other undesired changes by means of cancellation.

The familiar Schmitt trigger is an example of a circuit which illustrates many of these points. In this circuit, and many other comparators, the input signal is compared to a reference which is fixed or

at least is not easily changed with respect to the ground terminal. In many important comparator applications one input terminal is the ground terminal of the system and the output information desired is if the input signal is positive or negative with respect to ground.

Because comparator circuits are often quite similar to DC coupled differential amplifiers, performance specifications relating to the input of both are quite similar. In fact, the comparator action can be accomplished by a DC amplifier which has infinite gain if the output is clipped or limited to provide the two desired output states. This is possible because the output of a comparator for zero input is not defined.

Comparator Performance

In a perfect comparator the output is switched instantaneously from one state to the other at the exact instant the difference between the two input signals goes through zero. Such a comparator would always be able to resolve the sign of the difference between the two signals no matter how slowly the difference passed through zero. Because all realizable circuits contain noise and have finite gain and are thus unable to resolve signals below a certain level, positive feedback is used to assure binary output.

It can be seen that all of the performance characteristics of a comparator, except speed of operation, may be improved by placing a high quality DC amplifier between the input signal and the comparator.

Scope of Thesis

In many comparator applications, speed of response is just as important as the static accuracy. The design of high performance DC amplifiers and the static aspects of the design of comparators are well covered in the available literature. However, very little material is available which may be directly applied to the design of a high-speed comparator.

In the remainder of this thesis, factors which are pertinent to a high-speed comparator operation are first considered. A specific junction transistor comparator design suitable for use in a variety of high-speed applications is presented. This circuit is analyzed first for static response and then for dynamic response in order to determine what factors impose limits on the performance of the comparator. Actual measurements on an experimental model of the circuit are used to substantiate the importance of most of the factors which are considered. Special attention is given to the dynamic response for signals only slightly greater than the hysteresis.

CHAPTER II

CONSIDERATIONS FOR A HIGH-SPEED COMPARATOR DESIGN

Comparator Input

In many applications of comparators it is desirable to make the input impedance as high as possible in order to avoid loading the voltage source. High-speed signals are usually found only in relatively low impedance circuits where unavoidable capacity will not degrade the signal as badly as in high impedance circuits. For this reason it has been assumed that the input signals will be supplied from a terminated 50 ohm coaxial cable and that no effort is necessary to keep the comparator input impedance large.

Another consideration is the maximum signal which can be applied to the input. In order for the comparator to be useful in many applications, the maximum allowed input should be very large compared to accuracy of the comparator. For example, if the comparator can accurately resolve input differences of 0.5 millivolts, yet can accommodate input signals as large as 5 volts, then it might be considered to have an accuracy of 0.01 per cent. In some applications only the accuracy of resolution for small inputs is important. A circuit which can accept large inputs without damage but which has a relatively long recovery period, is limited to small inputs in high-speed applications.

Input offset current is usually not important when working from a low impedance source. It is often desirable for the comparator to be able to operate with a small offset voltage in order to accommodate static unbalances in the transducers which supply the input signal.

Comparator Output

Since a comparator is to provide only two output states it is important, particularly in a high-speed application, that the output is always switched between the two states very quickly even when the input is changed very slowly. In many cases the output of the comparator is fed into digital switching equipment which is capacity coupled and will not operate with a slowly changing input. The output impedance of the comparator should be low for the same reason that the input impedance is low and the output signal amplitude must provide adequate drive for subsequent circuits. It is usually important that sufficient isolation be provided so that the stability of the comparator is not affected by various loads or noise which may be present on the output line.

Static Transfer Characteristics

The ideal transfer characteristic for a perfect comparator is shown in Figure 1a, Page 7. Realization of this characteristic would require an amplifier with infinite gain and infinite band width in order to switch instantaneously between output states. Figure 1b through Figure 1f shows the transfer characteristics which would be obtainable for various circuit conditions to be described.

Figure 1b is the characteristic which would be obtained with a linear low gain amplifier. A higher gain amplifier with limiting would provide the characteristic shown in Figure 1c.

Figure 1d shows the characteristic of a very high gain amplifier with limiting and a region of uncertainty due to noise and drift which

FIGURE 1

THEORETICAL STATIC TRANSFER CHARACTERISTICS FOR VARIOUS
AMPLIFIER AND FEEDBACK CONDITIONS

become more apparent in very high gain amplifiers. Figure 1e shows the characteristic which would result if positive feedback is added to the amplifier. There is no longer a region of ambiguous output due to drift or noise but hysteresis has been added. Finally, Figure 1f shows how the previous characteristic can be improved by the addition of a very low noise, low drift amplifier between the source and comparator input.

Stability

The hardest problem to overcome in a DC amplifier design is usually that of providing sufficient stability of the zero point. This same problem of stability is often the limiting factor in the performance of a sensitive comparator. Most of the instability or drift in the output of a DC amplifier is introduced by the first stage and is subsequently amplified. The overall stability of a DC amplifier or of a comparator cannot be improved by the addition of negative feedback since this reduces the gain in the same proportion as the drift.

Drift in a DC coupled amplifier is analogous to noise in an AC amplifier. Higher frequency noise is also present in a wide band DC coupled amplifier but its amplitude is usually small compared to the drift. It is observed that drift is reduced in the same way as noise, such as by the incorporation of a high gain input stage to reduce the contributions caused by following stages.

Except for physical changes which might occur due to aging of components, drift is due to changes in the amplifier environment, particularly to temperature and to supply voltage changes. If these factors can be adequately controlled, then the desired degree of

stability of the zero point should be obtainable. However, this approach is usually not practical. A better approach is to make the circuit absolutely symmetrical with respect to the two inputs. Environmental changes will then affect both inputs in exactly the same way and their effects will cancel.

Chopper stabilized amplifiers are not readily useful because they require that the input be periodically disconnected in order to establish the zero point. With high-speed input circuits much information would be lost during the dead time. It would be possible in a more complex arrangement to use a dual amplifier system.

Dynamic Response

Errors introduced by the imperfect dynamic response can usually be separated into two types, errors due to output delays caused by a minimum fixed signal propagation time which can always be considered constant and errors that are a function of the input signal amplitude, waveshape, and DC level.

In a high-speed comparator the basic information desired is when did the input signal cross the reference level. If the input signal is known to always have certain characteristics then it is possible to subtract a previously determined propagation time in order to determine when the signal crossed the reference level. This is useful when the comparator is used to determine when a certain event occurred in relation to another event or when it is used to determine the phase relationship of two periodic signals. Thus, propagation delay errors do not impose limitation in some types of application.

Errors that are a function of the signal cannot be allowed for unless sufficient information is known about the signal. For example, when the comparator is used as a pulse height analyzer for random input pulses or to determine the length of time a pulse is above a reference level, errors can result which are a function of the shape of the input pulse. In some applications, involving random inputs or noise where the output of the comparator is integrated, errors that are a function of the signal can be reasonably assumed to cancel.

In still other applications where the input is a random function of time and the comparator output is used to initiate some action, such as is the case in many atomic physics instrumentation applications, any delay, predictable or otherwise, imposes severe application limitations.

A Practical Design

The schematic diagram of a particular practical high-speed comparator design which has been selected for detailed study is shown in Figure 2, Page 11. This circuit has the advantages of being relatively simple and of being applicable to a wide variety of uses. This design will be investigated in order to determine what performance could be expected and to determine how the factors that are important in predicting the performance are interrelated.

All of the factors which have been considered important in the design and performance of a high-speed comparator have been considered in this design. This circuit, which uses nine high-speed silicon epitaxial transistors, is completely symmetrical with respect to the two

FIGURE 2

SCHEMATIC DIAGRAM OF COMPLETE DC COMPARATOR CIRCUIT

inputs, thus accurate matching of components will assure good stability with respect to ambient temperature and to supply voltage changes. By the use of alternating NPN and PNP transistor stages the supply voltages can be kept low and the problem of DC level transformation is solved. All of the transistors are prevented, by the design, from saturating, thus eliminating the problem of excess charge storage and assuring the highest speed of operation of which the transistors are capable.

Although four power supply voltages are required, the current drawn from each is constant for all input signal conditions. This allows all of the voltages to be obtained from one power supply by the addition of a resistive voltage divider circuit. Also, since the supply currents are constant, no transients are created by the high-speed signals which could cause trouble in other high-speed circuits that might be incorporated with the comparator.

Both of the inputs are isolated from ground which provides maximum flexibility. The input voltages can be quite large without causing overload problems. Except for a small shunt capacity, the input impedance is nearly constant for all signal conditions.

The output circuit provides two completely isolated complementary outputs which are of constant impedance. Although the output signals for the circuit shown are only zero or positive with respect to ground, a negative output can easily be provided if desired.

CHAPTER III

STATIC CHARACTERISTICS

Assumptions

Several assumptions are made in order to simplify the analysis of static conditions. The effects of inductance and capacity are not considered. It is assumed that the transistors are linear while in the active region. Both large and small signal parameters need to be considered since switching in the comparator stage occurs while the transistors in the two preceding differential amplifier stages are operating under small signal conditions. However, DC coupling is maintained and the large input signals permitted can completely cut off one transistor in each of the two differential amplifiers.

The transistor parameters considered are V_{BE} , h_{ie} , and h_{fe} which is considered to be equal to h_{FE} . The load impedance of each stage is quite low and the resulting collector voltage swing is small so that h_{oe} and h_{re} can be neglected. Also, because of the low resistance of the collector load resistors, the output loading due to the following stage can also be neglected without introducing any appreciable error.

Linearity of the two differential amplifier stages is not important. However, it is important for good DC stability to be maintained near the balance point. It would also be desirable for the differential voltage gain of these two amplifiers to be high near balance. This can be accomplished if the collector load resistance is made large. Since large impedances are not compatible with high-speed operation, a

relatively low load resistance is used. The resulting operating conditions are quite different from those usually found in low level differential amplifier input stages.

The constant current source for the first stage is assumed to be perfect in the analysis. This, along with the fact that h_{oe} and h_{re} are neglected, implies that the common mode voltage gain of the first stage is assumed to be zero.

An equivalent circuit of the first stage differential amplifier is shown in Figure 3, Page 15. If the emitter resistors are omitted, this circuit may also be used for the equivalent circuit of the second stage. This equivalent circuit is valid only when both transistors in the amplifier are biased into the active region.

In this circuit, R_1 and R_2 are the collector load resistors for the stage. R_3 and R_4 include the common emitter input resistance h_{ie} . R_5 and R_6 , the series emitter resistance, is present only in the first stage, where it is the resistance of the arms obtained for an equivalent "T" circuit when the "TT" circuit actually used to balance the input is transformed.¹ V_{BE1} and V_{BE2} are the base-to-emitter voltage drops of the transistors and are considered constant with respect to current. Since switching in the comparator will always occur at practically the same operating point, this assumption will introduce little error. V_{BE} will be considered later as a function of temperature. I_{CBO} is neglected since it is quite small in planar silicon transistors and because the emitter constant current source provides a stabilization factor of one.

¹See Appendix A.

FIGURE 3

EQUIVALENT CIRCUIT USED FOR DC ANALYSIS OF
FIRST AND SECOND DIFFERENTIAL
AMPLIFIER STAGES

Amplifier Analysis

The following three equations describing the circuit shown in Figure 3 can be written by inspection:

$$e_o = i_3 h_{fe1} R_1 - i_4 h_{fe2} R_2, \quad \text{III-1}$$

$$e_i = [R_3 i_3 + V_{BE1} + R_5 (h_{fe1} + 1) i_3] - [R_6 (h_{fe2} + 1) i_4 + V_{BE2} + R_4 i_4]$$

which can be rewritten as

$$e_i + V_{BE2} - V_{BE1} = i_3 [R_3 + R_5 (h_{fe1} + 1)] - i_4 [R_4 + R_6 (h_{fe2} + 1)] \quad \text{III-2}$$

and,

$$I_T = i_3 (h_{fe1} + 1) + i_4 (h_{fe2} + 1). \quad \text{III-3}$$

Equations III-2 and III-3 may be solved simultaneously to obtain values for i_3 and i_4 which may then be substituted into Equation III-1 to obtain e_o as a function of e_i , I_T , and the circuit parameters.

$$\text{If } \Delta = [R_3 + R_5 (h_{fe1} + 1)] (h_{fe2} + 1) + [R_4 + R_6 (h_{fe2} + 1)] (h_{fe1} + 1),$$

$$i_3 = \frac{I_T [R_4 + R_6 (h_{fe2} + 1)] + (e_i + V_{BE2} - V_{BE1}) (h_{fe2} + 1)}{\Delta},$$

$$i_4 = \frac{I_T [R_3 + R_5 (h_{fe1} + 1)] - (e_i + V_{BE2} - V_{BE1}) (h_{fe1} + 1)}{\Delta}, \text{ and}$$

$$e_o = \frac{\{I_T [R_4 + R_6 (h_{fe2} + 1)] + (e_i + V_{BE2} - V_{BE1}) (h_{fe2} + 1)\} h_{fe1} R_1}{\Delta} - \frac{\{I_T [R_3 + R_5 (h_{fe1} + 1)] - (e_i + V_{BE2} - V_{BE1}) (h_{fe1} + 1)\} h_{fe2} R_2}{\Delta}. \quad \text{III-4}$$

Equation III-4 can be rewritten in the form

$$e_o = (e_i + V_{BE2} - V_{BE1})A + I_T B \quad \text{III-5}$$

where

$$A = \frac{(h_{fe2}+1)h_{fe1}R_1 + (h_{fe1}+1)h_{fe2}R_2}{\Delta} \quad \text{and} \quad \text{III-6}$$

$$B = \frac{[R_4 + R_6(h_{fe2}+1)]h_{fe1}R_1 - [R_3 + R_5(h_{fe1}+1)]h_{fe2}R_2}{\Delta} \quad \text{III-7}$$

It is desired to make $(V_{BE2} - V_{BE1})A + I_T B = 0$ so that $e_o = Ae_i$ or

$$\frac{e_o}{e_i} = A.$$

Unbalance Referred to Input Terminals

In multi-stage DC coupled amplifiers it is convenient to express any error or drift in terms of an equivalent input signal which would be required at the input in order to reduce the output to zero. This is because most of the error or drift usually occurs in the first stage, providing its gain is reasonably large, and because, if expressed in terms of the output of the amplifier, the value is proportional to the overall amplifier gain. Making $e_o = 0$ and solving for e_i in Equation III-5 results in the following expression for the input offset voltage, e_{i0} , (input voltage which makes the output voltage zero):

$$e_i = e_{i0} = V_{BE2} - V_{BE1} + \frac{I_T B}{A} \quad \text{III-8}$$

In an analogous manner it is also possible to solve for the input offset current. However, since the input amplifier is intended to be used with a low impedance source (a terminated 50 ohm coaxial cable), the offset current error is small and is neglected.

Equation III-8 clearly shows that any difference in the base-to-emitter voltages of the two input transistors is equivalent to an input signal equal to this difference. By adjusting the value of B with the potentiometer in the first stage it is possible to make $e_{i0} = 0$ by making $V_{BE2} - V_{BE1} = \frac{I_T B}{A}$. However, this is an undesirable solution since h_{fe} and h_{ie} , which are included in the expression for A and B, and V_{BE} are all functions of temperature such that the equality is not maintained when the temperature is varied. Thus, if possible, $V_{BE2} - V_{BE1}$ and $\frac{I_T B}{A}$ should each be made equal to zero. For this reason the base-to-emitter voltages and the temperature coefficients of the base-to-emitter voltages should be matched as closely as possible.

When the base-to-emitter voltages are matched, it is still necessary for the $I_T B/A$ term in Equation III-8 to equal zero in order to completely eliminate the offset term. I_T cannot be made small (usual first stage practice) without a resulting reduction in frequency response. The gain, A, could be increased by increasing the collector load resistors but this would also reduce the frequency response. Thus the only satisfactory solution is to make the numerator of the expression for B equal to zero. Thus:

$$\left[R_4 + R_6(h_{fe2} + 1) \right] h_{fe1} R_1 = \left[R_3 + R_5(h_{fe1} + 1) \right] h_{fe2} R_2 \quad \text{III-9}$$

R_1 and R_2 are 1 per cent resistors and are assumed equal. The current gains of the two transistors are closely matched (within 2 per cent) in the operating region and are large compared to one. For the first stage the value of h_{ie} is much larger than the source impedance and the sum of R_5 and R_6 must be 5 ohms.

Thus Equation III-9 is simplified to:

$$h_{ie2} + 5p h_{fe} = h_{ie1} + 5(1-p) h_{fe} \quad \text{where } 0 \leq p \leq 1 \quad \text{III-10}$$

When the approximate values of the transistor parameters are substituted into Equation III-10 it is found that the maximum unbalance in h_{ie} of the two first stage transistors which can be accommodated with the potentiometer is about 20 per cent. Since the current gains of the transistors are closely matched, the position of the potentiometer at balance can be used to give an indication of how accurately the other transistor parameters are matched.

Common Emitter Input Resistance

From basic semiconductor theory² the incremental resistance, r_e , of a forward biased p-n junction is given by

$$r_e = \frac{KT}{qI}$$

Where T is the absolute temperature, K is Boltzmann's constant, q is the charge of an electron, and I is the bias current. At room temperature when values for K and q are substituted in

$$r_e(\text{ohms}) \approx \frac{26}{I_e(\text{ma})}$$

In a common base T-equivalent circuit of a transistor, r_e is the emitter input resistance resulting from the forward biased emitter-base junction, and I_e is the emitter bias current. When this circuit is

²D. LeCroisette, Transistors (Englewood Cliffs, New Jersey: Prentice-Hall, 1963), p. 108.

transformed to a common emitter circuit, the equivalent input resistance is approximately r_e times the incremental common emitter current gain. The total input resistance must also include another term, r_b' , caused by the ohmic resistance in the base region. The value of r_b' depends upon the physical transistor structure and cannot be accurately predicted by semiconductor theory.

The common emitter input resistance, h_{ie} , may be predicted by

$$h_{ie} = r_b' + h_{fe} \frac{KT}{qI_E}.$$

For the two first stage transistors the following approximate values may be used to estimate h_{ie} :

$$r_b' = 50 \text{ ohms (see Chapter IV)}$$

$$I_E = \frac{1}{2} I_T = 1.25 \text{ Ma}$$

$$h_{fe} = 60 \text{ (measured at } I_C = 1.25 \text{ Ma)}$$

Thus,

$$h_{ie} = 50 + 60 \frac{26}{1.25} = 1300 \text{ ohms.}$$

First Stage Voltage Gain

The above values for the transistor parameters can be used to calculate the voltage gain of the first stage. A resistance, R_S , of 100 ohms was placed in series with each input to the first stage in order to limit the base current if too much voltage should accidentally be applied between the inputs, causing emitter to base breakdown in one transistor. For the first stage,

$$R_1 = R_2 = 330 \text{ ohms}$$

$$R_3 = R_4 = R_S + h_{ie} = 100 + 1300 = 1400 \text{ ohms}$$

$$R_5 = R_6 = 2.50 \text{ ohms (potentiometer assumed in center position)}$$

$$h_{fe1} = h_{fe2} = 60 \text{ (approximate measured value at } I_C = 1.25 \text{ Ma)}$$

Substituting these values into Equation III-6 to calculate the voltage gain,

$$A = \frac{(60+1)60 \cdot 330 + (60+1)60 \cdot 330}{[1400 + 2.50(60+1)](60+1) + [1400 + 2.50(60+1)](60+1)} = 12.6.$$

The experimentally measured gain of this stage was 13.6, which is in good agreement with the calculated value.

Second Stage Voltage Gain

Similar calculations can also be made for the second stage. The base voltage of the second stage during balanced conditions is: 6.0V - 1.25 Ma (300Ω) = 5.6V.

Assuming $V_{BE} = 0.6V$,

$$I_T = \frac{12V - 5.6V - 0.6V}{680\Omega} = 8.6 \text{ Ma}$$

For the two second stage transistors the following approximate values may be used to estimate h_{ie} :

$$r_b' = 50 \text{ ohms (See Chapter IV)}$$

$$I_E = \frac{1}{2} I_T = 4.3 \text{ Ma}$$

$$h_{fe} = 156 \text{ (measured at } I_C = 4.3 \text{ Ma)}$$

Thus,

$$h_{ie} = 50 + 156 \frac{26}{4.3} = 50 + 945 \approx 1,000 \text{ ohms}$$

For the second stage,

$$R_1 = R_2 = 150 \text{ ohms}$$

$$R_3 = R_4 = 330 + 1,000 = 1,330 \text{ ohms}$$

$$R_5 = R_6 = 0$$

$$h_{fe1} = h_{fe2} = 156 \text{ (average of measured values)}$$

Substituting these values into Equation III-6 to calculate the voltage gain

$$A = \frac{(156+1) 156 \cdot 150 + (156+1) 156 \cdot 150}{(1330) (156+1) + (1330) (156+1)} = 17.6$$

The experimentally measured gain of this stage was 17.9, which is in very good agreement.

Voltage Gain as a Function of Bias Current

The gain, A , of the stage is not a function of I_T insofar as the values of the transistor parameters are independent of current. However, A is actually related to I_T since h_{ie} , which makes up most of R_3 and R_4 , is almost inversely proportional to I_T , resulting in higher stage gain for larger values of I_T . The current gain, h_{fe} , will also increase slightly with increasing collector current since the transistors, particularly in the first stage, are operated considerably below the current at which h_{fe} reaches its maximum value.

Increasing I_T to obtain more gain and to improve the high frequency characteristics as described in Chapter IV, results in lower DC accuracy. This can be explained as a result of temperature effects. It has been implicitly assumed that both transistor junctions of a single stage were at ambient temperature, and thus both at the same temperature. If I_T is small enough the power dissipated in the transistor junctions will not be enough to appreciably raise the junction temperature of either transistor above the ambient temperature. Even quickly

following a long interval of time during which a large input signal causes one transistor to be cut completely off and the other transistor to dissipate twice its power at balance, the junction temperature of the "on" transistor is nearly the same as the ambient temperature and only a very small voltage error, or offset, can be introduced in the sensing level. However, if the power dissipated in the "on" transistor is large, the junction temperature will be raised a significant amount above the ambient temperature. In this case, if thermal resistance between the two junctions is not very low, the junction temperature of the "off" transistor will be lower and the resulting difference of $V_{BE2} - V_{BE1}$ will appear as an offset voltage which will exist at the sense level.

Thermal Instability

Because V_{BE} decreases with increasing temperature, there exists a possibility of thermal instability which could result in thermal run-away. Since the maximum run-away current would be limited to I_T , this condition would not be destructive. Assume, for example, that the transistors and the components are exactly balanced and the input is zero. If a small junction temperature unbalance occurs, resulting perhaps from a previous input signal, the transistor with the higher junction temperature will draw more than half of I_T . The increased dissipation may be enough to further raise the temperature of the hotter junction which would in turn cause even more power to be dissipated. A regenerative condition can exist until nearly all of the bias current has been shifted to the hotter junction.

This regenerative condition can occur only when the rate of change of power generated with an increase in temperature is greater than the rate of change of power dissipated with an increase of temperature. Expressed mathematically, run-away will occur if

$$\frac{dP_G}{dT} > \frac{dP_D}{dT}$$

The right hand side of this inequality is usually a constant and the reciprocal of this value is called thermal resistance and is denoted by the symbol θ . However, in this case the left hand side of the inequality is inversely proportional to V_{BE} as a function of temperature and this is also very nearly a linear function of temperature. Insofar as both sides of the inequality are constants, the ambient temperature has no bearing on whether or not regeneration and the resulting instability will occur. This depends only upon the thermal and electrical parameters of the amplifier stage.

Determination of Thermal Stability

To determine if regeneration will occur, a loop with the various transfer functions can be formed and the loop gain determined. If the gain is more than plus one, the amplifier will be thermally unstable. Figure 4, Page 25, shows how the loop is divided in order to facilitate this calculation and it defines the transfer functions. It is assumed that the input voltage is zero and that the thermal and electrical parameters of each stage are matched.

FIGURE 4

BLOCK DIAGRAM OF TRANSFER FUNCTIONS USED TO DETERMINE
THERMAL STABILITY OF FIRST AND SECOND
DIFFERENTIAL AMPLIFIER STAGES

From Equation III-5, Page 17, if $e_1 = 0$, and if $B = 0$, then

$$e_o = (V_{BE2} - V_{BE1})A$$

or

$$\frac{e_o}{V_{BE2} - V_{BE1}} = A \quad \text{III-11}$$

The value of A , which is simply the voltage gain of the stage, has already been determined.

To determine F , the difference in junction dissipation corresponding to an output e_o , it is assumed that the change in collector voltage due to the current flowing through the collector load resistor can be neglected compared to the total collector voltage. This will result in a slightly pessimistic analysis. For the second stage the value of the collector to emitter voltage is constant. However, in the first stage it depends upon the base voltage which may be allowed to vary between plus or minus five volts with respect to ground. This results in over a ten-to-one ratio between the maximum and minimum power which may be dissipated. The worst case will occur for the largest allowed negative input voltage so this value will be used for the first stage calculation.

$$e_o = I_{C1}R_C - I_{C2}R_C = (I_{C1} - I_{C2})R_C$$

where $I_{C1} - I_{C2}$ is the difference in collector currents and R_C is the collector load resistance.

Multiplying both sides by V_{CE} , the collector to emitter voltage, the expression

$$\left[V_{CE} \right] e_o = (I_{C1} - I_{C2})R_C \left[V_{CE} \right] = (P_{J1} - P_{J2})R_C$$

is obtained where $P_{J1} - P_{J2}$ is the difference in power dissipated in the two transistor junctions. Finally, the desired function is found to be

$$F = \frac{P_{J1} - P_{J2}}{e_o} = \frac{V_{CE}}{R_C} . \quad \text{III-12}$$

It is interesting to note that F is not a function of I_T , the bias current.

Figure 5, Page 28, is a thermal schematic diagram of a differential amplifier stage which assumes lumped elements for the thermal circuit. Thermal capacities are not shown in Figure 5 because the diagram is used only for a steady state analysis. When they are included, the resulting time constants can be as much as several seconds when separate transistor packages are mounted on a common heat sink.

The two power sources P_{J1} and P_{J2} , represent the power dissipated in the junction of each transistor of the amplifier stage and are analogous to constant current sources in an electrical circuit. θ_{JH} is the thermal resistance between each junction and the transistor case header. θ_{HA} is the thermal resistance between the header and the ambient temperature, T_A , which is used as the reference level. T_{J1} and T_{J2} are the temperatures of the two junctions and T_H is the temperature of the header.

If, in place of using a dual transistor consisting of two transistor junctions mounted on a common header, the two transistor junctions are mounted in separate packages, the same thermal schematic may be used if the two transistor cases are mounted close together on a

FIGURE 5

EQUIVALENT THERMAL SCHEMATIC DIAGRAM OF
TWO TRANSISTORS MOUNTED ON A
COMMON HEAT SINK

common heat sink. In this case the H subscripts refer to the header.

From Figure 5:

$$T_{J1} - T_{J2} = P_{J1}\theta_{JH} - P_{J2}\theta_{JH} = (P_{J1} - P_{J2})\theta_{JH}$$

or

$$\frac{T_{J1} - T_{J2}}{P_{J1} - P_{J2}} = G = \theta_{JC}.$$

From semiconductor theory it is found that the voltage across a p-n junction, which is forward biased at constant current, is approximately inversely proportional to the absolute temperature. This effect causes the base-to-emitter voltage, V_{BE} , across the forward biased emitter-base junction of a transistor to have a negative temperature coefficient. The value of this coefficient in silicon transistors is somewhat a function of bias current but is usually between -2.0 and -3.0 millivolts per degree centigrade. Since the temperature coefficient was not measured, a value of -2.5 Mv/ $^{\circ}$ C will be assumed. Thus:

$$\frac{V_{BE1} - V_{BE2}}{T_{J1} - T_{J2}} = H = 2.5 \frac{\text{Mv}}{^{\circ}\text{C}}$$

The effects of thermal stability are most important in the first amplifier stage and to a lesser extent in the second stage since the importance of this effect is reduced by the gain of preceding stages. Thus the loop gain, the product of the transfer function A, F, G, and H, is calculated for the first and second stages.

For the first stage:

$$A = 12.6$$

$$F = \frac{V_C}{R_C} = \frac{12V}{330\Omega} = .036 \frac{\text{volts}}{\text{ohm}} = 0.036 \frac{\text{Mv}}{\text{Mv}}$$

$$G = \theta_{JH} = 0.05 \text{ }^{\circ}\text{C/Mw}$$

$$H = \frac{\Delta V}{\Delta T} = 2.5 \text{ Mv/}^{\circ}\text{C}$$

$$A \cdot F \cdot G \cdot H = 12.6 (0.036)(0.05)2.5 = .057$$

For the second stage:

$$A = 17.6$$

$$F = \frac{V_C}{R_C} = \frac{6}{150} = 0.040 \frac{\text{Mw}}{\text{Mv}}$$

$$G = 0.05 \text{ }^{\circ}\text{C/Mw}$$

$$H = 2.5 \text{ Mv/}^{\circ}\text{C}$$

$$A \cdot F \cdot G \cdot H = 17.6(0.040)(0.05)2.50 = 0.088$$

The loop gain is less than one for both stages which indicates that the balanced condition is a stable state. This was, in fact, observed to be the case. In order to check this calculation, the first stage transistors were replaced with some very small junction transistors in separate cases without providing any heat sink. With this arrangement it was found that balance could not be maintained. Drift would start slowly and then increase until a large unbalance was reached.

Maximum Thermal Error

Although the preceding calculations show that the balanced state is stable, they give no indication of the error which can be introduced immediately following a large signal which causes one transistor to be cut off. The maximum error, V_e , can thus be introduced is,

$$V_e = P_{J \text{ max}} \cdot \theta_{JH} \cdot \frac{\Delta V}{\Delta T} = V_{BE \text{ max}} I_T \theta_{JH} \cdot \frac{\Delta V}{\Delta T}$$

For the first stage:

$$V_e = 12V \cdot 2.5Ma \cdot 0.05 \text{ } ^\circ C/Mw \cdot 2.5 \text{ Mv}/^\circ C = 3.75 \text{ Mv}$$

For the second stage:

$$V_e = 6V \cdot 8.6Ma \cdot 0.05 \text{ } ^\circ C/Mw \cdot 2.5 \text{ Mv}/^\circ C = 6.45 \text{ Mv}$$

The value of V_e for the second stage must be divided by the gain of the first stage in order to find the effect in terms of input error. The total error introduced is

$$V_{et} = 3.75 + \frac{6.45}{12.6} \approx 4.3 \text{ Mv}$$

of which most is introduced by the first stage.

It is seen that the amount of thermal error which can be introduced is a function of I_T but that the thermal stability is not a function of I_T .

Errors due to thermal effects also occur in the comparator stage which always operates a switching mode. However, sufficient voltage gain precedes this stage to make these errors negligible compared to those already introduced.

If the complete comparator is always used with signals that are very small, for example differences of less than 50 Mv, the first stage amplifier is never driven very far from balance. Total error due to thermal effects in this case will always be much less than the maximum error which was calculated, provided the amplifier stages are thermally stable.

Another special case would occur if the input to the comparator contains no average direct current component. The period of the lowest

frequency present could be several seconds and still cause negligible thermal error since the thermal time constant could be made even larger.

Still another special case would occur if an average large unbalance was always present. In this case the error caused by thermal unbalance could be eliminated by introducing electrical circuit unbalance in the direction to compensate for it by means of the balance potentiometer.

Positive Feedback Amplifier.

Figure 6, Page 33, is a schematic diagram of the third amplifier stage which incorporates the positive feedback necessary to obtain an abrupt switching point. Except for the addition of the two feedback resistors, R_5 and R_6 , the circuit configuration is the same as for the second amplifier stage. However, the feedback causes the stage to operate as a non-saturated flip-flop.

Figure 7, Page 34, is an equivalent circuit which shows the circuit parameters which are considered in the analysis of the stage. The loading of the collectors caused by the output stage is very small and is neglected. The two current sources indicated as i_1 and i_2 are the collector currents of the preceding stage and R_3 and R_4 are the collector load resistors of the preceding stage.

The input necessary to bring the feedback amplifier to the threshold of switching from one state to the other is found by determining the difference of the two input current sources, $i_2 - i_1$, which will just cause

FIGURE 6

SCHEMATIC DIAGRAM OF POSITIVE FEEDBACK AMPLIFIER

R_{in} is approximately equal to h_{ie} for i_B in positive direction and is very large for i_B in negative direction.

FIGURE 7

COMPLETE EQUIVALENT CIRCUIT OF POSITIVE FEEDBACK AMPLIFIER

the "off" transistor to start conducting. If the cascaded transconductance of the two preceding amplifier stages is known, and if it is assumed that there are no offset voltages in the first two stages, the input voltage difference, which will cause switching, is equal to the above current difference divided by the amplifier transconductance. The total hysteresis will then be twice this value.

Figure 8, Page 36, is a further simplified equivalent circuit which shows only the elements which need to be considered in order to find the current difference, $i_2 - i_1$, which will initiate switching by just bringing Q_2 to the threshold of conduction if Q_1 is assumed to be "on". Since the circuit is then considered to be in a linear active region, the loop gain will be high and switching will occur. Thus, in Figure 8 it is necessary to determine $i_2 - i_1$ such that the voltage across R_{1n} is just reduced to zero.

Determination of Current Difference Required to Initiate Switching

Assuming that there is no current through R_{1n} in Figure 8, the voltage, V_{B1} , at the base of Q_1 may be expressed as

$$V_{B1} = V_{CC} \frac{R_3}{R_2 + R_3 + R_5} + (i_1 - i_{B1}) \frac{R_3(R_2 + R_5)}{R_2 + R_3 + R_5}, \quad \text{III-13}$$

and the voltage, V_{B2} , at the base of Q_2 may be expressed as

$$V_{B2} = V_{CC} \frac{R_4}{R_1 + R_4 + R_6} - h_{fe1} i_{B1} \frac{R_1 R_4}{R_1 + R_4 + R_6} + i_2 \frac{R_4(R_1 + R_6)}{R_1 + R_4 + R_6}.$$

If the resistors in the circuit are assumed to be matched then $R_1 = R_2$, $R_5 = R_5$, and $R_4 = R_3$. In this case

FIGURE 8

SIMPLIFIED EQUIVALENT CIRCUIT OF POSITIVE FEEDBACK AMPLIFIER
FOR Q_1 "ON" AND Q_2 "OFF"

$$V_{B2} = V_{CC} \frac{R_3}{R_2+R_3+R_5} - h_{fe1} i_{B1} \frac{R_2 R_3}{R_2+R_3+R_5} + i_2 \frac{R_3(R_2+R_5)}{R_2+R_3+R_5}. \quad \text{III-14}$$

Since the voltage across R_{in} is assumed to be zero,

$$V_{B1} - i_{B1} h_{ie1} - V_{BE1} + V_{BE2} = V_{B2}. \quad \text{III-15}$$

When Equations III-13 and III-14 are substituted into Equation III-15, the V_{CC} terms cancel. Solving for $i_2 - i_1$ in the remaining equation

$$i_2 - i_1 = h_{fe1} i_{B1} \frac{1}{1 + \frac{R_5}{R_2}} - i_{B1} - \left[i_{B1} h_{ie1} + V_{BE1} - V_{BE2} \right] \left[\frac{1}{R_3} + \frac{1}{R_2+R_5} \right]. \quad \text{III-16}$$

Since $i_{B1} = \frac{I_T}{h_{fe1} + 1}$ and since $h_{fe1} \gg 1$, $i_{B1} \approx \frac{I_T}{h_{fe1}}$, i_{B1} in Equation III-16 can be expressed in terms of I_T . Thus,

$$i_2 - i_1 = I_T \frac{1}{1 + \frac{R_5}{R_2}} - \frac{I_T}{h_{fe1}} - \left[I_T \frac{h_{ie1}}{h_{fe1}} + V_{BE1} - V_{BE2} \right] \left[\frac{1}{R_3} + \frac{1}{R_2+R_5} \right]. \quad \text{III-17}$$

The first term in Equation III-17 does not contain any of the transistor parameters and should be the dominant term if the amount of hysteresis is to be independent of the transistors. This can be accomplished if R_2 and R_3 are made large and R_5 is small. However, this results in a large amount of hysteresis. By allowing the two negative terms to become appreciable, the hysteresis can be reduced. In fact, if the negative terms are larger than the positive term, the sign of $i_2 - i_1$ will be negative and there will not be any hysteresis in the amplifier.

This can be explained in terms of the transfer characteristics shown in Figure 9, Page 38. If the current difference $i_2 - i_1$, which will

FIGURE 9

STATIC TRANSFER CHARACTERISTICS OF
POSITIVE FEEDBACK AMPLIFIER

just bring Q_2 to the threshold of conduction, is negative, then the loop gain in the active region is less than one. In this case, starting at point A in Figure 9 and making $i_2 - i_1$ more positive, the path traveled from A to E is ABDE. However, if the current difference, $i_2 - i_1$, which will just bring Q_2 to the threshold of conduction is positive, then the loop gain in the active region is more than one and switching will occur. In this case, starting at point A as before, the path will be ABCDE with switching occurring between C and D.

In evaluating Equation III-17 it is difficult to determine the values that are appropriate to use for h_{ie1} and $V_{BE1} - V_{BE2}$. The term in which these parameters occur accounts for the difference in voltage between the two base terminals at the threshold of switching. Using the value of 18.5 ma for I_T , the data sheet for the 2N2219A indicates that a typical value for h_{ie} is 500 ohms.

If the theoretical equation

$$h_{ie} = r_b' + h_{fe} \frac{KT}{qI_E}$$

is used, and if

$$r_b' = 50 \text{ ohms}$$

$$I_E = I_T = 18.5 \text{ Ma, and}$$

$$h_{fe} = 85 \text{ (measured at } I_C = 20 \text{ Ma)}$$

then

$$h_{ie} = 50 + 85 \frac{26}{18.5} = 169 \text{ ohms.}$$

The actual voltage measured between the two bases just before switching occurred was approximately 65 millivolts. If V_{BE1} is assumed

to be equal to V_{BE2} then using the above values for I_T and h_{fe1} the value of h_{ie1} is found to be 307 ohms.

Since h_{ie} is a small signal parameter it is not theoretically correct to use it as a direct current resistance. However, the values above show that the effective resistance which is indicated in the equivalent circuit in Figure 7, Page 34, is approximately the same as h_{ie} .

Thus, the following values are used to evaluate Equation III-17:

$$I_T = 18.5 \text{ Ma}$$

$$h_{fe1} = 85 \text{ (measured value for } I_C = 20 \text{ Ma)}$$

$$I_T \frac{h_{ie1}}{h_{fe1}} + V_{BE1} - V_{BE2} = 65 \text{ Mv (measured in circuit)}$$

$$R_2 = 56 \text{ ohms}$$

$$R_3 = 150 \text{ ohms}$$

$$R_5 = 1,000 \text{ ohms}$$

Substituting (expressing currents in milliamperes and voltages in millivolts),

$$\begin{aligned} i_2 - i_1 &= 18.5 \frac{1}{1 + \frac{1000}{56}} - \frac{18.5}{85} - \left[65 \right] \left[\frac{1}{150} + \frac{1}{56+1000} \right] \\ &= 0.985 - 0.218 - 0.496 = 0.261 \text{ Ma} \end{aligned}$$

With these values it is observed that the negative terms are quite significant but that they would need to increase nearly 30 per cent in order for the loop gain in the active region to be less than one.

Hysteresis Referred to the First Stage Input

The hysteresis expressed in terms of the first stage input voltage can now be calculated. The transconductance, G , of the second stage

is equal to the voltage gain divided by the collector load resistance, R_L , which was used when the gain, A_2 , was calculated. Thus

$$G = \frac{A_2}{R_L} = \frac{17.6}{150} = 0.117 \text{ mhos.}$$

The cascaded transconductance, G_C , of the first and second stage is

$$G_C = A_1 G = 12.6 \times 0.117 = 1.48 \text{ mho}$$

where A_1 is the gain of the first stage.

The total hysteresis voltage referred to the input terminals of the first stage is

$$V_H = \frac{2(i_2 - i_1)}{G_C} = \frac{2 \times 0.261 \times 10^{-3}}{1.48} = 0.353 \text{ Mv.}$$

Using a low frequency sine wave, the actual measured minimum peak-to-peak input voltage which would cause switching was 0.385 Mv, which is in reasonably good agreement with the calculated value.

CHAPTER IV

DYNAMIC CHARACTERISTICS

Switching Speed Limitations of Transistors

In the DC analysis, no time effects were considered. Thus, if a signal just big enough to cause switching was applied, there was nothing to indicate that the output would not immediately change states. However, due to stray reactances in the circuit and even more important reactive effects inherent in the transistors, time delays are introduced which, though short (several hundredths of a microsecond), are not zero and thus the minimum signal would theoretically require an infinite amount of time to cause the output to switch states. For example, when a sine wave input signal is applied, the minimum amplitude input required to cause the feedback amplifier to switch is nearly constant until the frequency is increased to approximately one megacycle. Then, as the frequency is increased further, larger and larger input signals are required to cause switching.

Figure 10, Page 43, is a curve of minimum input versus frequency which was plotted from measurements made on the experimental circuit. Although some of the loss of sensitivity at high frequencies is caused by stray reactance in the circuit, the principal cause is the increased importance of capacity effects which are introduced into the circuit by the transistors. These same effects are always present, but at lower frequencies are negligible due to the slower rate of change of the signal.

FIGURE 10

MINIMUM PEAK-TO-PEAK SINE WAVE INPUT VOLTAGE REQUIRED
TO SWITCH OUTPUT OF EXPERIMENTAL COMPARATOR
VERSUS INPUT FREQUENCY

Causes of Transistor Switching Speed Limitations

Two mechanisms inherent in the transistors cause the capacity effects. Whenever a p-n junction, such as the emitter-base or the collector-base junction in a transistor, is reverse biased a field is set up around the junction which causes the mobile current carriers in the semiconductor to move away from the junction. This leaves many of the atoms with a net charge and gives rise to the capacity effect. The capacity effect thus introduced results in a capacity which is a function of the applied junction voltage. As the reverse bias is decreased, the incremental capacity increases. Figure 17, Page 64, shows curves of C_{BE} versus V_{BE} for the two transistors used in the first amplifier stage. The region where the mobile current carriers have moved away from the junction is called the transition or depletion region and the capacity is called the transition or depletion capacitance. A large supply voltage will minimize the collector to base transition capacity but will introduce errors due to the increased dissipation as discussed in Chapter III.

The second mechanism which causes capacitance effects occurs when the emitter base junction is forward biased and minority current carriers are injected into the base region. The density of these carriers is proportional to the emitter current. Assuming no field in the base region, the minority carriers move across the base to the collector by diffusion. When the emitter-base junction is quickly reverse biased after forward conduction, a reverse current will flow until these carriers have all been removed from the base region. If the reverse

bias voltage is supplied from a low impedance source, a large reverse current will flow until the carriers are removed. A large reverse current or turn-off drive will reduce the turn-off time. This capacity effect, which is proportional to current, is called the diffusion capacitance. The diffusion capacitance effect is minimized by using transistors with a very narrow base region, operating at low currents, and by preventing saturation which causes excess minority carriers in the base. Because of the circuit and transistor choice, the effects of the diffusion capacitance are minimized and the transition capacity effects dominate.

To obtain maximum switching speed with a transistor, the circuit impedance should be low so that the charge necessary to turn the transistor on or off can be supplied quickly by large currents. When this is attempted, it is found that the base current is limited by the resistance which occurs between the base terminal and the actual active base region of the transistor. Most of this undesirable base resistance occurs in the thin semiconductor material of the base. This resistance is usually called the base spreading resistance and is denoted by the symbol r_b' . Most of this resistance is strictly ohmic and is relatively independent of operating conditions. It is important because it reduces the base current during switching and its effects are considered in the analysis for each stage.

No information regarding r_b' is given on the 2N2219 or 2N1905 data sheets since this parameter is usually important only in RF amplifiers. However, the data sheets for the more completely specified

2N2219A include a collector base time constant curve and an approximate value of 50 ohms was calculated for r_b' from this information. The transient response of the complete circuit is not a strong function of r_b' , providing its magnitude is approximately as calculated. No effort was made to determine a more accurate value and 50 ohms is used in the calculations.

Justification for Neglect of Recombination

The calculations of the transient response of the comparator do not consider recombination of current carriers in the transistors. Little error is introduced by this simplification providing the switching time is short compared to the lifetime of current carriers in the active base region. Also, since recombination tends to increase turn-on time and decrease turn-off time, the effects tend to cancel in a differential amplifier circuit since both conditions must occur at the same time. Neglecting recombination in the transient analysis is the same as neglecting the loading effect of a subsequent stage when calculating the voltage gain of a stage as was done in Chapter III.

Method of Analysis

The switching speed or transient response of a transistor amplifier is often estimated in terms of the amount of charge which must be transferred. This method is particularly useful for large signal analysis where the capacity effects involved are very nonlinear and where constant current base drive may be assumed during the switching interval. In the comparator circuit, small signals applied to the

input of the first stage will cause switching in the positive feedback amplifier when the signal levels in the first two stages are small enough to use small signal or linear analysis. Linear analysis is easier to accomplish and since the first and second stages introduce the largest delays and errors in the transient response of the complete circuit, small signal response of the first two stages is considered first. The response to large input signals is then considered in less detail.

Transient Equivalent Circuit of Amplifier Stages

A complete schematic diagram of the entire comparator is shown in Figure 11, Page 48. This schematic includes capacitors, inductors, and diodes which improve the transient response but do not effect the low frequency response and were not included in the schematic shown in Figure 2.

The 1,000 pf capacitors in parallel with the 100 ohm series input resistors provide effective shunts for transients and the combination is considered a short and is not included in the equivalent circuit.

The center-tapped inductors function as peaking coils and their effect is considered later.

In the second stage two 5 pf feedback capacitors have been added, one from each collector to the opposite base. While the amplifier is in the active region, these capacitors are very effective in improving the transient response by reducing Miller effect caused by the collector to base capacity. The value of the capacitors has been chosen to be slightly less than C_{CB} and thus it is assured that the amplifier is

FIGURE 11

SCHEMATIC DIAGRAM OF COMPLETE COMPARATOR CIRCUIT INCLUDING
COMPONENTS ADDED TO IMPROVE DYNAMIC RESPONSE

completely stable. These capacitors are not completely effective in neutralizing or unilateralizing the effects of C_{CB} for very fast transients as it is not possible to reach the actual active base region of the transistors because of r_b' and because of the finite time required for current carriers to diffuse across the base region. Due to the cancelling of the effects of C_{CB} in the second stage, neither C_{CB} nor the "neutralizing" capacitors are included in the equivalent transient circuit.

The low storage diodes connected between the collectors of the feedback amplifier slightly decrease the delay time by reducing the amount of charge which must be transferred to initiate switching by biasing the transistors closer to the switching threshold during quiescent conditions.

In order to simplify calculations it is noted that if the equivalent capacitors, which are introduced by the transistors, are considered to be linear, and if the circuit and transistors are balanced, then all of the equivalent circuits are symmetrical along the center axis and may be bisected along this axis for purposes of transient analysis.

An example of bisection is shown in Figure 12, Page 50. Figure 12a is an equivalent circuit of the part of the base input circuit which is considered in determining the rise time of the first stage collector current. Since recombination is being neglected, it is appropriate to consider the transistors as voltage controlled devices in which the collector current is proportional to the voltage in the active base region. This is actually an unaccessible internal point though C_{CB} ,

(a)

(b)

FIGURE 12

SIMPLIFICATION OF SYMMETRICALLY BALANCED
CIRCUIT BY BISECTION

C_{BE} , and r_b' , are shown as external circuit elements. The simplified circuit shown in Figure 12b is obtained by bisecting the circuit shown in Figure 12a and by neglecting the resistance of the potentiometer which is small compared to the other resistance. Figure 13, Page 52, is the complete circuit which is obtained when this process is applied to the two first stages and the input to the positive feedback amplifier stage.

Usefulness of Equivalent Transient Circuit

Measurements made on the feedback amplifier and the output stage have shown that the actual time between the start of regeneration in the feedback amplifier when triggered by a slowly changing input and the time that the output voltage reaches 90 per cent of its final value, is less than 10 nanoseconds. A considerably longer time delay occurred between the application of a small step signal to the input of the first amplifier and the start of regeneration in the feedback amplifier.

The minimum static voltage difference which would just initiate switching when applied to the input terminals of the comparator was determined in Chapter III. In these calculations it was found that the base current for each stage was relatively small and that only a small voltage drop occurred across r_b' . For these small base currents the voltage in the active base region is very nearly equal to the terminal base voltage.

During rapid switching, a much larger base current flows because of the capacities which must be charged. This results in a significant

FIGURE 13

EQUIVALENT CIRCUIT USED FOR INVESTIGATION OF FIRST AND SECOND
STAGE AMPLIFIER TRANSIENT RESPONSE

difference between the terminal and the active base voltage. It is assumed that regeneration in the feedback amplifier starts at the time when the voltage difference between the active base regions of the transistors in the feedback amplifier is the same as the voltage difference at the threshold of switching which was determined in the static analysis.

The amplitude of the input voltages which are applied to the comparator to determine transient response can conveniently be expressed in terms of the static input voltage required to initiate switching.

The transient response of the amplifier is then considered in terms of the delay which is required to initiate switching in the feedback amplifier for the applied input voltage expressed as a ratio.

Rise Time of Collector Current in the First Stage

Examination of the equivalent circuit shown in Figure 13 reveals that there is a feedback loop which must be considered and that considerable effort would be required in order to find an analytical expression $E_0(t)$ for a given $E_1(t)$ even when E_1 is assumed to be a step function. When the actual values of the circuit parameters are considered it is apparent that additional simplifications can be made without introducing very large errors.

If only the part of the equivalent circuit which was shown in Figure 12b is considered, the response of the first stage collector current to a voltage step input can easily be calculated. If E_0 is assumed to be constant due to the loading caused by the part of the circuit which is not shown, no Miller effect occurs and a minimum response

time can be calculated. If E_0 is assumed to be related to V_b' by the low frequency voltage gain, Miller effect will reduce the rate of current increase and a maximum response time can be calculated. The actual response of the collector current is assumed to be between these two limits.

When E_0 is assumed constant, C_{CB} and C_{BE} may be considered in parallel and the collector current response to a step input is

$$i_c(t) = E_s g_m \left[1 - \exp \frac{t}{(R_S + r_b')(C_{CB} + C_{BE})} \right]$$

The final value is known from the static analysis so only the time constant

$$\tau_{\min} = (R_S + r_b')(C_{CB} + C_{BE}), \quad \text{IV-1}$$

is of interest.

When E_0 is assumed to vary according to the low frequency gain, the effective value of C_{CB} is increased by a factor of $(1+A)$. A maximum limit for the value of the time constant may be calculated.

$$\tau_{\max} = (R_S + r_b') [C_{CB}(1+A) + C_{BE}] \quad \text{IV-2}$$

By substituting in the following values

$$R_S = 25 \text{ ohms (50 ohm coaxial cable in parallel with a 50 ohm termination)}$$

$$r_b' = 50 \text{ ohms}$$

$$C_{CB} = 6.4 \text{ pf (average of measured values)}$$

$$C_{BE} = 45 \text{ pf (extrapolated value, see Figure 17, Page 64)}$$

$$A = 12.6$$

into Equations IV-1 and IV-2 it is found that τ must be between 3.86 and 9.77 ns.

Rise Time of Second Stage Base Voltage

When C_{CB} of the first and second stage are not included, the circuit shown in Figure 14, Page 56, may be used to find the active base voltage of the second stage as a function of time. In this Figure, I_C is the collector current of the first stage, R_C the first stage collector load resistance, V_b the terminal base-to-emitter voltage of the second stage, r_b' the second stage base spreading resistance, and $V_{b'}$ the active base-to-emitter voltage of the second stage.

The inductance, L , serves as a peaking coil and is chosen to provide the best overall comparator transient response. If no inductance is added ($L = 0$) the circuit is overdamped and the output voltage response to a step change in collector current is a simple exponential function of time. The time constant for $R_C = 330$ ohms, $r_b' = 50$ ohms, and $C_{BE} = 35$ pf (extrapolated from measured data) is

$$\tau = (R_C + r_b') C_{BE} = (330 + 50) 35 \times 10^{-12} = 13.3 \text{ ns}$$

If enough inductance is added to provide critical damping, the response to a step function is considerably improved though the general shape of the curve is about the same. If twice the inductance required for critical damping is added, the circuit will be underdamped and the output will overshoot if a step function input is applied. Figure 15, Page 57, shows the normalized voltage response of this circuit versus time for a step change in input current for these three cases. These curves are plotted from the following three equations which are developed in Appendix B.

FIGURE 14

SIMPLIFIED CIRCUIT OF INPUT TO ACTIVE BASE REGION
OF SECOND STAGE AMPLIFIER

FIGURE 15

THEORETICAL TRANSIENT RESPONSE OF SECOND STAGE BASE VOLTAGES VERSUS TIME FOR AN INPUT CURRENT STEP FOR OVER, CRITICALLY, AND UNDERDAMPED CONDITIONS

For $L = 0$ (overdamped):

$$V_b' = IR_C \left[1 - \exp \frac{-t}{(R_C + r_b')C_{BE}} \right] \quad \text{IV-3}$$

For $L = 1.26 \mu\text{h}$ (critical damped):

$$V_b' = IR_C \left[1 - \exp \frac{-t}{\sqrt{LC_{BE}}} \right] - I \sqrt{\frac{L}{C_{BE}}} \left[\frac{R_C}{L} - \frac{1}{\sqrt{LC_{BE}}} \right] t \exp \frac{-t}{\sqrt{LC_{BE}}} \quad \text{IV-4}$$

For $L = 2.52 \mu\text{h}$ (underdamped):

$$V_b' = IR_C - \left[IR_C \cos \left(\frac{1}{\sqrt{LC_{BE}}} - \frac{r_b' + R_C}{2L} \right) t - \frac{\frac{I}{C_{BE}} - \frac{I(r_b' + R_C)}{2L}}{\frac{1}{\sqrt{LC_{BE}}} - \frac{r_b' + R_C}{2L}} \sin \left(\frac{1}{\sqrt{LC_{BE}}} - \frac{r_b' + R_C}{2L} \right) t \right] \cdot \exp \frac{-(r_b' + R_C)t}{2L} \quad \text{IV-5}$$

Selection of Inductors

The actual inductances which were used in the experimental comparator were not selected by evaluating these equations in terms of the desired damping factor, but were determined experimentally by applying various input signals and then adjusting the inductors for the best overall transient response. This was done by making the inductance in each circuit as large as possible with a maximum limit set by not allowing the comparator to switch as the result of overshoot introduced by a large step input which just came up to the near side of the DC hysteresis level.

After the inductance had been adjusted, the coils, which were wound on small powdered iron toroids, were removed from the circuit and

the inductance was measured. The following inductances were found to have been selected for the collector circuits:

TABLE I
EXPERIMENTALLY DETERMINED INDUCTOR VALUES

Measured Across	1/2 of Inductor	Total Inductor
First Stage	2.7 μ h	10.2 μ h
Second Stage	0.40	1.4
Third Stage	0.15	0.49

As would be expected, smaller inductances were found to be optimum in the lower impedance stages. Also, these measurements indicate that the inductive coupling between the two halves of the windings was not as high as might be expected for a toroid.

The measured inductance for one-half of the first stage, 2.7 μ h, is only slightly larger than the inductance used to plot the underdamped curve shown in Figure 15, Page 57. This is a good indication that the inductors are functioning in the circuit in the expected manner. No calculations are made to justify the values of inductance chosen for the second and third stage collector circuits.

Prediction of Transient Response with Inductors

The curves shown in Figure 15, Page 57, can be used to show how the addition of the inductors can provide a significant improvement in the transient response for small input signals but very little improvement for large ones. Figure 16, Page 60, shows three input pulses which are applied to the input of a comparator which is assumed to have a total

FIGURE 16

PER CENT OF INPUT PULSE AMPLITUDE NECESSARY FOR
SWITCHING FOR DIFFERENT AMPLITUDE
INPUT PULSES

hysteresis of 0.5 Mv. Note that the base line for each of the three pulses is selected so that the pulse extends an equal distance above and below the center of the hysteresis band. If a 1 Mv pulse is applied it is seen that the input crosses the switching point when the voltage is 75 per cent of its final value. From Figure 15 it is observed that for the underdamped case shown, only about 9.5 ns is required to reach this point while about 18.5 ns is required for the overdamped case with no inductance.

If a 2 Mv pulse is applied, the input crosses the switching level at 62 per cent of its final value. For this pulse the times required for the voltage to reach the switching level for the overdamped and underdamped cases are approximately 7.5 ns and 13.5 ns respectively. For a very large pulse, which is centered on the hysteresis band, the switching level would be crossed at 50 per cent of the final value and the times for the above cases are approximately 5.5 ns and 9.0 ns respectively. If the input pulse is just equal to the hysteresis the switching point is 100 per cent of its final value. This point is reached in 19 ns for the underdamped case but is never reached for the overdamped case. In fact, it is possible for a pulse with an amplitude slightly less than the hysteresis to cause switching due to overshoot.

Two other conditions can also be considered. For example, if a large pulse is applied and the base, or initial value, is near the switching level so that the switching level is crossed at 5 per cent of the final value, the time required from Figure 15 is about 0.5 ns for all cases. The actual measured delay through the complete circuit

cannot be reduced to less than about 7 ns even with large signals. This is in part due to the limited drive available for the feedback stage and in part due to the fact that even very large drive currents cannot reduce the switching time below certain minimums.

The last example which is considered is when a large pulse is applied when the base, or initial value, is much below the final value so that the switching level is very slightly above the final value. For the underdamped case the overshoot is about 6 per cent so it appears that the output could switch and then switch back to the original state as the final value was approached. This condition was found to occur if the inductance was made larger than the final values which were experimentally chosen. However, this could not be made to occur using the shortest rise time pulse available with any amplitude input with the final inductance values.

In the preceding discussion the effects of the transient response of the base voltage of the feedback amplifier as a function of second stage collector current have not been considered. Thus the response of the complete circuit will be slower than has been predicted. By observing the values of the circuit parameters, it can be seen that the transient response of this part of the circuit is slightly faster than the preceding part and the overall response will be predominately determined by the part that has been considered. Also, since there would be no validity for using a step function input, a useful analysis would be much more complex.

Response to Large Input Signals

When large input signals are applied to the input of the comparator, one transistor in each of the two amplifier stages is cut completely off and the emitter-base junction is reverse biased. While a transistor is cut off no Miller effect can occur, and C_{CB} can be considered to be in parallel with C_{BE} . To bring the cut-off transistor to the threshold of conduction, charge must be supplied from the source through r_b' to these junction capacities. C_{CB} is fairly constant since the total voltage change is only a small fraction of the total voltage. It can be seen by reference to Figure 17, Page 64, that the large input voltages permissible between the first stage input terminals can cause C_{BE} to vary over a three-to-one range. Because of this large variation it is easier to estimate the time delay between the application of an input step and the time when the cut-off transistor reaches the threshold of conduction in terms of the charge which must be transferred rather than considering the nonlinear capacity.

For example, graphical integration by determining the area under the curve of Figure 17 shows that a charge of approximately 80×10^{-12} coulombs must be supplied to the emitter-base junction in order to change the emitter-to-base voltage from a reverse bias of 4.0 volts to a forward bias of 0.6 volts. Also, if the collector to base capacity is considered to be a constant 6 pf, an additional charge of approximately 28×10^{-12} coulombs must be supplied to the collector base junction. Thus a total charge of about 108×10^{-12} coulombs must be transferred. When this charge is supplied at a constant rate, the time delay could be

MEASURED BASE TO EMITTER CAPACITY VERSUS BASE TO EMITTER
VOLTAGE FOR TWO FIRST STAGE AMPLIFIER TRANSISTORS

easily calculated. For example, if the total series input resistance is 75 ohms, a 4.6 volt voltage step would cause an initial current of 53 Ma. If this current was maintained the delay time would be about 2 ns. In the actual circuit a constant current drive is only approximated for very large input voltage steps in which case the delay is negligible. The average input capacity over this voltage range is about 23 μ f which, with the 75 ohm input resistance, results in a time constant of 1.6 ns. Although this is quite short, large delays can result when the input signal is switched from a very large level to a level which is just enough to cause switching. These two extremes are illustrated by the photograph shown in Figure 23d, Appendix C.

In the second stage, because of the inductors, charge is supplied at more nearly a constant rate. Also, it is not possible to reverse bias the emitter base junction by more than about 0.2 volts. Thus the delay introduced by this stage is small.

Observed Transient Response

The transient response of the complete comparator to an input voltage step function is shown in Figure 18, Page 66. This data was taken by applying rectangular input pulses which were long compared to the response time. The DC level was adjusted so that the half amplitude point was centered in the hysteresis band. The 10 to 90 per cent rise time of both the input and output pulse was about 5 ns. The delay time was measured between the half amplitude point of the input pulse and the half amplitude point of the comparator output pulse. Curves are shown

FIGURE 18

MEASURED OUTPUT DELAY TIME VERSUS INPUT PULSE AMPLITUDE

with and without the inductors included in the circuit. It can be seen, as was previously indicated, that the inductors are of little value when the input pulse amplitude is large compared to the hysteresis.

The improvement in the transient response for small inputs is shown more clearly when this same data is plotted as shown in Figure 19, Page 68. Here the abscissa is the low frequency hysteresis as a per cent of input pulse amplitude. The overdrive ratio, which is defined as the ratio of the input pulse amplitude to the hysteresis, is also shown along the abscissa. It is observed that for small overdrive ratios the inductors provide a significant improvement. For small signals, larger overdrive ratios produce shorter delays. However, as the overdrive ratio becomes quite large, no further reduction in delay time results. This occurs when one transistor in the amplifier stage is driven to cut-off.

The positive curvature for overdrive ratios in the region 10 was not expected.

FIGURE 19

MEASURED OUTPUT DELAY TIME VERSUS HYSTERESIS
AS A PER CENT OF INPUT PULSE AMPLITUDE
OR OVERDRIVE RATIO

CHAPTER V

CONCLUSIONS

General

The characteristics of a voltage comparator which are particularly important for applications requiring sensitive high speed performance, were first considered. These included the impedance of signal source; the maximum allowable input voltage; recovery time after large input voltages; absolute accuracy; output transition time for slowly changing input signals; compatibility of output signal with other high-speed circuits; immunity to temperature, supply voltage, and load changes; and propagation time for various types of input signals.

A design which successfully incorporated these features into a relatively simple differential circuit configuration employing a high speed, non-saturating, positive feedback amplifier was presented. This circuit was analyzed to determine what factors imposed limitations on the accuracy and on the speed of response. Some important accuracy limitations were the imperfect matching of the components in the balanced circuits and transistor junction temperature unbalance due to unavoidable thermal resistance between the two junctions of each stage. The response time was principally limited by the transition capacitance associated with the transistor p-n junctions. The effect of this capacity was aggravated by the transistor base spreading resistance. A circuit using this design was built and electrically tested in order to verify the correctness of the assumptions which were made, and to check the complete

circuit performance. The theoretical and experimental results are summarized below.

Sensitivity

The basic sensitivity or hysteresis of the complete comparator to relatively slowly changing input signals was calculated to be 0.353 Mv. This was found to agree very closely with a measured value of 0.385 Mv. Higher voltage sensitivity could easily have been obtained at the expense of accuracy and high speed performance.

Accuracy

The accuracy or stability was found to be limited by the difference in junction temperature of the two transistors in each amplifier stage. The relatively high transistor dissipation required for high speed operation and the thermal resistance between the two junctions were the limiting factors. It was calculated that a maximum error of about 4.3 Mv could occur for large inputs. An improved thermal circuit would reduce this error. A lower bias current in the amplifier stages would improve the accuracy but reduce high speed performance.

Dynamic Response

The dynamic response was considered in terms of the delay which occurred between the application of various amplitude voltage steps and the resulting output. This delay was caused by the transition capacitance which is associated with the reverse biased p-n junction. It was shown that base spreading resistance made it difficult to charge these

capacities quickly. The dynamic response was improved for some conditions by the addition of shunt peaking coils and by cross-connected capacitors which reduce the effects of internal feedback. The delay time was found to vary from about 10 ns for large inputs (20 Mv or more) up to about 80 ns for signals of 0.5 Mv.

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BIBLIOGRAPHY

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APPENDIX A

INPUT BALANCE CIRCUIT "T" EQUIVALENT

APPENDIX A

INPUT BALANCE CIRCUIT "T" EQUIVALENT

The circuit used to balance the input terminals of the amplifier is shown in Figure 20a, Page 76. This circuit was used to avoid the difficulty of obtaining a low resistance infinite resolution potentiometer. In Figure 20b, this circuit is redrawn to emphasize the " π ". The value of p is determined by the potentiometer setting and is between zero and one. By use of the π to T transformation, Figure 20b is equivalent to Figure 20c if

$$Z_1 = \frac{Z_a Z_c}{Z_a + Z_b + Z_c} = \frac{5 [200(1-p)]}{205} \approx 5(1-p) \text{ ohms}$$

$$Z_2 = \frac{Z_b Z_c}{Z_a + Z_b + Z_c} = \frac{5 [200(p)]}{205} \approx 5(p) \text{ ohms}$$

$$Z_3 = \frac{Z_a Z_b}{Z_a + Z_b + Z_c} = \frac{200(1-p)200p}{205} \approx 200(1-p)p \text{ ohms.}$$

When $p = 0.5$, Z_3 has a maximum value of 50 ohms. Since Z_3 is in series with the very large equivalent resistance of the constant source, Z_3 may be neglected. Thus the original circuit is very nearly equivalent to the desired circuit shown in Figure 20d.

FIGURE 20

TRANSFORMATION OF INPUT BALANCE CIRCUIT
TO EQUIVALENT "T"

APPENDIX B

DEVELOPMENT OF EQUATIONS USED TO SHOW
EFFECTS OF PEAKING COIL

APPENDIX B

DEVELOPMENT OF EQUATIONS USED TO SHOW EFFECTS OF PEAKING COIL

The circuit shown in Figure 21, Page 79, is analyzed to determine the transient response of $e_2(t)$ for a step change in current, i . Solutions are determined for the underdamped, critically damped, and overdamped ($L=0$) cases using Laplace transformations.

$$\frac{I}{S} = \frac{E_1}{R_C + SL} + \frac{E_1}{R_B + \frac{1}{SC}} = E_1 \left[\frac{R_B + \frac{1}{SC} + R_C + SL}{(R_C + SL)(R_B + \frac{1}{SC})} \right]$$

$$E_1 = \frac{I(R_C + SL)(R_B + \frac{1}{SC})}{S(R_B + R_C + \frac{1}{SC} + SL)}$$

$$E_2 = E_1 \frac{\frac{1}{SC}}{R_B + \frac{1}{SC}} = \frac{I(R_C + SL)(R_B + \frac{1}{SC})}{(R_B CS + 1) \left[S(R_B + R_C) + (\frac{1}{C} + S^2 L) \right]}$$

$$= \frac{I(R_C + SL)}{S \left[S^2 LC + SC(R_B + R_C) + 1 \right]}$$

B-1

Overdamped:

$$L = 0$$

$$E_2 = \frac{IR_C}{S \left[SC(R_B + R_C) + 1 \right]}$$

$$e_2(t) = IR_C \left[1 - \exp \frac{-t}{(R_B + R_C)C} \right]$$

B-2

FIGURE 21

SIMPLIFIED BASE DRIVE CIRCUIT WITH
SHUNT PEAKING INDUCTANCE

Critically damped:

$$E_2 = \frac{I \frac{1}{C} \left(\frac{R_C}{L} + s \right)}{s \left[s^2 + s \left(\frac{R_B + R_C}{L} \right) + \frac{1}{LC} \right]} \quad \text{B-3}$$

The denominator is of the form

$$s(s^2 + 2s d f + f^2)$$

where

$$d = \frac{R_B + R_C}{2L} \sqrt{LC} = \frac{1}{2}(R_B + R_C) \sqrt{\frac{C}{L}} = \text{damping factor} \quad \text{B-4}$$

and

$$f = \frac{1}{\sqrt{LC}}.$$

For critical damping, $d = 1$, therefore

$$L = \frac{(R_B + R_C)^2 C}{4} \quad \text{B-5}$$

and

$$E_2 = \frac{I \frac{1}{C} \left(\frac{R_C}{L} + s \right)}{s(s+f)^2} \quad \text{B-6}$$

The Roots are $S_1 = 0$ and $S_2 = S_3 = -f$.

For $S_1 = 0$

$$e_2(t) = \frac{\frac{I}{C} \frac{R_C}{L}}{f^2} = I R_C$$

For $S_2 = S_3 = -f$

$$\phi(s) = \frac{\frac{I}{C} \left(\frac{R_C}{L} + s \right)}{s} \quad \phi'(s) = \frac{s \frac{I}{C} - \frac{I}{C} \left(\frac{R_C}{L} + s \right)}{s^2}$$

$$e_2(t) = \left[\frac{\frac{I}{C} \left(\frac{R_C}{L} - f \right)}{-f} t + \frac{-f \frac{I}{C} - \frac{I}{C} \left(\frac{R_C}{L} - f \right)}{f^2} \right] e^{-ft}.$$

The complete solution for critical damping is

$$e_2 = IR_C - \left[I \sqrt{\frac{L}{C}} \frac{R_C}{L} - \frac{1}{\sqrt{LC}} t + IR_C \right] \exp \frac{-t}{\sqrt{LC}}. \quad B-7$$

Underdamped:

By partial fractions B-3 becomes

$$E_2 = \frac{IR_C}{s} + \frac{\frac{I}{C} - IR_C \frac{R_B + R_C}{L} - IR_C s}{s^2 + s \left(\frac{R_B + R_C}{L} \right) + \frac{1}{LC}}. \quad B-8$$

The denominator of the second term can be rewritten as

$$\begin{aligned} s^2 + s \left(\frac{R_B + R_C}{L} \right) + \frac{1}{LC} &= s^2 + 2s \cdot df + f^2 \\ &= (s + fd)^2 + [f(1-d)]^2 \end{aligned}$$

The inverse transform will be of the form³

$$\frac{e^{-fd t}}{f(1-d)} \left[\phi_i \cos f(1-d)t + \phi_r \sin f(1-d)t \right]$$

where ϕ_r and ϕ_i are the real and imaginary parts of

$$\phi \left[-fd + if(1-d) \right]$$

³C. R. Wylie, Jr., Advanced Engineering Mathematics. New York: McGraw-Hill Book Company, 1951. p. 172.

The complete solution of Equation B-8 for the underdamped case is

$$e_2 = IR_C + \left[\frac{\frac{I}{C} - \frac{I(R_B+R_C)}{2L}}{\frac{1}{\sqrt{LC}} - \frac{R_B+R_C}{2L}} \sin \left(\frac{1}{\sqrt{LC}} - \frac{R_B+R_C}{2L} \right) t - IR_C \cos \left(\frac{1}{\sqrt{LC}} - \frac{R_B+R_C}{2L} \right) t \right] \exp \frac{-(R_B+R_C)t}{2L} \quad \text{B-9}$$

Equations B-2, B-7, and B-9 are presented as Equations IV-3, IV-4, and IV-9 in Chapter IV. The following values were substituted into these three equations in order to obtain numerical values:

$$R_C = 330 \text{ ohms}$$

$$R_B = 50 \text{ ohms}$$

$$C = 35 \text{ pf}$$

$$L = 1.26 \text{ } \mu\text{h (critical damping, } d=1)$$

$$L = 2.52 \text{ } \mu\text{h (overdamped, } d = .707)$$

Each equation was divided by 330I. Figure 15, Page 57, was plotted from the points in Table II, Page 83, which was obtained by evaluating the following equations for values of t:

$$\frac{e_2}{330I} = 1 - e^{-\frac{t(\text{ns})}{13.3}} \quad (\text{overdamped})$$

$$\frac{e_2}{330I} = 1 - \left[.0677t(\text{ns}) + 1 \right] e^{-\frac{t(\text{ns})}{6.64}} \quad (\text{critical damping})$$

$$\frac{e_2}{330I} = 1 - \left[1.52 \sin 1.77t(\text{ns}) - \cos 1.77t(\text{ns}) \right] e^{-\frac{t(\text{ns})}{13.3}} \quad (\text{underdamped})$$

TABLE II

THEORETICAL TRANSIENT RESPONSE OF BASE VOLTAGE FOR
OVER-, CRITICALLY, AND UNDERDAMPED CONDITIONS

t(ns)	Overdamped	Critically Damped	Underdamped
2	.140	.150	.209
4	.260	.302	.401
6	.363	.410	.550
8	.452	.527	.672
10	.528	.626	.766
12	.594	.700	.844
14	.650	.762	.908
16	.700	.812	.959
18	.742	.854	.988
20	.777	.882	1.014
22	.801	.911	1.032
24	.835	.938	1.047
26	.858	.945	1.057
28	.878	.957	1.063
30	.899	.967	1.061

APPENDIX C

EXPERIMENTAL EQUIPMENT, TEST SETUP, AND

MISCELLANEOUS TEST RESULTS

APPENDIX C

EXPERIMENTAL EQUIPMENT, TEST SETUP AND MISCELLANEOUS TEST RESULTS

The comparator circuit shown in Figure 11, Page 48, was built on a copper clad circuit board so that measurements could be conveniently made on the complete circuit. All of the NPN transistors are Type 2N2219 and all of the PNP transistors are Type 2N2905. The manufacturer's data sheets for these transistors are reproduced in Appendix D. The two transistors in each stage were selected from a group to obtain the best matched pairs possible using the base-to-emitter voltage drop (measured with an Electronic Associates Type 5001 Digital Voltmeter) and the common emitter collector characteristics (displayed on a Tektronix Type 575 Transistor Curve Tracer) as the matching criteria.

Most of the input signals which were applied to the comparator during testing were supplied from a 1000 to 1 voltage divider. This was done because the oscilloscopes which were available could not be used to provide a DC coupled display of the small signals used for testing and because the attenuators on the signal generators which were used did not provide accurate amplitude control for small signals. When using the 1000 to 1 voltage divider, signals which were measured in volts were recorded as millivolts. Figure 22, Page 86, is a block diagram which is an example of how the voltage divider was used to display the hysteresis loop shown in Figure 24, Page 89.

Photographs of both sides of the comparator circuit board are shown in Figure 23, Page 88. The top photograph shows the dual heat

FIGURE 22

BLOCK DIAGRAM OF EQUIPMENT SETUP USED FOR DYNAMIC TESTS
ON EXPERIMENTAL COMPARATOR

sinks which were used on the first and second stage transistors. Also visible in this photograph are the input and output coaxial connectors and capacitors and protective zener diodes which were placed across the supply voltage busses. The bottom photograph shows the wiring and components which were used. Included in this view are the resistors which formed the voltage divider used to obtain the various supply voltages from one voltage source. A switch, used to provide an AC coupled input, and a potentiometer, used to apply various input bias levels, are also visible though these additional circuits, which were convenient for some testing, are not included in the schematic diagram shown in Figure 11.

Tables III, IV, and V list the experimentally measured values which were used to plot the curves shown in Figures 10, 17, and 18 and 19 respectively.

(Top View)

(Bottom View)

FIGURE 23

PHOTOGRAPHS OF EXPERIMENTAL COMPARATOR CIRCUIT BOARD

Input signal to vertical amplifier is DC coupled with zero volts in center for all photographs except (d) where zero volts is at the base of the input pulse. In photographs (c) and (d), rise times are limited by oscilloscope response to 15 ns.

(a) Vertical 1 Mv/cm Horizontal 5 μ S/cm

Input 2.4 Mv peak-to-peak 50 Kc sine wave. Output vertical scale not calibrated.

(b) Vertical 1 Mv/cm Horizontal 1 Mv/cm

Static hysteresis loop. Vertical inputs same as (a). Sine wave also applied to horizontal. Width of hysteresis loop is approximately 350 μ V.

(c) Vertical 1 Mv/Cm Horizontal 100 ns/Cm

Input 2 Mv 380 ns pulse. Output vertical scale not calibrated.

(d) Vertical 1 Volt/Cm Horizontal 100 ns/Cm

Input 2.6 volt 380 ns pulse. Output vertical scale is not calibrated.

FIGURE 24

PHOTOGRAPHS OF INPUT AND OUTPUT OSCILLOSCOPE WAVEFORMS
OBTAINED WITH EXPERIMENTAL COMPARATOR

TABLE III

MINIMUM PEAK-TO-PEAK SINE WAVE INPUT VOLTAGE REQUIRED
TO SWITCH OUTPUT OF EXPERIMENTAL COMPARATOR
VERSUS INPUT FREQUENCY

Input Frequency (Mc)	Peak-to-Peak Sine Wave Input Voltage	
	Figure 5 Circuit (Mv)	Figure 11 Circuit (Mv)
0.1	.385	.385
0.2	.385	.385
0.4	.385	.385
0.6	.385	.385
0.8	.385	.385
1.0	.385	.385
1.5	.410	.385
2.0	.430	.385
2.5	.455	.400
3.0	.520	.405
4.0	.660	.420
5.0	.820	.450
6.0	1.00	.480
7.0	1.22	.630
8.0	1.45	.750
9.0	1.70	.950
10.0	2.00	1.25
12.5	3.20	1.90
15.0	4.00	2.60
20.0	7.40	4.40
25.0	12.0	9.50

All measurements were made with a Tektronix Type 545A oscilloscope using a Type 1A1 plug-in amplifier and a General Radio Type 1330-A oscillator.

TABLE IV
FIRST AND SECOND STAGE TRANSISTOR JUNCTION CAPACITIES
VERSUS JUNCTION BIAS VOLTAGE

Transistor Type Identification	2N2219(NPN)		2N2905(PNP)	
	#24	#25	#44	#45
Forward Bias (Volts)	C_{BE} (pf)	C_{BE} (pf)	C_{BE} (pf)	C_{BE} (pf)
.45	34.4	38.3	32.2	30.1
.40	31.9	34.4	29.2	27.5
.35	30.0	32.6	27.6	26.2
.30	28.5	30.8	26.2	24.9
.25	27.6	29.7	24.9	23.8
.15	25.5	27.6	23.3	22.1
0.00	23.4	25.4	21.0	20.0
-0.25	20.8	22.7	18.9	17.9
-0.50	19.4	20.7	17.3	16.5
-0.75	18.1	19.5	16.2	15.4
-1.0	17.1	18.4	15.4	14.5
-1.5	15.7	16.8	14.0	13.2
-2.0	14.5	15.5	12.9	12.2
-2.5	13.6	14.5	--	--
-4.0	11.7	12.4	10.5	9.7
	C_{CB}	C_{CB}	C_{CB}	C_{CB}
-8.0	5.14	5.94	6.01	6.12
-6.0	5.63	6.50	6.45	6.50
-5.5	5.78	6.70	--	--
-4.0	6.33	7.35	7.26	7.20
-2.0	7.78	8.98	9.36	8.70

All measurements were made with a Boonton Model 75A-S9 Capacitance Bridge.

TABLE V
OUTPUT DELAY VERSUS INPUT PULSE AMPLITUDE

Input Pulse (Mv)	Per Cent of DC Hysteresis (3.85 Mv)	Output Delay Time	
		With Inductors (ns)	Without Inductors (ns)
.5	78.0	90	220
.75	51.5	69	138
1.0	38.5	59	101
1.5	25.7	49	76
2.0	19.3	43	56
3.0	12.8	36	41
4.0	9.6	31	33
6.0	6.4	23	24
8.0	4.8	19	19
10	3.9	16	16
15	2.6	9.9	10
20	1.9	8.1	8.2
40	1.0	7.2	7.2

All measurements were made with a Fairchild Switching Time Tester Model G100 using a Tektronix Sampling Dual-Trace Preamplifier Type 3376 (risetime 0.4 ns) and a Hewlett-Packard Model 214A Pulse Generator.

APPENDIX D
TRANSISTOR DATA SHEETS

MOTOROLA Semiconductors

BOX 955 • PHOENIX 1, ARIZONA

SILICON ANNULAR STAR* TRANSISTORS

NPN

DESIGNED for
COMPLEMENTARY
HIGH-SPEED SWITCHING
APPLICATIONS and
DC to UHF AMPLIFIER
CIRCUITS

PNP

- High Uniform Beta from 0.1 to 500 mA.
- High Voltage Ratings
- Similar Switching Characteristics
- Low $V_{CE(sat)}$ — 0.4 V at 150 mA Maximum

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	NPN	PNP	Units
Collector - Base Voltage	V_{CBO}	60	60	Vdc
Collector - Emitter Voltage	V_{CEO}	30	40	Vdc
Emitter - Base Voltage	V_{EBO}	5	5	Vdc
Collector Current	I_C	800	600	mA dc
Total Device Dissipation @ 25°C Case Temperature To - 5: 2N2218, 2N2219 Derate Above 25°C	P_D	3 20		W mW/°C
2N2904, 2N2905 Derate Above 25°C			3 17.2	W mW/°C
To - 18: 2N2221, 2N2222 Derate Above 25°C		1.8 12		W mW/°C
2N2906, 2N2907 Derate Above 25°C			1.8 10.3	W mW/°C
Total Device Dissipation @ 25°C Ambient Temperature To - 5: 2N2218, 2N2219 Derate Above 25°C	P_D	0.8 5.33		W mW/°C
2N2904, 2N2905 Derate Above 25°C			0.8 3.43	W mW/°C
To - 18: 2N2221, 2N2222 Derate Above 25°C		0.5 3.33		W mW/°C
2N2906, 2N2907 Derate Above 25°C			0.4 2.28	W mW/°C
Operating Junction Temperature	T_J	-65 to +175	-65 to +200	°C
Storage Temperature	T_{stg}	-65 to +300	-65 to +300	°C

*Trademark of Motorola Inc.

†Manufactured by the annular process, Motorola patents applied for.

NPN

2N2218-2N2219

2N2221-2N2222

PNP

2N2904-2N2905

2N2906-2N2907

SILICON
ANNULAR† EPITAXIAL
COMPLEMENTARY
SWITCHING
TRANSISTORS

SEPTEMBER, 1963

DS 5057

TO-18

TO-5

TO-5 OUTLINE

TO-18 OUTLINE

SI HIGH-FREQUENCY TRANSISTORS
2N2218, 2N2219, 2N2221, 2N2222 (NPN)
2N2904 thru 2N2907 (PNP)
DS 5057

MOTOROLA Semiconductor Products Inc.

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PNP

FIGURE 15 — COLLECTOR SATURATION VOLTAGE versus BASE CURRENT

FIGURE 16 — BASE SATURATION VOLTAGE versus BASE CURRENT

FIGURE 17 — TEMPERATURE COEFFICIENTS

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FIGURE 12 — COLLECTOR SATURATION VOLTAGE versus BASE CURRENT

FIGURE 13 — BASE SATURATION VOLTAGE versus BASE CURRENT

FIGURE 14 — TEMPERATURE COEFFICIENTS

ELECTRICAL CHARACTERISTICS (At 25°C ambient unless otherwise noted)

Static Characteristic	Fig. No.	Symbol	Min	Max	Unit
Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{A}$, $I_E = 0$) All Types	---	BV_{CBO}	60	---	Vdc
Collector-Emitter Breakdown Voltage* ($I_C = 10 \text{ mA}$, $I_B = 0$) 2N2218-19, 2N2221-22 2N2904 thru 2N2907	9	BV_{CEO}^*	30 40	---	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{A}$, $I_C = 0$) All Types	---	BV_{EBO}	5	---	Vdc
Collector Cutoff Current ($V_{CB} = 50 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 50 \text{ Vdc}$, $I_E = 0$, $T_A = 150^\circ\text{C}$) 2N2218-19, 2N2221-22 2N2904 thru 2N2907	---	I_{CBO}	---	.01 .02 10 20	μA
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $V_{BE} = 0.5 \text{ Vdc}$) 2N2904 thru 2N2907	---	I_{CEX}	---	50	nA
Base Cutoff Current ($V_{CE} = 30 \text{ Vdc}$, $V_{BE} = 0.5 \text{ Vdc}$) 2N2904 thru 2N2907	---	I_{BL}	---	50	nA
Collector-Emitter Saturation Voltage* ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$) ($I_C = 500 \text{ mA}$, $I_B = 50 \text{ mA}$) All Types All Types	12, 15	$V_{CE(sat)}^*$	---	0.4 1.6	Vdc
Base-Emitter Saturation Voltage* ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$) ($I_C = 500 \text{ mA}$, $I_B = 50 \text{ mA}$) All Types All Types	13, 16	$V_{BE(sat)}^*$	---	1.3 2.6	Vdc
DC Forward Current Transfer Ratio ($I_C = 0.1 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$) ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$) ($I_C = 10 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$) ($I_C = 150 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$)* ($I_C = 500 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$)* 2N2218, 2N2221, 2N2904, 2N2906 2N2219, 2N2222, 2N2905, 2N2907 2N2218, 2N2221, 2N2904, 2N2906 2N2219, 2N2222, 2N2905, 2N2907 2N2218, 2N2221, 2N2904, 2N2906 2N2219, 2N2222, 2N2905, 2N2907 2N2218, 2N2221, 2N2904, 2N2906 2N2219, 2N2222, 2N2905, 2N2907 2N2218, 2N2221, 2N2904, 2N2906 2N2219, 2N2222, 2N2905, 2N2907	10 11	h_{FE}	20 35 25 50 35 75 40 100 20 30	---	---

Dynamic Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kc}$) All Types	4	C_{ob}	---	---	8	pf
Input Capacitance ($V_{BE} = 0.5 \text{ Vdc}$, $I_C = 0$, $f = 100 \text{ kc}$) ($V_{BE} = 2 \text{ Vdc}$, $I_C = 0$, $f = 100 \text{ kc}$) 2N2218-19, 2N2221-22 2N2904 thru 2N2907	4	C_{ib}	---	---	30 30	pf
Current Gain - Bandwidth Product ($I_C = 20 \text{ mA}$, $V_{CE} = 20 \text{ Vdc}$, $f = 100 \text{ mc}$) ($I_C = 50 \text{ mA}$, $V_{CE} = 20 \text{ Vdc}$, $f = 100 \text{ mc}$) 2N2218-19, 2N2221-22 2N2904 thru 2N2907	8	f_T	250 200	---	---	mc
Delay Time 2N2904 thru 2N2907	1	t_d	---	6	10	nsec
Rise Time 2N2904 thru 2N2907	1	t_r	---	20	40	nsec
Turn-On Time 2N2218-19, 2N2221-22 2N2904 thru 2N2907	1	t_{on}	---	26 26	---	nsec
Storage Time 2N2904 thru 2N2907	2	t_s	---	50	80	nsec
Fall Time 2N2904 thru 2N2907	2	t_f	---	20	30	nsec
Turn-Off Time 2N2218-19, 2N2221-22 2N2904 thru 2N2907	2	t_{off}	---	70 70	---	nsec
Total Switching Time All Types	3	t_{total}	---	12	---	nsec

*Pulse Test, Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$

PNP SWITCHING-TIME TEST CIRCUITS

For NPN Switching Tests, reverse diodes, polarities, and input pulses.

FIGURE 1 — SATURATED TURN-ON SWITCHING-TIME TEST CIRCUIT

FIGURE 2 — SATURATED TURN-OFF SWITCHING-TIME TEST CIRCUIT

FIGURE 3 — NON-SATURATED SWITCHING-TIME TEST CIRCUIT

FIGURE 4 — CAPACITANCE VARIATIONS versus VOLTAGE

FIGURE 5 — ACTIVE REGION TIME CONSTANT versus COLLECTOR CURRENT

FIGURE 6 — TOTAL CONTROL CHARGE versus BASE CURRENT

FIGURE 7 — NORMALIZED TURN-OFF TIME versus COLLECTOR CURRENT

NPN

FIGURE 8 — CURRENT GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

PNP

NPN

PNP

FIGURE 9 — COLLECTOR CURRENT versus MINIMUM COLLECTOR-EMITTER BREAKDOWN VOLTAGE

FIGURE 10 — LOW CURRENT GAIN

FIGURE 11 — HIGH CURRENT GAIN