ON THE DESIGN OF CAMAC BRANCH DRIVERS*

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ABSTRACT

An interface for the CAMAC branch highway to a computer is called a branch driver. The design of a branch driver with various capabilities is studied and the modular aspects of the design are explored. The design is divided into three sections, namely, computer, branch highway and internal. This approach has been implemented on the PDP8 and the PDP15 and also, in the near future, on the PDP11 computer.

SUMMARY

CAMAC systems can be assembled in many ways by using suitable modules. The modules can either be designed in house or purchased from commercial vendors. A branch highway is used for linking more than one crate. Also, the branch highway communicates to a particular computer by an interface called the branch driver.

The CAMAC system specifies a particular command (instruction) set which contains the external field address and the function to be executed. A branch driver can randomly access any address location. In an actual experimental or control situation, an event may require the generation and execution of a set of CAMAC commands. Also, rapid handling of interrupts is desirable. These system requirements place severe performance requirements on the design of branch drivers. A simple branch driver can handle programmed input output transfers and treats branch demand (interrupt) as a program interrupt to the CPU. On the other extreme, the branch driver can be a microprogrammable computer.

A branch driver consists of three separate sections:

1. Computer Section. This consists of special line receivers/drivers, address generation, control, etc., to communicate with a particular computer.

2. Branch Highway Section. This con-

sists of a standard set of line receivers/drivers, control, cards, etc.

3. Middle Section. This section may have program I/O, multiple data channels, storage memory, fast interrupt handler, etc.

The first two sections are always required in any branch driver, while the third section determines the specification. Most of the parts in section 3 are modular. It is possible to put complete functions on p.c. boards, which can be interconnected by wire wrap techniques. These techniques can handle various computer word lengths.

This three section approach is shown in Fig. 1. The middle section's functional modules are as follows.

1. Data Register. A 24 bit register which can be written into or read from either the branch highway or computer.

2. EPCNA. This register contains the CAMAC command F (function), C (crate), N (station), A (subaddress). The E implies extended function and consists of address modifier bits for sequential scan, control, single/double word transfers, etc.

3. Control and Status. This contains the computer I/O address decoding, status information, and control timing of the branch driver.

4. DCH. This consists of the base address and word count register for a 1 cycle data channel.

5. LAM. This register holds the LAM information after a BG (read graded L) cycle and also generates the vector interrupt addresses.

TYPES OF TRANSFERS

The following is a brief review of the types of transfers that can be implemented in a branch driver. The transfers can be of data or control information.

1. Programmed I/O. This type of transfer is done under software control, i.e., software commands are sequenced to

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execute a set of events, which can be loading of registers, executing CAMAC cycles, BG, etc. As such, this type of transfer is very flexible and easily alterable by software.

2. Data Channel. Here, the transfers are completely done by hardware. The software supplies a set of parameters in the initialization process which consist of computer memory's base address, word count (number of transfers), EFCNA, number of CAMAC transfers, etc. The actual operation can be triggered by a software command or a LAM. In the 1 cycle type DCH operation, the base address and word count are resident in the branch driver and are incremented by one on every transfer from the branch driver. In the 3 cycle DCH, memory locations are used to store the base address and the word count. Each one of these takes a memory cycle to fetch the word, increment by one and restore the result to memory and another memory cycle for the actual transfer of information between memory and branch driver. Thus it takes three memory cycles to do a 3 cycle DCH; however, the total dead time can be more than this. In the case of the PDP15, it is more than 5 memory cycles.

3. Multiple Data Channels. Several of the 1 cycle or 3 cycle data channels can be used for concurrent tasks or sequential tasks.

BRANCH HIGHWAY SECTION Fig. 2

This section mainly contains the resistive terminations, line drivers and line receivers in accordance with EUR 4600e. When a branch highway cycle is not in progress all the lines are bussed off. This is a necessary condition if multiple branch drivers are to be used. The twenty-four data lines are bidirectional and these are separated into read and write lines for connection to the data register. The bus of the BRW drivers is enabled only if a CAMAC write function is to be executed. Similarly, the receiver bus is enabled only for CAMAC read functions. The control bus is enabled during the branch highway cycles.

COMPUTER SECTION

The design of this section depends mainly on the I/O bus structure of the computer used. The design is somewhat dependent on the features required, i.e., program I/O transfers, DCH, priority interrupt vectors, etc.

The simplest design is for program I/O transfers with skip polling of the interrupting devices and is shown in Fig. 3 for a PDP15 computer. The PDP15 has 18 bit word lengths and bidirectional data lines. All the lines on the computer I/O bus are buffered by line drivers/receivers. The data transfers from data register to PDP15 I/O bus are by either the lower 18 bits or the upper 6 bits. This selection is made by a data multiplexer switch. The data flow from the PDP15 to the data register is done by clocking either the lower 18 bits or the upper 6 bits into the data register. The EFCNA has 18 bits; 17 bits are for FCNA, and E has one bit for addressing all on-line crates.

A design is shown in Fig. 4 for a PDP8 computer with program I/O and DCH (data break in PDP8 terminology). PDP8 has a 12 bit word length and separate unidirectional busses for program I/O and DCH. The data multiplexers are used to form two 12 bit words from the data register, and then to route them to the accumulator inputs for program I/O and to the memory buffer for DCH operation. Similarly, transfer to the data and EFCNA register can be from the memory buffer or the accumulator. The DCH register supplies the base address in the 1 cycle DCH mode.

The LAM card stores the graded L information in response to a BG cycle, which can be initiated by software or by hardware in response to a branch demand. The priority encoders are used to generate the vector addresses of the LAM's. This is not currently being implemented on the PDP8 or PDP15. The branch demand is treated like a program interrupt and software issues a BG command and the 24 bit LAM information is stored in the data register for transfer to the accumulator of the computer.

The DCH card contains 8 sets of base address and word count in RAM cells. When a DCH set is selected the contents of that set from the RAM cell are transferred to the output base address and word register, both of which can be incremented. This card has an enable register (one bit for each DCH) which can be set by program I/O or LAM card. When a go type command is issued the DCH control will do back to back transfers for the enabled data channels.

MIDDLE SECTION

The functional blocks of this section are shown in Fig. 1. The 24 bit data register is built on 3 cards. The circuit

of a data bit is shown in Fig. 5. An input from the computer section is applied to the D input of an MC4015 latch and is latched in by a positive transition of the clock input terminal. An input from the branch highway is received by a suitable line receiver (SP384A). A store pulse first resets the latch and then sets it if the branch data line is high (not asserted). The negative true logic is used here. The 24 bits from the branch highway are latched in as one word. The data from the computer section is latched in as two words if the computer word length is less than 24 bits. Here, only a single buffer is shown. In case of 1 cycle DCH making back to back transfers, a set of 2 buffers is required. It is rather simple to have 8 or more buffer words by using memory cells.

The EFCNA card is shown in Fig. 6. The SN7489 RAM (random access memory) cells are used to store eight sets of EFCNA's and are transparent to loading of the EFCNA register for program I/O transfers. The N and A registers can be incremented and provide outputs for N = 23, 28, 30 and A = 15, 7 for sequential scan. The C register can be shifted up or set to a logical one state. The E and F are holding registers. The E has 2 bits for the sequential scan mode, which is controlled by the Q response from the branch highway. The modes available are

E	MODE
0 0	No Scan Operation
0 1	Horizontal Scan: Skip A's and N's with Q = 0
1 0	Vertical Scan
1 1	GL Scan

The horizontal scan is used for reading/writing modules located physically in a sequence. The scanner examines the Q response during each branch highway cycle, and if Q = 1, A is incremented; if Q = 0, A goes to zero and N is incremented. The N is incremented until Q = 1, then A is incremented. It takes a branch highway cycle to get the Q response from a station. However, data transfers to the middle sections are made only when Q is true. After reading N = 23 the crate number is incremented, N goes to one and A goes to zero and scan goes on.

The vertical scan is normally used for executing commands of fixed FNA with C incrementation. This mode is useful in executing the type A crate controller's commands like enabling branch demands under DCH operation.

The GL scan is like the horizontal scan but with N = 30, F = 0 and A = 0 to

7. It is used to read all GL registers in the system under DCH control.

One bit of E is used for single/double word format for DCH operation. In the one word format only 12 bits for the PDP8 and 18 bits for the PDP15 are transferred to and from the computer. While, in the two word format, another word transfers the rest of the bits.

Before starting a branch highway cycle the on-line status of the crate controllers is latched in and only the on-line crates are addressed. If an off-line crate is addressed, it will set an error flag.

The control and status card provides all the necessary timing and control for the branch driver. The instruction set is divided into two fields. The first field contains instructions like write branch driver registers from the accumulator, check status, issue BZ or BG, execute highway cycle, etc. The second field contains instructions like "Load EF/CNA from the accumulator, execute branch cycle and Jam transfer upper/lower data bits to accumulator if a read command was executed". The second field instructions are not implemented in the PDP15 branch driver because of I/O bus timing constraints.

The DCH controls can be arranged in two ways. The first can be thought of as eight independent data channels servicing modules which may be connected to peripherals. The second can be thought of as eight independent command sets which can be executed between the CAMAC system and the computer memory. In one operation any combination of the sets can be executed. Any CAMAC command can be specified in a set. A typical data acquisition arrangement may be as follows:

Set 1	Disable System	(FCNA) ₁
Set 2	Read 100 Single Words	constant (FCNA) ₂
Set 3	Read 20 Double Words	sequential (FCNA) ₃
Set 4	Read 10 Single Words	sequential (FCNA) ₄
Set 5	Write 20 Single Words	constant (FCNA) ₅
Set 6	Clear	Vertical SCAN (FCNA) ₆
Set 7	Enable CCA IAM	Vertical SCAN (FCNA) ₇
Set 8	Enable System	(FCNA) ₈

The system is disabled by Set 1, reads various lengths of data at different addresses in Sets 2 - 4, writes (display) in Set 5, clears latches, scalars, etc., in

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Set 6, enables LAM's in the crate controllers in Set 7 and enables the system in Set 8. Currently, this set arrangement has been implemented.

A custom data acquisition system can be designed to transfer data more efficiently than a CAMAC system with commercial modules. In a custom system, bit packing is for a particular computer while commercial CAMAC modules have different bit lengths. This arrangement of DCH sets allows faster data transfers and also keeps software micro control of the system in data channel mode.

CONSTRUCTION TECHNIQUES

Digital Equipment Corporation's M series hardware is used to build the branch driver. Standard cards are used for line drivers/receivers for both the branch highway and computer sections. The middle section cards are built by hand wiring on blank DEC boards. All the interconnections between the cards is by wirewraps. It is observed that most of the wirewraps are for data transfer and only a small number are for control functions. In the middle section, the data transfer wiring is mostly dependent on the computer word length and is essentially identical for two computers with the same word length.

In the designs implemented here, the pin assignments for the middle section cards are kept the same. This makes updating simpler.

CONCLUSIONS

The approach described here has been implemented for two computers. A PDP15 program I/O branch driver has been in use for more than a year and the data channels will be added in a few months. A PDP8 branch driver with eight sets of DCH has been in operation for a month. Also, work has started to implement this approach on a PDP11.

Fig. 1. Three Sections of a Branch Driver

Fig. 2. Branch Highway Section

Fig. 3. Computer Section--PDP15 Program 10

Fig. 4. Computer Section--PDP8 DCH

Fig. 5. Data Register

Fig. 6. EFCNA Card