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Computer Control of EPICS Beam Line and Spectrometer

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Computer Control of EPICS Beam Line and Spectrometer

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COMPUTER CONTROL OF EPICS BEAM LINE AND SPECTROMETER

by

J. P. Egger and Henry A. Thiessen

ABSTRACT

This report describes computer controls and checking of the EPICS channel and spectrometer using the CAMAC system and a PDP-11/45 computer interfaced with a microprogrammed branch driver (MBD).

I. INTRODUCTION

The EPICS beam line and spectrometer will be controlled locally with a PDP-11/45 computer (24 K memory, disk, magtape). A data link to the central control room (CCR) is planned, but there will be no control of the line equipment from CCR.

The general configuration of the line is shown in Figs. 1 and 2 which locate the computer controlled devices along the channel and spectrometer. The following devices are computer-controlled or computer-checked:

- bending magnets (NMR, H_t -windings, currents)
- quads (current)
- electrostatic particle separator (current, E-field voltage)
- slits (4 jaws, position)
- beam plug (position)
- target (position)
- veto counters and trigger scintillators (DC voltage check)
- helical proportional chambers (wire check)
- taut wire position indicators (alignment check)
- angle of spectrometer.

II. BENDING MAGNET CONTROL

The four bending magnets of the channel and the two of the spectrometer have a common power supply each. The control diagram is shown in Fig. 3. The power supply is turned on/off and the polarity reversed using one bit of a CAMAC 12-bit output register (Kinetic Systems KS 3082 or 3086). The power supply stepping motor

is driven with a CAMAC stepping motor driver made at Yale (Satish Dhawan). This driver can control 15 stepping motors. The field of the magnets is measured with a DVM multiplexed through a CAMAC multiplexer (Joerger AM). The DVM has a computer readout via a CAMAC 24-bit input register (KS 3470).

Each bending magnet has 6 to 8 H_t -windings. The control diagram of these H_t -windings is shown in Fig. 4. The H_t -windings currents are measured with a 64-channel ADC (5-D System) and readout through a CAMAC 24-bit input gate (KS 3420).

The field of each bending magnet will also be measured with a NMR probe. This probe will be driven by a M-093 stepping motor controlled with the Yale stepping motor driver. The type of computer-controlled NMR data read-out has not been decided yet.

III. QUADS AND ELECTROSTATIC PARTICLE SEPARATOR (EPS)

The quads and EPS are controlled in the same way as the bending magnets (see Fig. 3) except that there is no NMR control.

IV. PHOTOTUBE DC HV CHECK FOR SCINTILLATORS

The checking of the DC high voltages for scintillators is shown in Fig. 5. Like the H_t -windings control, these voltages are read out with a 5-D system (64-channel ADC's) and a CAMAC 24-bit input gate (KS 3420).

V. TAUT-WIRE POSITION INDICATOR CHECK

Groups of eight sensors of position in X and Y direction are multiplexed into a NIM 8-channel visual control module. The choice of display of one particular sensor is made with 3 bits of a CAMAC 12-bit output register (KS 3082 or 3086). The read-out is done through the 5-D system and the CAMAC KS 3420 input gate. The corresponding diagram is shown in Fig. 6.

VI. SLITS, TARGET, AND BEAM PLUG

All these devices are driven with stepping motors and CAMAC Yale stepping motor drivers. We have a computer read-out of the position and height of the target.

EPICS Beam Line

EB: Bending magnet
 S: Slit
 NMR: NMR probe
 H_t : H_t -winding
 EPS: Electrostatic Particle Separator
 T: Target
 BP: Beam plug

Fig. 1. Computer controls of EPICS beam line.

EPICS Spectrometer

EB: Bending magnet
 Q: Quadrupole magnet
 NMR: NMR probe
 H_t : H_t -winding
 V: Pole tip veto counter
 TS: Trigger scintillator
 H: Helical proportional chamber (MWPC)
 C: Čerenkov counter

Fig. 2. Computer controls of EPICS spectrometer.

Fig. 3. Magnet control without NMR.

Fig. 4. H_t -winding control.

Fig. 5. Phototube DC high voltage check.

TABLE I
CAMAC 12-bit Output Register, KS 3082/3086

COMMAND	ACTION
F(0)·A(0)	Gates actual state of relays onto Dataway.
F(6)·A(0)	Gates module identifying number onto Dataway.
F(8)·A(0)	Returns Q if LAM is set.
F(9)·A(0)·S1	Clears 12-bit register and clears LAM.
F(10)·A(0)·S1	Clears LAM.
F(11)·A(0)·S1	Presets 12-bit register and clears LAM.
F(14)·A(0)·S1	Sets LAM.
F(16)·A(0)·S1	Writes 12-bit register and clears LAM.
F(20)·A(0)·S1	Selectively clears ¹ 12-bit register and clears LAM.
F(22)·A(0)·S1	Selectively sets ² 12-bit register and clears LAM.
F(24)·A(0)·S1	Prevents setting of the LAM flip flop.
F(26)·A(0)·S1	Allows setting of the LAM flip flop.
F(28)·A(X)·S1 ³	Clears bit defined by Sub-address and clears LAM.
F(30)·A(X)·S1 ³	Sets bit defined by Sub-address and clears LAM.
C·S2	Clears LAM and 12-bit register.
Z·S2	Clears LAM and 12-bit register and prevents LAM from being set.

NOTES

- Let A = bit register before Dataway cycle,
B = data bit transferred during Dataway cycle,
C = resulting bit in register after Dataway cycle.
For Selective Clear, $C = A \cdot \bar{B}$
- Let A, B, and C be defined as above.
For Selective Set, $C = A + B$
- The Sub-address (X) may range from 0 through 11.

TABLE II

FORTRAN V003A		25-OCT-72
	C	'OUTTST' MAKING FRIENDS WITH OUTPUT REGISTERS
0001		IMPLICIT INTEGER (A-Z)
0002		COMMON F(3),N,A
	C	
	C	F(1)=CAMAC F COMMAND, F(2)=Q RESPONSE, F(3)=DATA
	C	N=CAMAC N COMMAND, A=CAMAC A COMMAND
	C	
	C	LOAD THE CONTROL MEMORY
	C	
0003		CALL LOADAL
0004		CALL LOADCN
0005		WRITE(6,2)
0006	2	FORMAT(' TYPE IN N-COMMAND OF MODULE PLEASE (FORMAT I2)')
0007		READ(6,1)N
0008	1	FORMAT(I2)
0009		A=0
0010		F(1)=6
0011		CALL MBDFNA(F,N,A)
0012		WRITE(6,4)F(3)
0013	4	FORMAT(' MODULE IDENTIFICATION NUMBER : KS',I5)
0014		F(1)=0
0015		CALL MBDFNA(F,N,A)
0016		WRITE(6,3)F(3)
0017	3	FORMAT(' STATE OF RELAYS : ',O5)
0018		F(1)=9
0019		CALL MBDFNA(F,N,A)
0020		WRITE(6,5)
0021	5	FORMAT(' MODULE CLEARED')
0022		F(1)=0
0023		CALL MBDFNA(F,N,A)
0024		WRITE(6,3)F(3)
0025		WRITE(6,6)
0026	6	FORMAT(' WRITE 12-BIT REGISTER IN OCTAL FORMAT 04')
0027		READ(6,7)F(3)
0028	7	FORMAT(04)
0029		F(1)=16
0030		CALL MBDFNA(F,N,A)
0031		READ(6,1)I
0032		F(1)=0
0033		CALL MBDFNA(F,N,A)
0034		WRITE(6,3)F(3)
0035		WRITE(6,8)
0036	8	FORMAT(' WRITE BIT (00-11) YOU WANT TO SET (FORMAT I2)')
0037		READ(6,1)A
0038		F(1)=30
0039		CALL MBDFNA(F,N,A)
0040		A=0
0041		F(1)=0
0042		CALL MBDFNA(F,N,A)
0043		WRITE(6,3)F(3)
0044		WRITE(6,9)
0045	9	FORMAT(' WRITE BIT (00-11) YOU WANT TO CLEAR (FORMAT I2)')
0046		READ(6,1)A
0047		F(1)=28
0048		CALL MBDFNA(F,N,A)
0049		A=0
0050		F(1)=0
0051		CALL MBDFNA(F,N,A)
0052		WRITE(6,3)F(3)
0053		END
BLOCK		LENGTH
MAIN		00682 (002524)*
\$\$\$		00005 (000012)

TABLE III

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RU OUTTST
TYPE IN N-COMMAND OF MODULE PLEASE (FORMAT I2)
15
MODULE IDENTIFICATION NUMBER : KS 3082
STATE OF RELAYS : 1573
MODULE CLEARED
STATE OF RELAYS : 0
WRITE 12-BIT REGISTER IN OCTAL FORMAT 04
4444

STATE OF RELAYS : 4444
WRITE BIT (00-11) YOU WANT TO SET (FORMAT I2)
00

STATE OF RELAYS : 4445
WRITE BIT (00-11) YOU WANT TO CLEAR (FORMAT I2)
11

STATE OF RELAYS : 445
$

```