HARDENING ELECTRONIC DEVICES AGAINST VERY-HIGH-TOTAL-DOSE RADIATION ENVIRONMENTS

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The possibilities and limitations of hardening silicon semiconductor devices to the high neutron and gamma radiation levels (greater than 10^{16} neutrons/cm^2 (1 Mev eq.) and greater than 10^8 rads (Si) required for the NERVA nuclear engine development are discussed. A comparison is made of the high dose neutron and gamma hardening potential of bipolar, metal insulator semiconductor (MIS), and junction field effect transistors (JFET). Experimental data is presented on device degradation for the high neutron and gamma doses. Previous data and comparisons[1,2,3] indicate that the JFET is much more immune to the combined neutron displacement and gamma ionizing effects than other transistor types. Presently, hardened JFET's degrade about 50% at 10^{16} neutrons/cm^2. Theoretically they can be improved, but the resulting hardened JFET's have low breakdown voltages (less than 20 volts). Experimental evidence (5 volt threshold shift at 10^8 rads) is also presented, which indicates that p channel MOS devices, made by Hughes Aircraft may be able to meet the requirements. Electrical characteristics compromises caused by device hardening and the ability to satisfy requirements on a practical reliable basis are discussed.

Introduction: If electronic components can be made to perform their function after total doses of 10^8 rads gamma and 10^{16} neutrons/cm^2, then many shielding and cabling problems would be eliminated in electronic control systems for nuclear engines, such as the NERVA. Even though the original work more than 10 years ago on radiation effects on electronic components was directed toward radiation environments near a nuclear reactor, relatively little effort has been specifically directed toward hardening transistors to these high total dose levels. The lack of apparent effort has been partly due to great difficulty in hardening the bipolar transistor (which has been by far the most used transistor type) to these high levels.

The three principal categories of radiation damage near a reactor are displacement, ionization, and heating. (It is assumed here that the heating is accounted for in the temperature specifications). The main cause of displacement damage is fast neutrons, and the main effects which permanently degrade transistor operation are minority carrier lifetime reduction and carrier removal. A second-order effect is mobility reduction. The main cause of ionization damage is gamma radiation which results in permanent effects due to charge build-up in the oxide and photo-current generation. The extent of the transistor degradation due to displacement and ionization damage depends strongly on the transistor types.

Transistors can be classified into 2 broad types, bipolar and unipolar. The unipolar is, however, usually referred to as a field effect transistor (FET), of which there are two basic types - the Junction FET (JFET) and the Insulated Gate FET (IGFET). The IGFET is often referred to generally as an MIS (metal insulator semiconductor) and specifically as an MOS, where the insulator is an oxide. The original reason for the designation of the two classes of transistors was that the unipolar operation depends on only one carrier (majority) and the bipolar operation depends on both minority and majority carriers. The bipolar is then seriously degraded by minority carrier lifetime reduction, whereas the unipolar or field effect transistor is not. One of the two principal classes of field effect transistors, the junction field effect transistor (JFET), depends strongly on carrier removal. However, the insulated gate (MIS) is little affected by either carrier removal or lifetime changes, but is very sensitive to permanent charge build-up in the insulator caused by ionizing radiation. The bipolar and JFET suffer only minor effects due to charge build-up in the oxide passivation when compared to the MOS. This is because the active region of the MOS is adjacent to or part of the oxide layer.

Since the electrical changes in the transistor operating characteristics induced by radiation damage to materials properties vary considerably with the transistor type, it is necessary to consider "hardening" each device separately. Electronic device hardening is essentially the science of designing the device to minimize the functional dependence of the device's electrical characteristics on known radiation sensitive materials properties.

JFET Hardening: If the JFET is operated in the region of maximum transconductance, g_m, the g_m is given[4] by:

$$g_m = \frac{2Nq\mu a}{L}$$

where

- N = majority carrier concentration in the channel, either n or p
- q = the electronic charge
- μ = the mobility
- a = the channel width
- L = the channel length.

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It should be noted that if the JFET is operated in a region other than for maximum g_m, the g_m has a weaker dependence on N than the linear one given by this expression. It has been shown[2,5] that the normalized neutron induced transconductance degradation for silicon JFET's is given by:

$$\frac{g_{m\Phi}}{g_{mo}} = \exp\left(-\frac{\Phi}{K}\right) = \frac{N_\Phi}{N_o}$$

where

$$K = K_p = 398\ P_o^{.77} \text{ for a p type channel and}$$

$$K = K_n = 93\ N_o^{.82} \text{ for an n type channel.}$$

Where N_o and P_o are carrier concentrations before irradiation, g_{mo}, $g_{m\Phi}$ are the maximum transconductances before and after irradiation. These relations were derived by: 1) using the above standard JFET parameter relations, 2) assuming that carrier removal in the JFET channel is the only degradation mechanism, 3) using Stein's[6,7] initial carrier removal data and assuming the exponential law, $N = N_o \exp(-\frac{\Phi}{K})$. The theoretical g_m degradation is plotted in Fig. 1 for both n and p type channels. Since the n channel devices both theoretically and actually show less degradation and n type material has a higher mobility resulting in initially higher g_m, the results of tests on n channel JFET designs only will be reported in this paper.

The method of increasing the neutron radiation tolerance of JFET's is clearly then to heavily dope the channel. This cannot be done without some compromise, since the pinch-off voltage of the JFET must be less than the avalanche breakdown voltage and the pinch-off voltage increases with channel doping while the breakdown voltage decreases. It is fortuitous, however, that satisfying this hardening requirement actually increases the JFET gain.

The g_m and source to drain current degradation are shown in Fig. 2. Typical on resistance after $5X10^{15}$ neutrons/cm^2 is 150 ohms and after 10^{16} neutrons/cm^2 is 250 ohms. Typical leakage currents are shown in Table 1.

TABLE 1

TYPICAL LEAKAGE CURRENT CHANGES FOR JFET'S

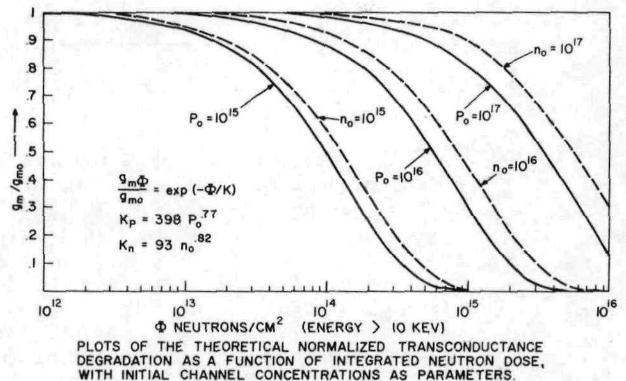
I_{DSS} RANGE 20-48 ma

GAMMA DOSE IN RADS

	0	$3.7X10^6$	$2.7X10^7$	$1.6X10^8$
GATE DRAIN				
LEAKAGE	$2.3X10^{-12}$	$3.4X10^{-11}$	$2.6X10^{-10}$	$2.7X10^{-10}$
AT 5V	$1.4X10^{-11}$	$5.1X10^{-11}$	$1.9X10^{-10}$	$2.1X10^{-10}$
RAD 201	$2.1X10^{-12}$	$3.2X10^{-11}$	$2.4X10^{-10}$	$3.1X10^{-10}$

NEUTRON DOSE AND GAMMA DOSE

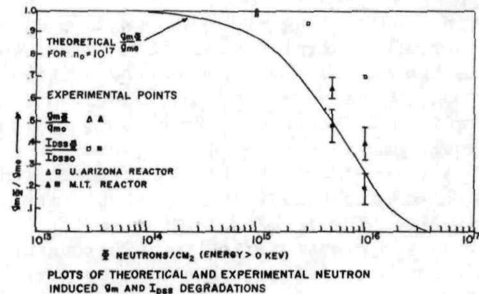
	0	$5X10^{15}$ n/cm^2	10^{16} n/cm^2
GATE DRAIN		$1.3X10^8$ rads	$2.6X10^8$ rads
LEAKAGE			
AT 10V	$3.3X10^{-12}$	$1.1X10^{-9}$	$2.6X10^{-9}$
RAD 201	$9X10^{-12}$	$1.6X10^{-9}$	$3.5X10^{-9}$



PLOTS OF THE THEORETICAL NORMALIZED TRANSCONDUCTANCE DEGRADATION AS A FUNCTION OF INTEGRATED NEUTRON DOSE, WITH INITIAL CHANNEL CONCENTRATIONS AS PARAMETERS.

AFCRL PHOTO 129-377

Figure 1



PLOTS OF THEORETICAL AND EXPERIMENTAL NEUTRON INDUCED g_m AND I_{DSS} DEGRADATIONS

Figure 2

The electrical characteristic penalty for hardening JFET's is then the resulting low breakdown voltage. Even though some increase above the bulk breakdown voltage can be achieved by grading the doping profile near the surface,[8] a breakdown voltage requirement above 40 volts cannot be satisfied simultaneously with 10^{16} neutrons/cm^2. The ionizing radiation even at the very high levels has negligible effect on the JFET.

Simplified Bipolar Hardening Relations: Using the charge control approach a simplified expression for β can be shown[9] to be

$$\beta = \frac{\tau}{t_b}$$

where τ is the minority carrier lifetime in the base and t_b is the base transit time. The base transit time is proportional to the square of the basewidth. The usual relation between the lifetime before and after a dose of Φn/cm^2 is assumed:

$$\frac{1}{\tau} = \frac{1}{\tau_o} + \frac{\Phi}{K\tau}$$

where τ_o is the lifetime before irradiation and K_τ is the lifetime damage constant. From these relations we obtain

$$\frac{\beta_\Phi}{\beta_o} = \frac{1}{1 + \Phi\tau_o/K_\tau}$$

where β_Φ and β_o are respectively the gain before and after irradiation. This is, of course, a greatly simplified expression for neutron induced β degradation, since other parameters, such as emitter efficiency are neglected. A good indication of neutron induced β degradation is given by this expression, however, which clearly points out the importance of "killing" lifetime to harden against permanent gain degradation (see Fig. 3). A plot of the simplified theoretical bipolar hardness and actual experimental points are compared to the JFET theoretical and actual hardness in Fig. 4. It should be noted that the low injection value of K_τ is used, which is compensated for in the comparison by using the high estimate for carrier removal rate. In addition to neutron damage, significant degradation occurs for ionizing radiation, especially for μ amp collector currents as is clearly shown in Fig. 5.

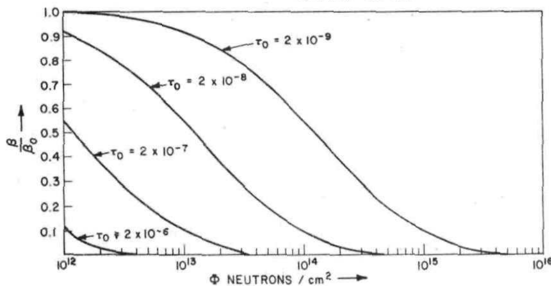
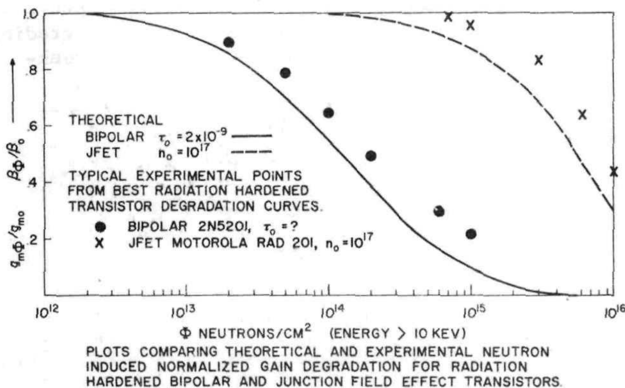


Figure 3
Plot of fractional beta degredation as a function of neutron dose.



PLOTS COMPARING THEORETICAL AND EXPERIMENTAL NEUTRON INDUCED NORMALIZED GAIN DEGRADATION FOR RADIATION HARDENED BIPOLAR AND JUNCTION FIELD EFFECT TRANSISTORS.

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Figure 4

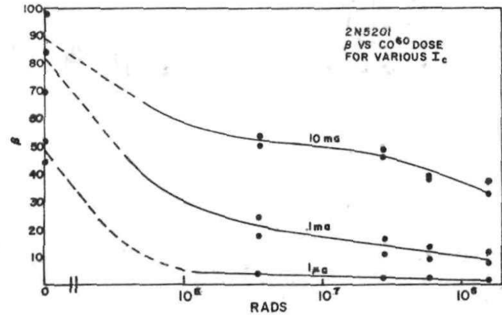

Figure 5

MIS Hardening: The effects of ionizing radiation on the transfer characteristic of a typical MOS transistor is illustrated in Fig. 6. The entire characteristic curve is seen to shift with integrated dose. The point on the curve at which the drain current I_d equals zero is referred to the "pinch off", "turn on" or "threshold" voltage V_T. Henceforth, unless otherwise noted, when reference is made to a shift in V_T, it is also meant that every point on the curve is shifted by the same amount as the threshold voltage shift. This is not true in all cases since the curve is sometimes shifted and distorted, but it is a good approximation for a simplified discussion. There is general agreement[10,11] as to the basic mechanisms that cause the threshold shifts in an ionizing radiation environment: a) the build-up of a positive space charge within the oxide by the occupation of pre-existing charge-trapping sites in the oxide and b) the creation of so called "fast surface states" at the oxide-silicon interface. Mechanism (a) seems to occur to some extent in all insulators and to be a strong feature of amorphous insulators of very low conductivity. Mechanism (b) does not seem to occur in all MIS systems. The charge build-up mechanism causes the largest threshold shifts in most cases and is much better understood than the fast surface states. The magnitude of a radiation induced threshold shift is strongly dependent on the processing of the MIS devices. The magnitude of a radiation induced threshold shift is usually an even stronger function of the bias on the MOS during irradiation. Most commercial MOS transistors show threshold shifts of 40 or more volts with a bombardment bias of less than 10 volts and a bombardment dose of approximately 10^6 rads. In addition to the regular (even though statistically varying) effects mentioned above other anomalous radiation effects, including room temperature instabilities have been reported.[10,12]

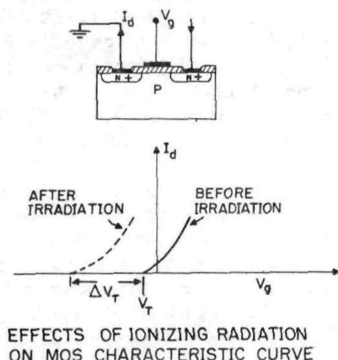

Figure 6

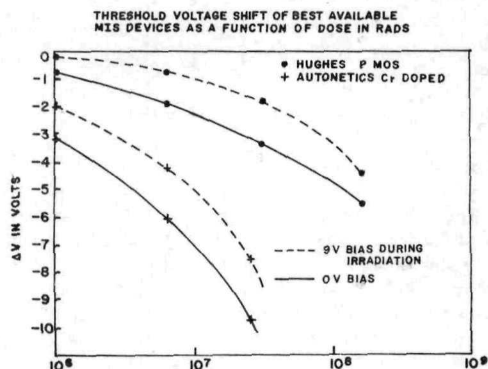

Figure 7

Since the dominant mechanism leading to threshold shifts in MOS devices is the positive charge-trapping sites in the oxide, obvious approaches to harden MIS devices are (1) either attempt to eliminate these traps in the SiO_2 or (2) attempt to find an insulator which is not afflicted by this problem. Considerable research has been devoted to approach (1). By adding various dopants to the oxide, dopants have been found which considerably reduce the threshold shifts for irradiations performed with positive gate voltages, but greatly increases the threshold shifts for irradiations with negative gate voltages. Numerous insulators have been tried to replace the silicon dioxide, which is the oxide (insulator) used in commercial MOS transistors. One such insulator, silicon nitride, showed great promise for some time of solving the problem. The nitride silicon interface was found to be much more resistant to radiation induced threshold shifts. However, offsetting this increased radiation tolerance several disadvantages were found.[11] The most notable of these is threshold shifts (instabilities) in MNS (Metal Nitride Silicon) transistors caused by a high voltage. This, combined with higher values of interface charge, makes it impractical to use a nitride-silicon interface in high field regions such as the gate of an MIS transistor.

Recently Al_2O_3 has been investigated as a replacement for SiO_2 in MIS devices. We have tested two of the RCA Al_2O_3 devices to 10^6 rads cobalt 60 gamma and the threshold voltage shifted less than 2 volts after 10^6 rads. We do not have data for higher levels because the devices developed gate to source shorts.

Results on ionizing radiation tests up to 10^8 rads are shown in Fig. 7 for new experimental radiation hardened MOS devices. The P-MOS (p channel MOS) made by Hughes appears to be the hardest MIS device at 10^8 rads. The scientific reasons for the hardness of these p-MOS devices are not clearly understood.

Even though it is generally believed that neutrons do not have an appreciable effect to the electrical characteristics of MIS devices, the fact that neutrons may have an effect should not be overlooked. Very little meaningful data exists on the radiation effects of low neutron doses on MIS devices and it is virtually non-existant at 10^{16} neutrons/cm^2. One known effect of neutrons on MIS devices is threshold shifts due to neutron induced positive charge in the oxide. This effect is due to the ionizing capability of neutrons, which is approximately 1 rad = 10^{10} neutrons/cm^2. This would give 10^6 rads at 10^{16} neutrons/cm^2, which can be neglected in comparison to the 10^8 rads from gamma for the NERVA requirement. At least two other neutron effects are possible, threshold shifts due to carrier removal and electrical characteristic changes due to neutron induced fast surface states at the interface. The reason why a threshold shift due to carrier removal, which is simply an increase in the substrate resistivity, has not been observed is probably because the substrate resistivity, ρ, of the devices tested has been too high for the effect to be noticeable. Carrier removal will have a significant effect on the threshold voltage only if the threshold voltage is strongly dependent on ρ. Brotherton[14] has determined the curve for threshold voltage V_T as a function of ρ for an n channel MOS. This curve shows that V_T is approximately independent of ρ, if $\rho > 10\ \Omega$-cm. Since the known effect of fast neutrons on the bulk silicon is to increase the resistivity, even very high neutron doses would therefore not be expected to cause a significant threshold shift, if the initial resistivity is greater than 10 Ω-cm. Most n channel devices are made with $\rho > 10\ \Omega$-cm, which explains why threshold shifts due to carrier removal have not been observed in n channel MOS's. If $\rho \ll 10\ \Omega$-cm and carrier removal is the only effect present, a considerable threshold shift should occur for neutron doses $> 10^{15}$ neutrons/cm^2. This fact is illustrated in the following example:

If $\rho = 1$ Ω-cm, then according to Brotherton's curve $V_T \approx 0$. One ohm-cm roughly corresponds to a p-type substrate initial doping concentration of $2 \times 10^{16} = p_o$. The doping concentration p after a neutron dose of Φ neutrons/cm^2 is given by[2]

$$p = p_o \exp\left(- \frac{\Phi}{398\, p_o^{-77}} \right).$$ Therefore, if

$\Phi = 3 \times 10^{15}$ neutrons/cm^2, $p \approx 2 \times 10^{15}$ which roughly corresponds to a resistivity of 10 Ω-cm. According to Brotherton's curve the resistivity change from 1 to 10 Ω-cm would cause V_T to shift roughly from 0 to -4 volts. Similar arguments hold for p channel devices. Fortunately, if a p channel device is affected by carrier removal, the resulting threshold shifts should be in the opposite direction to ionizing induced threshold shifts.

Hardening efforts for MIS devices are then quite different from hardening efforts on bipolar and JFET devices. Whereas, bipolar and JFET hardening has stayed within the standard silicon, silicon dioxide technology, MIS hardening has involved new and different technologies. This imposes a penalty of longer term development to achieve equal reliability confidence. Other penalties which seem to be paid for MIS hardness are lack of threshold voltage control, and for MOS the use of p channel devices only.

Experimental procedure: The neutron irradiations performed to provide the data for this paper were done at the MIT nuclear reactor in the pneumatic tube facility. The temperature in this facility is approximately 42°C. The thermal neutron flux is 2.2×10^{13} n/cm^2 sec, the gamma dose rate is 1.3×10^8 R/hr and the neutron flux above 10 Kev is 1.2×10^{12} n/cm^2 sec.

Cobalt gamma radiations were performed at the AFCRL cobalt cell which delivers 1.5×10^6 Rad/hour. The MOS samples were irradiated with both positive and negative gate biases. The bipolar and junction field effect transistors were irradiated without bias applied.

The transistor electrical characteristics where measured under swept D.C. conditions on a curve tracer and under pulsed D.C. conditions when necessary to avoid annealing by electrical dissipation. The MOS threshold shift data was obtained by measuring capacitance as a function of voltage to determine the threshold voltage for each device. The electrical characterization of the devices was performed both before and after each radiation exposure.

Tentative NERVA Requirement: In a private conversation with representatives of NASA and the Aerojet Corporation, NERVA requirements for a power switch and for multiplexing were given. The radiation requirement for both was a total of 3×10^{16} neutrons/cm^2 and 7×10^7 rads gamma. The power device had a 60 volt breakdown requirement which was firm and a 5 amp current capability. The temperature requirement on the power device was -250°C to 100°C, but was considered to be flexible. The multiplexer switches were to have after irradiation 300 Ω on resistance and 10^8 Ω off resistance, with an isolation resistance of 10^6 ohms. The voltage requirements were not firm, but could be in the vicinity of 5 volts. The switching current was to be in the vicinity of 1 μ amp, with a leakage current less than 100 nano amps.

Conclusions: Theoretical and experimental information indicates that the JFET devices can meet the multiplexer requirements on a reliable reproducible basis. The power device requirements cannot be met by the JFET, however, because of the 60 volt breakdown requirement. A possibility exists that the p MOS device can meet this power device requirement. It must be cautioned, however, that the hard p MOS device is still in the experimental research stage of development and more neutron data at these high levels is needed. Further, the development of a high power device poses many more serious problems than for low power devices like those tested. It appears very doubtful that bipolar transistors can be made hard enough to meet either of these requirements. In the final analysis, however, just what constitutes an acceptable degradation (and therefore the device hardness) is determined by the circuit and systems designer.

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