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TITLE: PLAN FOR TEST CELL "A" NARROW BAND DATA ACQUISITION
ACCURACY TEST.

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1.0 INTRODUCTION

Accuracy tests performed to date on the Test Cell "A" Data Acquisition System have resulted in differing accuracy values.

Meetings have been held (Reference (1) NTO-M-2775, dated March 5, 1965; (2) NTO-M-3976, dated May 5, 1965; (3) WANL-TR-4529 (ISFS-973), dated May 11, 1965) to resolve these inconsistencies and it was agreed:

- a. That a narrow band accuracy test should be performed at the end of the NRX-A3 tests.
- b. That the plan and procedure for this test should be reviewed and agreed upon by all parties concerned.
- c. That the statistical method of selecting channels and analyzing data, and the tests employed should result in an accuracy value for each of the ten possible channel configurations and that these accuracy values will be used by all parties concerned.
- d. That while the tests shall be performed on specific channels typical of NRX-A3 configurations, the results will be used to predict the accuracy of similar narrow-band channels.

2.0 TEST OBJECTIVES

The evaluation tests are designed to determine the following objectives for high and low level channels:

- 2.1 Overall channel accuracy (error band limits).
- 2.2 Channel linearity, drift, noise, zero offset.
- 2.3 Channel frequency response.

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2.4 Channel crosstalk.

2.5 Contribution of data instrument component error to channel (amplifier, etc.) inaccuracy.

2.6 Provide data that would permit component error contribution isolation if large errors are encountered.

3.0 TEST DESCRIPTION AND PLAN

3.1 System Description

The narrow band data acquisition system at Test Cell "A" consists of a high-level and a low-level Pulse Amplitude Modulated-Frequency Modulated (PAM/FM) system. The high-level system accepts input signals in the 0 to 5 volt range. These signals are derived either from high-level transducer outputs or from amplified low-level transducer outputs. Input analog signals are sampled at 40 samples per second by solid-state (EG&G) high-level multiplexers. These input signals are converted, in the multiplexer, to pulses of finite widths whose amplitudes are proportional to the value of the signals themselves. This Pulse Amplitude Modulated (PAM) signal is next converted to a Frequency Modulated (FM) signal by a voltage controlled oscillator (VCO). The resulting PAM/FM signal is then transmitted over approximately two miles of transmission line to the Control Point where it is recorded on magnetic tape.

The low-level system functions the same as the high-level system using appropriate low-level components such as low-level multiplexers. Both 40 sample-per-second solid-state (SEL) and 10 sample-per-second mechanical (Bendix) multiplexers are used in the low-level system. Each signal conditioner contains resistance networks which are used to range or scale the transducer output voltage for input to the rest of the system.

Figures 1A through 10A indicate the 10 basic channel configurations found on NRX-A3 high and low-level measurements. These 10 basic channel configurations are typical and cover most of the NRX-A3 diagnostic measurement possibilities. Figures 1A through 4A are the high-level configurations; Figures 5A through 10A are low-level configurations. The configurations covered are:

- Figure 1A - Thermocouple (Ch/A) Measurement - High-Level,
With Reference Well (EG&G Multiplexer).
- Figure 2A - Thermocouple (W/W) Measurement - High-Level,
Without Reference Well (EG&G Multiplexer).
- Figure 3A - Strain Gage Measurement - High-Level (EG&G Multiplexer).
- Figure 4A - Swept Pot Measurement - High-Level (EG&G Multiplexer).
- Figure 5A - Thermocouple (C/C) Measurement - Low-Level
With Reference Well (Bendix Multiplexer).
- Figure 6A - Temperature (RTT) Measurement - Low-Level
Without Reference Well (Bendix Multiplexer).
- Figure 7A - Strain Gage Measurement - Low-Level (Bendix Multiplexer).
- Figure 8A - Thermocouple (C/C) Measurement - Low-Level
With Reference Well (SEL Multiplexer).
- Figure 9A - Temperature (RTT) Measurement - Low-Level
Without Reference Well (SEL Multiplexer).
- Figure 10A - Strain Gage Measurement - Low Level (SEL Multiplexer).

3.2 Test Description

3.2.1 Data System Calibration

In order to correctly utilize existing data reduction programs, an ordinary system voltage calibration will be performed before and after each phase. Also, before Linearity Run A; and before and after Linearity Run E.

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3.2.2 Frequency Response Tests

A signal generator may be used to activate the amplifier sections of the power supplies permitting AC signals to be applied for the frequency response test, conducted at 0.1, 1.0, 5.0 and 10 cps. The accuracy of the frequency response measurements should be within 0.1 per cent. All test instruments used in this test shall be laboratory calibrated prior (within 2 weeks) to this test.

3.2.3 Crosstalk Tests

Determination of the level of cross talk will be accomplished by setting channels up as follows:

- (1) DC-1 Crosstalk (13 data channels at full scale input while the 27 remaining data channels are also at full scale)
- (2) DC-2 Crosstalk (13 data channels at zero level input while the 27 remaining data channels are at full scale)
- (3) DC-3 Crosstalk (the 40 test channels will have full scale to zero input in 11 steps while all unused multiplexer inputs are at 75% of full scale)
- (4) DC-4 Crosstalk (the 40 test channels will have full scale to zero input in 11 steps while all unused multiplexer inputs are at 200% of full scale)
- (5) AC Crosstalk (13 data channels at zero level input while the 27 remaining data channels are at full scale 1 cps)

The chart which follows indicates the multiplexers and the total number of bits which are involved in this crosstalk test with channels as wired for NRX-A3.

Multiplexer	HL1	HL2	HL4	HL5	LL2	LL5	LL6	LL9	LL10	Total
Data Channel Bits	33	03, 05	31	02	30, 20	16	15, 28	35, 37	10	(13)
Adjacent Channel Bits	34	04	32	03	31, 21	17	16, 29	36, 38	11	(12)

The channels are preselected (see section 8.0) and the programmable power supply system is wired to the mating car plug (at the Test Cell wall) from the ELR. Care should be taken to account for line drop in this cabling.

All NRX-A3 channel hook-ups shall remain intact after completion of the NRX-A3 tests. None of the channels indicated herein will be disconnected; these tests are to be performed on the indicated channels as wired for NRX-A3 (see Table I).

3.2.4 Linearity Tests

The programmable power supply system will be used to insert test signals in ten 10 per cent steps from zero to full scale through a "patch-plug" type arrangement at the test cell plug. A brief description of this EG&G set-up is covered in section 5.0. In providing the 10 per cent steps the power supplies will provide data needed to fulfill the linearity, drift, noise, and zero offset test objectives.

The linearity, frequency response, and crosstalk tests as indicated in section 3.5.1 will constitute a complete test cycle for each of the three phases described in the following sections.

3.2.5 Phase I

Figures 1B through 10B are block diagrams indicating the ten basic channel configurations repeated for four identical channel measurements. The same signal source levels (except for the crosstalk test) will be inserted simultaneously into these four channels. Each of

the two multiplexers will receive inputs from two channels. These forty channels will be sampled at time intervals of 0, 2, 4, 8 and 16 hours (16 hour total). These time intervals will be designated Test Runs A, B, C, D, and E.

3.2.6 Phase II

For the Phase II tests, amplifiers A and B are interchanged in the block diagram of each test setup. For example, in Figure 1B, amplifier A_1 is connected with multiplexer bit H0134 and A_2 is connected to H0124. With the amplifiers interchanged, the same 40 channels will be sampled again, for additional time intervals of 0, 2, 4, 8 and 16 hours. Where amplifiers cannot be interchanged, signal conditioners will be interchanged.

3.2.7 Phase III

For Phase III, the amplifiers are reconnected in their original positions but the multiplexers are interchanged. For example, in Figure 1B, multiplexer A will now be connected with inputs B_1 and B_2 , while multiplexer B is connected with inputs A_1 and A_2 . The same 40 channels (with multiplexers interchanged) are again sampled at the same time intervals as before. This will now provide a total of 120 channels of sampled data taken over a span of 16 hours each. If time permits, another data sample (run F) should be taken after an additional 16 hours; a final data sample (run G) is then taken after another 16-hour period. Specified time intervals for drift tests may be modified in order that normal working schedules can be maintained. However, this modification should remain consistent throughout all phases of the test.

3.3 Components Test

A cross check on the data instrument components in the above manner is an essential part of this test. The common methods of adding the certified accuracies of all the components, or even calculating the square root of the sum of the squares of the accuracies of all the components does not always result in realistic estimates. When a number of

instruments are grouped to perform a single overall function, their individual errors may become combined in such a way that the error of the whole group is largely random. If statistical methods can be used to evaluate the entire system, the contribution of each part can be determined. The system error can then be considered as a statistical combination of the errors of the parts.

3.4 Test Measurements and Setup

Refer to Figure 2B as a typical block diagram. The following voltage and frequency measurements are to be manually recorded as indicated under 3.5.1:

- V_1 - at the test car wall plug
- V_2 - at signal conditioner input
- V_3 - at signal conditioner output
- V_4 - at amplifier output
- F - output frequency of the VCO
- V_{1A} - at power supply output bus. (Note: this bus is the input to the source signal conditioners which is the EG&G system for transducer simulation. This circuit is not shown on the attached block diagrams.)

In addition, the calibration voltage to the VCO's, as well as the frequency shifts associated with this voltage, are to be recorded. All voltage measurements are to be made with digital voltmeters within 0.1 per cent. The frequency measurement is to be made with the Hewlett-Packard frequency counter within 0.1 per cent.

To provide four channels each for Figures 6B and 9B, three simulated temperature channels (identified as T-XXX-1, -2 and -3) were added.

3.5 Test Procedure

3.5.1 Each of the three phases will consist of the following 28 separate runs:

Manual Measurements

(1) Data System Calibration 1	
(2) AC-1 Frequency Response at 0.1 cps	40 V1
(3) AC-2 Frequency Response at 1.0 cps	40 V1
(4) AC-3 Frequency Response at 5.0 cps	40 V1
(5) AC-4 Frequency Response at 10.0 cps	40 V1
(6) AC-5 Crosstalk (13 channels)	52 V1, V2, V3, V4
(7) DC-1 Crosstalk	40 V1
(8) DC-2 Crosstalk	---
(9) DC-3 Crosstalk	---
(10) DC-4 Crosstalk	---
(11) Data System Calibration No. 2	266 V1A, V1, V2, V3, V4
(12) Linearity Run A at 0 hours	66 F
(13) Linearity Run B at 0 + 2 hours	240 V1
(14) Linearity Run C at 0 + 4 hours	---
(15) Linearity Run D at 0 + 8 hours	---
(16) Data System Calibration No. 3	266 V1A, V1, V2, V3, V4; 66 F
(17) Linearity Run E at 0 + 16 hours	---
(18) Data System Calibration No. 4	---
(19) DC-5 Crosstalk	40 V1
(20) DC-6 Crosstalk	---
(21) DC-7 Crosstalk	---
(22) DC-8 Crosstalk	---
(23) AC-6 Frequency Response at 0.1 cps	40 V1
(24) AC-7 Frequency Response at 1.0 cps	40 V1
(25) AC-8 Frequency Response at 5.0 cps	40 V1
(26) AC-9 Frequency Response at 10.0 cps	40 V1
(27) AC-10 Frequency Response at 10.0 cps	52 V1, V2, V3, V4
(28) Data System Calibration No. 5	---

3.5.2 Recording

3.5.2.1 Tape Signals

The programmable power supply system will be stepped off in ten 10 per cent increments for the linearity tests and the PAM/FM channel (multiplexer output signals) will be recorded on magnetic tape at the Control Point. A 10 second data sample will be recorded for all measurements for each step. All measurements will be simultaneously recorded on two tape recorders. Each of the 28 runs indicated on 3.5.1 will be recorded on tape for each phase. The time code generator will be running during the entire test; and a log recorded of the test portion being conducted and the time.

NOTE: Do not operate tape recorder while V_1 signals are being measured, because of loading effects.

3.5.2.2 Digital Signals (Manual Measurements)

The voltage and frequency measurements specified in section 3.4 will be manually recorded for each of the 16 separate runs indicated in section 3.5.1. The specified voltages can be measured with the Electro-Instruments voltmeter in the Transducer Test Equipment if desired.

3.5.3 Quick-Look System

The quick-look system will be checked by comparing all V_3 voltages (signal conditioner outputs for configurations typical of Figure 6B), or all V_4 voltages (amplifier outputs for configurations typical of Figure 1B) with the recordings made on the Sanborns. Admittedly, only gross errors can be determined by this visual procedure.

4.0 STATISTICAL BASIS FOR TEST PLAN

4.1 Since the primary objective of this experiment is to estimate the accuracy of data channels, it would seem that a simple experimental plan involving repeated tests of

several channels would be sufficient. However, the circuitry of these channels varies with the type of input being observed and thus the accuracy of measurements transmitted would not necessarily be independent of the type of channel (channel configuration), nor necessarily independent of the components of the circuit for a particular configuration. Then too, if the accuracy as determined from a simple experiment differs substantially from the expected, an indication as to what configuration or what components may be at fault cannot be easily obtained. Thus, it is necessary to perform tests which help to pinpoint individual component errors, rather than solely system error limits.

4.2 Section 3.0, Test Description and Plan, contains a description of a plan considering ten channel configurations with two multiplexers per configuration and two channels (different amplifiers or signal conditioners) per multiplexer, for a total of 40 channels for Phase I. Phases II and III also consider 40 channels using the same test conditions with an interchange of multiplexers and/or signal conditioners and/or amplifiers occurring between each phase. In each phase the parameters of interest are to be measured at 0, 2, 4, 8 and 16 hours with the possibility of two additional sets of measurements after an additional 16 and 32 hours in Phase III.

4.3 Following the plan as described in section 3.0, a total of 200 measurements for each parameter in each phase will be obtained. These data will be analyzed using the Analysis of Variance technique and should yield a valid estimate of the accuracy of a data channel. Furthermore, by combining data from Phase I and Phase II, an estimate of the effect of amplifiers and/or signal conditioners on the accuracy estimate will be derived; by combining the data from Phase I and Phase III, an estimate of the effect of multiplexers on the accuracy estimate will be obtained; and finally, by combining the data of Phase II and Phase III, estimates of possible interaction effects will be evaluated. Additional analyses using the Analysis of Variance technique will be made to derive correlations between the parameters of interest, primarily to determine weighing factors (if these exist) for combining variance (accuracy) estimates from all parameters. The Plan described in section 3.0 was established to yield valid

estimates associated with the overall accuracy of data channels. It was established with the Analysis of Variance technique considered as the statistical tool to be used to obtain these valid estimates. The tests were established to obtain maximum information (configuration, multiplexer, amplifier, signal conditioner, time, and their interaction effects) for a minimum experimental effort.

4.4 Test data taken in the program described are to be analyzed using analysis of variance techniques, as described in the following references 1 and 3. The additional references describe techniques of lesser importance which will be utilized as needed.

1. Chew, V.
Experimental Designs in Industry
John Wiley and Sons, New York City
2. Cochran, W. G., and Cox, G. M.
Experimental Designs
John Wiley and Sons, New York City
3. Davies, O. L.
Design and Analysis of Industrial Experiments
Hafner Publishing Company, New York City
4. Fisher, R. A.
Design of Experiments
Hafner Publishing Company, New York City
5. Kempthorne, O.
Design and Analysis of Experiments
John Wiley and Sons, New York City

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4.5 Source of Analysis Data

The analysis will be done from the digital (N_3) tapes and separate values will be reported for the CAL COMP plotter and non-linear calibrations. A comparative analysis will be made (for the same channels) between the CAL COMP PLOTS of this test and those from the calibrations on NRX-A3.

4.5.1 Use of NRX-A3 Data in Verification of Derived Values

A comparison of the ambient run data from NRX-A3 will be made of the channels under test in the accuracy test plan in order to establish the transducer contribution to the inaccuracy. Such transducer contribution should be helpful, especially in the determination of noise.

4.5.1.1 The end-to-end stimulus test from NRX-A3 data will also be considered as a possible addition to the analysis data. (It should be noted that the mechanical commutators were not running at this time, and some reduction of noise will be observed because of this.)

4.5.1.2 NRX-A3 data from the test channels specified in the test plan will be analyzed and compared with the results of the accuracy test. Check values for linearity and long term drift (approximately 13 hours) can be evaluated from the pre- and post-voltage calibrations of NRX-A3. Also, a quasi-crosstalk measurement (considering the multiplexer component only, and disregarding cable and connector contributions) from the signal conditioners to the recorders can be obtained from these NRX-A3 calibrations, and used to check crosstalk figures obtained by the analysis technique.

4.6 Reports

The final analysis report will include samples of CAL Comp plots, Sanborn charts, and a description of the data reduction and analysis techniques used in determining the accuracy values. If possible, the analysis report will indicate the separate inaccuracy contributions for the transducer, the data acquisition and the data reduction systems.

5.0 SIMULATION OF TRANSDUCER OUTPUTS

The programmable power supplies will remain in and be used from the ELR, thus keeping the ambient temperature of the power supplies well controlled. These supplies (in conjunction with 40 source signal conditioners) will be used with the channel signal conditioners as follows:

5.1 EG&G will hook up the power supplies and source signal conditioners to provide the correct signal levels and simulated transducer impedances, route a cable from the ELR to the test pad, and connect the cable to the test car plug. These signals will permit the accomplishment of the linearity test (section 3.2.4) objective of section 2.2.

5.2 Channel crosstalk (section 3.2.3) will be accomplished by routing signals from a separate power supply to the test car plug in order to supply the required two signals.

5.3 EG&G will provide a function generator and read out equipment required to accomplish the frequency response test (section 3.2.4) objectives.

6.0 DATA REDUCTION AND PRESENTATION METHOD

6.1 Data Reduction

The PAM/FM data recorded on magnetic tape for this test will be decommutated, digitized by the CDC160-A computer, reduced to engineering units by an IBM-704 computer, formatted for plotting by the CD160-A computer and plotted as time versus function (voltage) curves by California Computer Corporation (CAL COMP) plotters.

A portion of the data will be reduced twice. This will be done for the purpose of checking any errors resulting from the making of tape copies.

6.2 Figure 11 shows a flow chart of the data flow through the data reduction system. The operations shown are:

1. Digitization: Under control of input cards (I) and manual switches data (A) is digitized over specific time intervals and at specific sampling rates.
2. Reduction: The data on the N2 tape (B) is reduced to engineering units via a calibration (C) in the form of straight line segments approximating the transducer calibration curve to within 0.1 per cent. Data is reduced from channels as specified on the patch panel tape (D) over time intervals as specified by the input cards (J). All data will be reduced linearly for direct comparison with the manually recorded data. In addition, all linear data for Phase I will be processed to generate CAL COMP plots similar to NRX-A3 calibration data. These CAL COMP plots will include both voltage calibrations and transducer conversion data associated with particular channels. (NOTE: Transducer conversion is defined as the reduction process of converting the transducer calibration to engineering units. Since Phase I of this test is wired as it was during NRX-A3, CAL COMP plots for Phase II and III will not include the transducer conversion.) To evaluate the accuracy of the CAL COMP plots in general, and not those associated with transducer conversion inaccuracies, CAL COMP plots of all the linearly reduced data will be made.
3. Formatting: The data in engineering units contained on the N3 tape (E) is formatted for the plotters and written on the N4 tape (G).
4. Plotting: Plots (H) are prepared under control of the CDC160-A computer.

7.0 CHANGES TO SYSTEM CONFIGURATION - NEW EQUIPMENT

When new components are substituted in the data system, it is not necessary to perform the entire system check again. The following procedure shall be observed.

7.1 Bench test values for linearity, crosstalk, drift, frequency response and noise for any new component shall be used to calculate a new expected channel accuracy value based on one of the correct channel configurations.

7.2 An end-to-end channel check shall then be performed to confirm the predicted channel accuracy. This is done by applying known voltages at the test car plug and noting the frequency shift at the output of the VCO. Also, the output shall be recorded on the N3 tape, and this N3 tape compared with the N3 tape made with previous (NRX-A3) equipment.

7.3 If this new accuracy value is not within ± 0.5 per cent of the predicted channel configuration accuracy value, then a complete Phase II or Phase III (depending upon the type of component) test shall be performed as described in section 3.2.5 or 3.2.6 to determine the reasons for the lack of estimated accuracy.

8.0 DETAILS OF CHANNEL SET-UP AIDS

8.1 Table I shows the channels which will be used during the accuracy tests. The column headings are defined as follows:

<u>Column</u>	<u>Description</u>
1	System measurement types, as given previously (Figure 1B through Figure 10B).
2	Channels for which signals will be simulated.
3	Transducer type being simulated.
4	Full scale signal for that channel.
5	Band width of this type of measurement.
6	Multiplexer and bit position for that multiplexer for the channel indicated.
7	Multiplexer type.
8	Zero calibration offset signal required.

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8.2 Table II describes the signal insertion points for each channel measurement at the master plug. (Note: Signals for Figure 4B will be inserted at the most convenient terminal boards located in the ELR, FCR, or RER.)

9.0 DATA ANALYSIS AND COMPUTATION METHOD

9.1 Linearity

Linearity is determined by defining a function such that $V_i = f[V_i^1]$

where: V_i = the computer calculated output voltage

V_i^1 = the input voltage as recorded at the TCA

i = 1 to 11 voltage calibration steps

Therefore linearity is defined as the maximum of the absolute difference $[V_i^1 - \bar{V}_i]$, where $\bar{V}_i$ is the measured output voltage as read from the N3 tape.

This, linearity for the entire system includes the data reduction system linearity correction capability as well as the data system contribution. The maximum deviation on any single step of the eleven step calibration signal then becomes the defining system linearity.

9.2 Drift

9.2.1 Full Scale Drift (Gain Stability)

For a full scale input voltage applied at several distinctly separate times, some variation in N3 indicated voltages can be expected. This variation represents (primarily) full scale drift (or gain stability) in the channel.

9.2.2 Zero Offset Drift

In a similar manner to full scale drift, zero offset drift is represented by the variation of the digitized values representing zero input signals taken at separate times.

9.2.3 Determination of Drift

Full scale drift and zero offset drift as described in paragraphs 9.2.1 and 9.2.2 should be combined into one overall drift figure by comparing the linearity curves taken at several distinctly separate time intervals. Then the overall channel drift is defined as the maximum deviation between these curves over the zero to full scale span. This deviation should be expressed as a percent of full scale per hour.

9.3 Noise

Noise will be determined by using the N3 peak-to-peak values. From these values, the standard deviation for the eleven steps, (each being a 10 second data sample period) will be determined. Noise will be expressed as a percentage of the full scale input.

For each step, the maximum difference of the peak-to-peak values will be determined and compared with the standard deviation to ascertain the presence of spurious signals.

9.4 Crosstalk

Crosstalk will be defined as the maximum coupling (expressed as a percentage of full scale signal on the test channel) observed in any of the tests described in section 3.2.3.

9.5 Channel Accuracy

The accuracy of some systems have commonly been computed by taking the variances of the data runs for each parameter (linearity, drift, noise, etc.), then adding the sum of the square of the variances and extracting the square root. This method may be realistic if the parameters are independent.

For this accuracy tests, the subsequent analysis of the data may indicate that some of the parameters under test are not independent. Therefore, weighing factors will be

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developed from the analyses, and will be appropriately assigned for computing the channel accuracy. An equation cannot be given at this time, except to state that it will generally follow the form of the root mean square formula.

NOTE: The writer acknowledges the contribution of all who have participated in the preparation and review of this test plan, especially Mr. W. Horton (WANL, Reliability) for preparing section 4.0 "Statistical Basis for Test Plan," and Mr. M. Vuckovich (WANL, Instrumentation Systems and Facilities Support) for technical contributions.

FIG. 1.A THERMOCOUPLE MEASUREMENT THROUGH HIGH LEVEL SYSTEM/USING REFERENCE WELL. (EG&G MULTIPLEXER)

605352A

*ONLY USED WITH EG & G MULTIPLEXERS

605353A

FIG. 2.A THERMOCOUPLE MEASUREMENT THROUGH HIGH LEVEL SYSTEM WITHOUT A REFERENCE WELL. (EG&G MULTIPLEXER)

605354A

FIG. 3.A STRAIN GAGE MEASUREMENT THROUGH HIGH LEVEL SYSTEM, (EG&G MULTIPLEXER)

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FIG. 4.A SWEEP POT MEASUREMENT THROUGH HIGH LEVEL SYSTEM. (EG&G MULTIPLEXER)

FIG. 5.A THERMOCOUPLE MEASUREMENT THROUGH LOW LEVEL SYSTEM USING REFERENCE WELL. (BENDIX MULTIPLEXER)

605356A

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FIG. 6.A TEMPERATURE MEASUREMENT THROUGH LOW LEVEL SYSTEM WITHOUT REFERENCE WELL (BENDIX MULTIPLEXER)

605357A

WANT-TME-1161

FIG. 7.A STRAIN GAGE MEASUREMENT THROUGH LOW LEVEL SYSTEM. (BENDIX MULTIPLEXER)

605358A

WALT-TME-1161

FIG. 8.A TEMPERATURE MEASUREMENT THROUGH LOW LEVEL SYSTEM USING REFERENCE WELL. (SEL MULTIPLEXER)

605359A

FIG. 9.A TEMPERATURE MEASUREMENT THROUGH LOW LEVEL SYSTEM WITHOUT REFERENCE WELL. (SEL MULTIPLEXER)

605378A

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605379A

FIG. 10.A STRAIN GAGE MEASUREMENT THROUGH LOW LEVEL SYSTEM (SEL MULTIPLEXER)

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FIGURE 1B - (CH/A) T/C MEASURE THROUGH HIGH LEVEL SYSTEM WITH
REFERENCE JUNCTION (EG&G MULTIPLEXER)

FIGURE 2B - (W/W) T/C MEASUREMENT THROUGH HIGH LEVEL SYSTEM
WITHOUT A REFERENCE WELL (EG&G MULTIPLEXER)

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FIGURE 3B - STRAIN GAGE MEASUREMENT THROUGH HIGH LEVEL SYSTEM (EG&G MULTIPLEXER)

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FIGURE 4B - SWEPT POT MEASUREMENT THROUGH HIGH LEVEL SYSTEM (EG&G MULTIPLEXER)

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FIGURE 5B - (C/C) T/C MEASUREMENT THROUGH LOW LEVEL SYSTEM WITH REFERENCE JUNCTION
(T/C MULTIPLEXER.)

FIGURE 6B - (RTT) TEMPERATURE MEASUREMENT THROUGH LOW LEVEL SYSTEM WITHOUT REFERENCE JUNCTION (BENDIX MULTIPLEXER)

FIGURE 7B - STRAIN GAGE MEASUREMENT THROUGH LOW LEVEL SYSTEM (BENDIX MULTIPLEXER)

FIGURE 8B - (C/C) T/C MEASUREMENT THROUGH LOW LEVEL SYSTEM WITH
REFERENCE JUNCTION (SEL MULTIPLEXER)

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FIGURE 9B - (RTT) TEMPERATURE MEASUREMENT THROUGH LOW LEVEL SYSTEM WITHOUT REFERENCE JUNCTION (SEL MULTIPLEXER)

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FIGURE 10B - STRAIN GAGE (PRESSURE) MEASUREMENT THROUGH LOW LEVEL SYSTEM (SEL MULTIPLEXER)

FIGURE 11 DATA FLOW THROUGH DATA REDUCTION SYSTEM

TABLE I

<u>Fig.</u>	<u>Channel</u>	<u>Descrip.</u>	<u>F.S.</u>	<u>B/W</u>	<u>Mplx.</u>	<u>Type</u>	<u>Z Cal.</u>
1.B	T-603-3A	C/A	40 mv	5	H0203	EG&G	+5.714
	T-607-3A	C/A	40 mv	5	H0205	EG&G	+5.714
	T-613-3A	C/A	40 mv	5	H0124	EG&G	+5.714
	T-763-3A	C/A	40 mv	5	H0134	EG&G	+5.714
2.B	T-601-3A	W/W	40 mv	5	H0122	EG&G	0
	T-663-3A	W/W	40 mv	5	H0133	EG&G	0
	T-602-3A	W/W	40 mv	5	H0222	EG&G	0
	T-139-3A	W/W	40 mv	5	H0213	EG&G	0
3.B	P-124-3A	SG PS	20 mv	5	H0103	EG&G	0
	PD-401-3A	SG PS	20 mv	5	H0110	EG&G	0
	P-210-3A	SG PS	20 mv	5	H0204	EG&G	0
	PD-203-3A	SG PS	20 mv	5	H0209	EG&G	0
4.B	DP-XXX-1	Pot.	10 v	5	H0431	EG&G	0
	DP-049B-K	Pot.	10 v	5	H0432	EG&G	0
	DJ-011-G	Pot.	10 v	5	H0502	EG&G	0
	DJ-XXX-2	Pot.	10 v	5	H0503	EG&G	0
5.B	T-245-3A	C/C	10 mv	1	L0316	Ben.	+6.155
	T-433-3A	C/C	10 mv	1	L0320	Ben.	+6.125
	T-246-3A	C/C	10 mv	1	L0416	Ben.	+6.155
	T-434-3A	C/C	10 mv	1	L0420	Ben.	+6.125
6.B	T-856-3A	RTT	40 mv	1	L0528	Ben.	-55.253
	T-866-3A	RTT	40 mv	1	L0530	Ben.	-39.173
	T-860-3A	RTT	40 mv	1	L0628	Ben.	-76.708
	T-XXX-1	RTT	40 mv	1	L0629	Ben.	-55.253
7.B	M-254-3A	SG	40 mv	1	L0516	Ben.	+20.00
	M-256-3A	SG	40 mv	1	L0517	Ben.	+20.00
	M-253-3A	SG	40 mv	1	L0615	Ben.	+20.00
	M-255-3A	SG	40 mv	1	L0616	Ben.	+20.00
8.B	T-216-3A	C/C	10 mv	5	L0936	SEL	+6.155
	T-226-3A	C/C	10 mv	5	L0937	SEL	+6.155
	T-360-3A	C/C	10 mv	5	L1010	SEL	+6.066
	T-361-3A	C/C	10 mv	5	L1011	SEL	+6.066

TABLE I (Cont'd)

<u>Fig.</u>	<u>Channel</u>	<u>Descrip.</u>	<u>F.S.</u>	<u>B/W</u>	<u>Mplx.</u>	<u>Type</u>	<u>Z Cal.</u>
9.B	T-854-3A	RTT	100 mv	5	L0230	SEL	-51.147
	T-864-3A	RTT	100 mv	5	L0231	SEL	-51.147
	T-XXX-2	RTT	100 mv	5	L0935	SEL	-51.147
	T-XXX-3	RTT	100 mv	5	L0938	SEL	-51.147
10.B	P-406-3A	SG PS	20 mv	5	L0220	SEL	0
	P-500-3A	SG PS	20 mv	5	L0221	SEL	0
	P-305-3A	SG PS	20 mv	5	L1019	SEL	0
	P-308-3A	SG PS	40(20)mv	5	L1030	SEL	0

TABLE II

<u>Fig.</u>	<u>Channel</u>	<u>Type</u>	<u>Wire Code</u>	<u>Master Plug</u>	<u>Mplx.</u>
1.B	T-603-3A	CH/A	CH	J15-88	H0203
			AL	J15-89	
			SH	J15-90	
	T-607-3A	CH/A	CH	J15-98	H0205
			AL	J15-97	
			SH	J15-96	
	T-613-3A	CH/A	CH	J17-1	H0124
			AL	J17-2	
			SH	J17-3	
	T-763-3A	CH/A	CH	J17-19	H0134
			AL	J17-20	
			SH	J17-21	
2.B	T-601-3A	W/W	BLK	J9-1	H0122
			WHT	J9-2	
			SH	J9-3	
	T-663-3A	W/W	BLK	J11-82	H0130
			WHT	J11-81	
			SH	J11-80	
	T-602-3A	W/W	BLK	J9-4	H0222
			WHT	J9-5	
			SH	J9-6	
	T-139-3A	W/W	BLK	J-28-91	H0213
			WHT	J-28-92	
			SH		
3.B	P-124-3A	SG PS	BLK-7	J22-19	H0103
			WHT	J22-20	
			BLK-8	J22-22	
			WHT	J22-23	
			SH	J22-33	
	PD-401-3A	SG PS	BLK-24	J30-70	H0110
			WHT	J30-71	
			BLK-25	J30-73	
			WHT	J30-74	
			SH	J30-75	

TABLE II (Cont'd)

<u>Fig.</u>	<u>Channel</u>	<u>Type</u>	<u>Wire Code</u>	<u>Master Plug</u>	<u>Mplx.</u>
3. B (Cont'd)	P-210-3A	SG PS	BLK-9	J23-32	H0204
			WHT	J23-31	
			BLK-10	J23-29	
			WHT	J23-28	
			SH	J23-27	
	PD-203-3A	SG PS	BLK-5	J23-8	H0209
			WHT	J23-7	
			BLK-6	J23-16	
			WHT	J23-17	
			SH	J23-18	
4. B	DP-XXX-1	Pot.		J-14-70	H0431
				J-14-71	
	DP-049B-K	Pot.		J-14-76	H0432
				J-14-77	
	DJ-011-G	Pot.		J-14-82	H0502
				J-14-81	
	DJ-XXX-2	Pot.		J-14-88	H0503
				J-14-89	
5. B	T-245-3A	C/C	CU BLK-19	J28-55	L0316
			CN WHT	J28-56	
			SH	J28-57	
	T-433-3A	C/C	CU BLU-4	J16-11	L0320
			CN RED	J16-10	
			SH	J16-9	
	T-246-3A	C/C	CU BLK-20	J28-58	L0416
			CN WHT	J28-67	
			SH	J28-66

TABLE II (Cont'd)

<u>Fig.</u>	<u>Channel</u>	<u>Type</u>	<u>Wire Code</u>	<u>Master Plug</u>	<u>Mplx.</u>
5.B (Cont'd)	T-434-3A	C/C	CU BLU-5 CN RED SH	J16-8 J16-7 J16-15	L0420
6.A	T-856-3A	RTT	BLK-24 WHT BLK-25 WHT SH	J29-70 J29-71 J29-73 J29-74 J29-75	L0528
	T-866-3A	RTT	BLK-17 WHT BLK-18 WHT SH	J30-44 J30-43 J30-52 J30-53 J30-54	L0530
	T-860-3A	RTT	BLK-28 WHT BLK-29 WHT SH	J29-82 J29-81 J29-79 J29-78 J29-87	L0628
	T-XXX-1	RTT	BLK WHT	J24-22 J24-23	L0629
7.B	M-254-3A	SG	BLK-1 WHT BLK-2 WHT SH	J30-1 J30-2 J30-4 J30-5 J30-6	L0615
	M-256-3A	SG	BLK-5 WHT BLK-6 WHT SH	J30-8 J30-7 J30-16 J30-17 J30-18	L0517

TABLE II (Cont'd)

<u>Fig.</u>	<u>Channel</u>	<u>Type</u>	<u>Wire Code</u>	<u>Master Plug</u>	<u>Mplx.</u>
7.B (Cont'd)	M-253-3A	SG	BLK-32	J23-94	L0615
			WHT	J23-100	
			BLK-33	J23-98	
			WHT	J23-97	
			SH	J23-96	
	M-255-3A	SG	BLK-3	J30-14	L0616
			WHT	J30-13	
			BLK-4	J30-11	
			WHT	J30-10	
			SH	J30-9	
8.B	T-216-3A	C/C	CU BLK-12	J27-34	L0936
			CN WHT	J27-35	
			SH	J27-36	
	T-226-3A	C/C	CU BLK-14	J27-40	L0937
			CN WHT	J27-41	
			SH	J27-42	
	T-260-3A	C/C	CU BLU-13	J8-37	L1010
			CN RED	J8-38	
			SH	J8-39	
	T-361-3A	C/C	CU BLU-14	J8-40	L1011
			CN RED	J8-41	
			SH	J8-42	
9.B	T-854-3A	RTT	BLK-22	J29-62	L0230
			WHT	J29-61	
			BLK-23	J29-59	
			WHT	J29-68	
			SH	J29-69	
	T-864-3A	RTT	BLK-32	J29-94	L0231
			WHT	J29-100	
			BLK-33	J29-98	
			WHT	J29-97	
			SH	J29-96	

TABLE II (Cont'd)

<u>Fig.</u>	<u>Channel</u>	<u>Type</u>	<u>Wire Code</u>	<u>Master Plug</u>	<u>Mplx.</u>
9.B (Cont'd)	T-XXX-2	RTT	BLK-17	J29-44	L0935
			WHT	J29-43	
			BLK-18	J29-52	
			WHT	J29-53	
			SH	J29-54	
	T-XXX-3	RTT	BLK-19	J29-55	L0938
			WHT	J29-56	
			BLK-20	J29-58	
			WHT	J29-67	
			SH	J29-66	
10.B	P-406-3A	SG PS	BLK-10	J14-29	L0220
			WHT	J14-28	
			BLK-11	J14-26	
			WHT	J14-25	
			SH	J14-24	
	P-500-3A	SG PS	BLK-16	J14-47	L0221
			WHT	J14-46	
			BLK-17	J14-44	
			WHT	J14-43	
			SH	J14-51	
	P-305-3A	SG PS	BLK-6	J14-16	L1019
			WHT	J14-17	
			BLK-7	J14-19	
			WHT	J14-20	
			SH	J14-21	
	P-308-3A	SG PS	BLK-8	J14-22	L1030
			WHT	J14-23	
			BLK-9	J14-32	
			WHT	J14-31	
			SH	J14-30