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# THE ET-12 LINEAR CLAD THICKNESS TESTER

by
T.J. Davis

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# THE ET-12 LINEAR CLAD THICKNESS TESTER

T. J. Davis

February 1970

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SUMMARY:

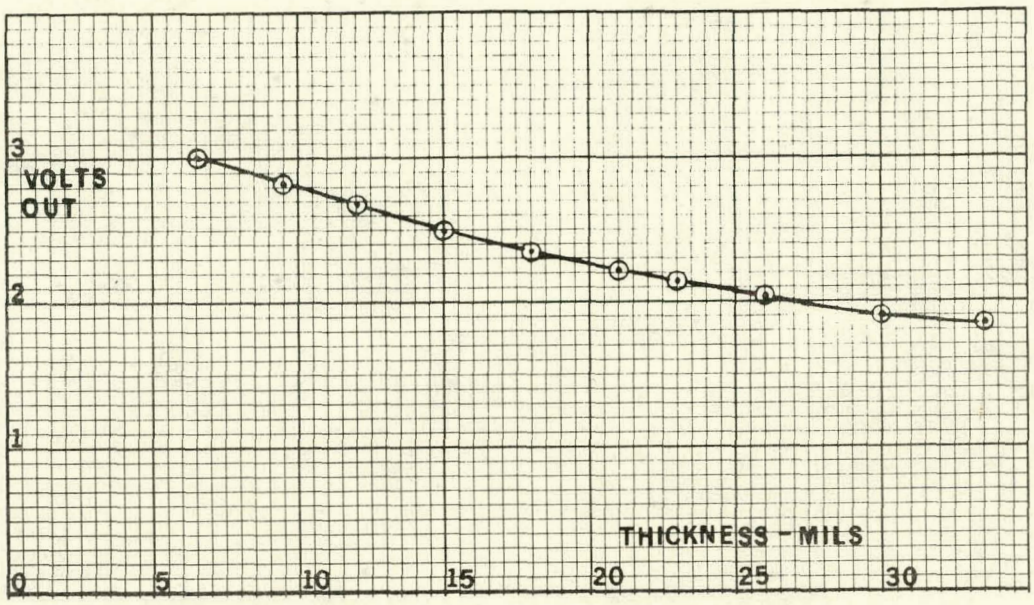
The ET-12 is a solid state eddy current tester designed specifically for nondestructively measuring the clad thickness of N-Reactor fuels. The tester incorporates a linearizing circuit to correct for the inherently nonlinear eddy current response to thickness of zircaloy-2 cladding over uranium. It replaces the UE-2B testers which have been used since initial startup of the reactor.

The ET-12 represents a vastly simplified model in comparison with the UE-2B. Its design requires no transformers, no inductive filtering, and employs a large array of integrated circuits, including audio powers amplifiers and internally compensated op amps.

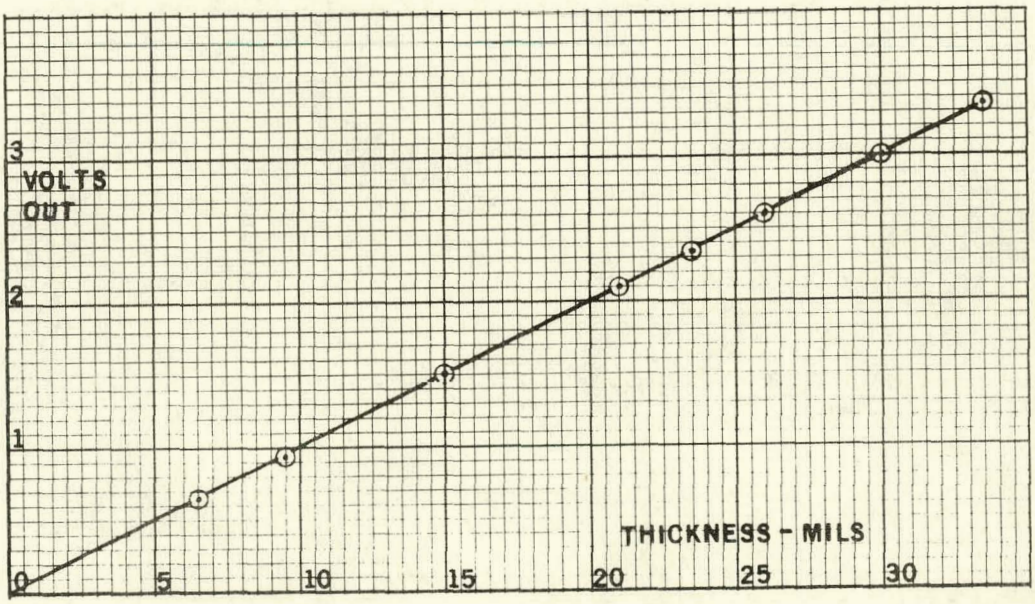
INTRODUCTION:

The original N-Fuels clad thickness testers (UE-2B) have been used solely with initial balance in air to produce the clad thickness response curve shown in Figure 1-a. The inherent nonlinearity of this curve was not highly detrimental until the advent of the MK IV thin clad fuels. It may be seen from examination of Figure 1-a that extension of the UE-2B test range into lower thickness yields an overall response curve of questionable linearity. Additionally, the UE-2B response curve is of an inverted nature with increasing output for decreasing thickness.

Figure 1-b shows the ET-12 tester response for initial balance on uranium. Note that the response is both linear and that zero output corresponds to zero thickness. Also note that the uranium balance produces a three fold increase in sensitivity (volts per mil) over the original test mode.




a) UE-2B (original testers)




b) ET-12 (new tester)

Figure 1. Response curves of UE-2B and ET-12 testers

For these reasons, NDT Systems Engineering, BNW, was directed by Douglas United Nuclear, Inc. to initiate the replacement of the original testers with a new design to remedy the above mentioned problems. The result of this project was development of the ET-12 linear clad thickness tester.

The ET-12 is a solid state, temperature compensated tester which contains a complete test channel on one chassis. It is equipped with selection of two operating modes, direct and linear. The direct mode essentially duplicates the output characteristic of the UE-2B. With initial balance on uranium in the linear mode, the output response of Figure 1-b is attained. Output drift of the ET-12 has been measured in the laboratory to less than 0.125 mils of cladding per hour.

## TEST TECHNIQUE

A wide variety of solutions to the original nonlinear response problem were evaluated before selecting a design for the ET-12. Among these were single coil probes and phase detection eddy current schemes, none of which were successful. No commercial instruments were found to have specifications suitable for this application.

Optimal measurement of clad thickness on another metal with eddy currents dictates a ratio of the two metals' conductivities of at least 10. Clad thickness measurement for N fuel elements is complicated by the fact that the conductivity ratio for zircaloy-2 and uranium is only 2.4

Under these conditions, the original UE-2B eddy current configuration, dual coil probe with amplitude detection at 20KHz, is the most

sensitive that may be attained. The ET-12 tester employs this mode of operation, with the incorporation of analog linearizing circuitry for straightening the response curve.

## FUNCTIONAL DESCRIPTION

Photographs of the ET-12 tester are included as Figures 2 and 3. Figure 2 illustrates the tester's front panel. Chassis component layout is shown in Figure 3.

The front panel contains the usual gain and balance controls and probe connectors. An easy-view panel meter displays the tester's output. For linear mode operation, this meter is calibrated in mils of zircaloy-2.

On top of the chassis are located the four PC boards and a power supply. Note that the driver coil amplifier board supports a heat sink to dissipate power from the IC audio amplifier.

At the rear of the chassis are located BNC output jacks for monitor scope, recorder and oscillator voltages.

## SET-UP AND CALIBRATION

Before beginning any calibration, connect the probe to the instrument, turn on the power, and allow the probe temperature to stabilize in the test tank for approximately 1 minute.

I Direct Mode.

A. Via observation of the balance voltage on the monitor oscilloscope, balance the tester to a null using the front panel X and R adjustments and chasis mounted phase shift switches.

To duplicate the operation of the original testers, this balance is performed with the probe free of any fuel piece.

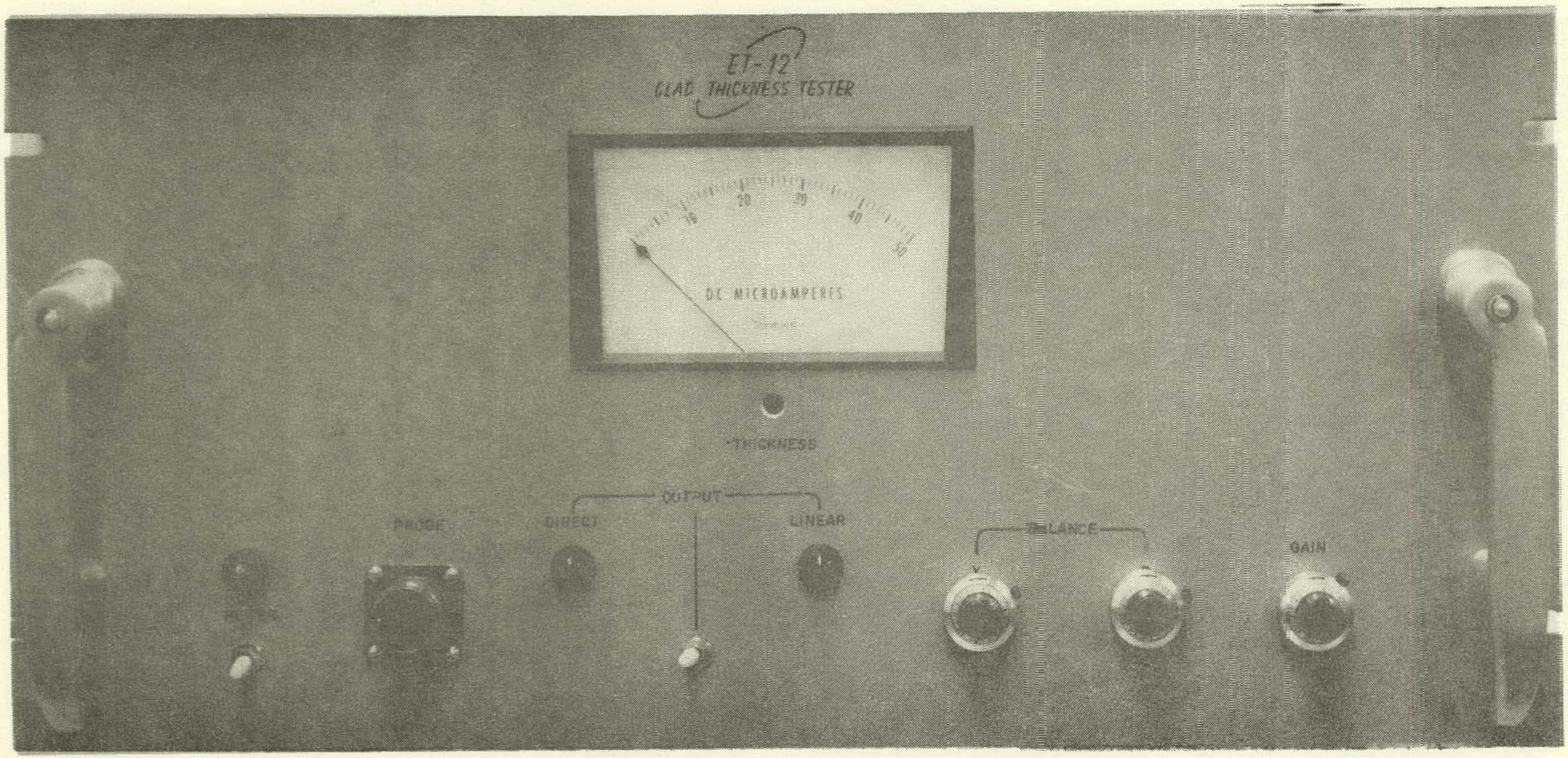



Figure 2. ET-12 front panel

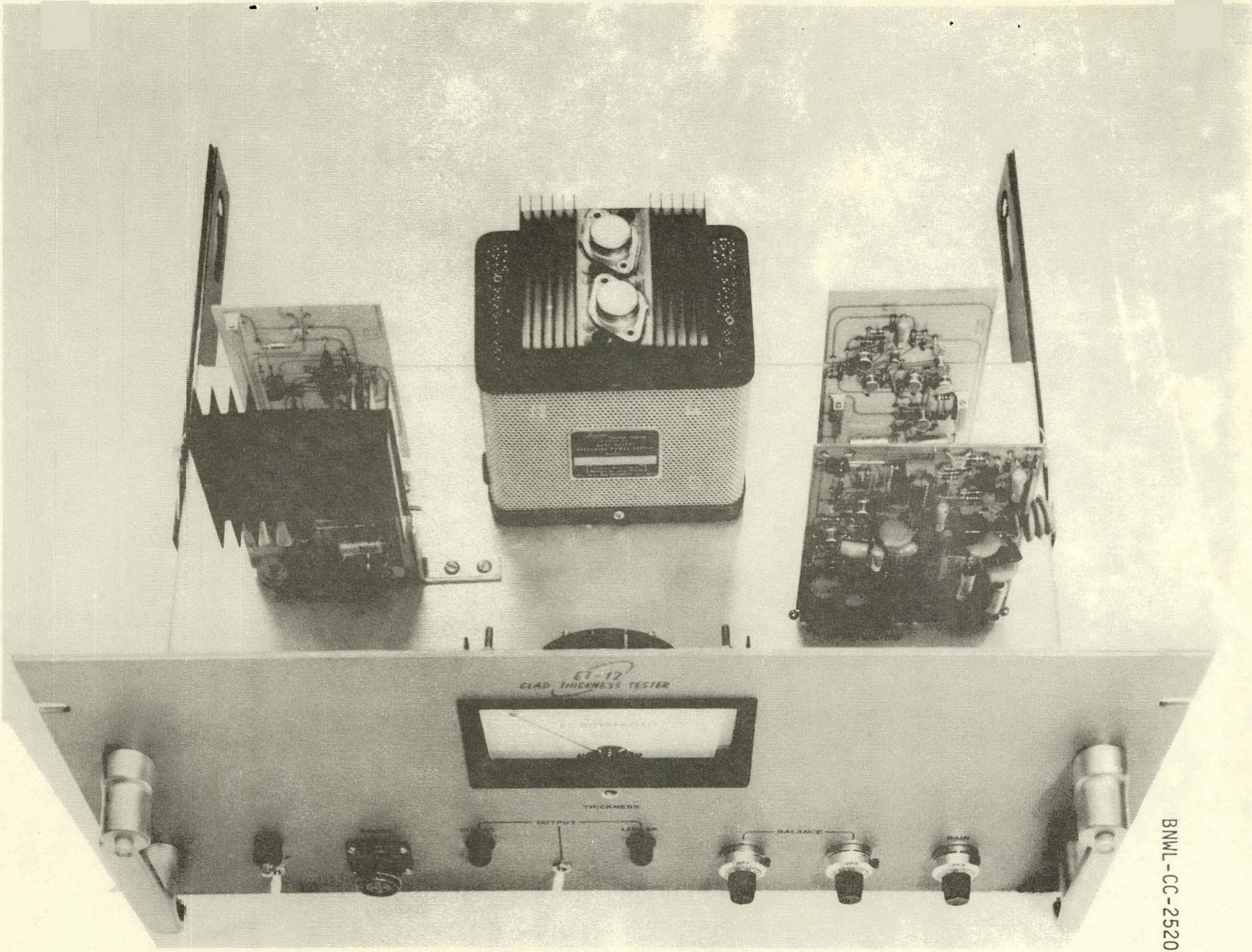



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Figure 3. ET-12 Chassis Component Layout

B. Adjust the front panel gain as required to produce conformance of the tester's output with the master recorder trace of the fuel piece used for standardization.

II LINEAR MODE.

A. Lower the probe onto a piece of bare uranium. Via observation of balance voltage on the monitor oscilloscope, balance the tester to a null using the front panel X and R adjustments and chassis mounted phase shift switches.

B. Place the probe on a stationary fuel standard in a location where the clad thickness is known to be 15 mils. Now adjust the front panel gain to produce a reading of 15 on the panel meter. Verify this reading for both direct and linear modes.

Verify the probe alignment tolerance by twice raising and lowering the probe back on to the standard. If the same thickness reading is not obtained each time, probe wobble adjustment is required.

C. Place the probe on a stationary fuel standard at a point where the thickness is known to be 30 mils. Verify conformance of of the tester's meter output to the curves of Figure 4. (25 on direct, 30 on linear).

D. With the output selector switch in the linear position, the tester is ready for production testing.

SPECIAL CONSIDERATIONS

1. The output meter on the tester's front panel is not intended for facilitating balance adjustments. The slow response time of this meter allows one to adjust a balance control completely through null before its null itself is registered on the meter. The monitor scope should be employed for balancing.

2. When performing initial balance, it is helpful to decrease tester gain so that the output to the monitor scope is not being clipped in the tester circuitry. A clipped waveform on the scope heavily masks the indications of approaching a null.

3. The operation of two chassis in the same console with individual oscillators may result in beat frequency interference. Refer to oscillator section, Appendix I, for instructions on synchronous operation.

4. To initially calibrate a linearizer board for proper curvefitting, refer to instructions in Appendix I. (Page I-11)

LINEAR OUTPUT MODE

Introduction

Analog circuitry on the ET-12 linearizer board subjects the input DC signal to an antilog operator to straighten the overall response curve.

The curves of Figure 4 display the circuitry's computational properties. It may be shown that for a gain setting which produces 1 volt for 10 mils thickness after initial balance on bare uranium, the nonlinear output curve (direct mode) may be expressed by the following function:

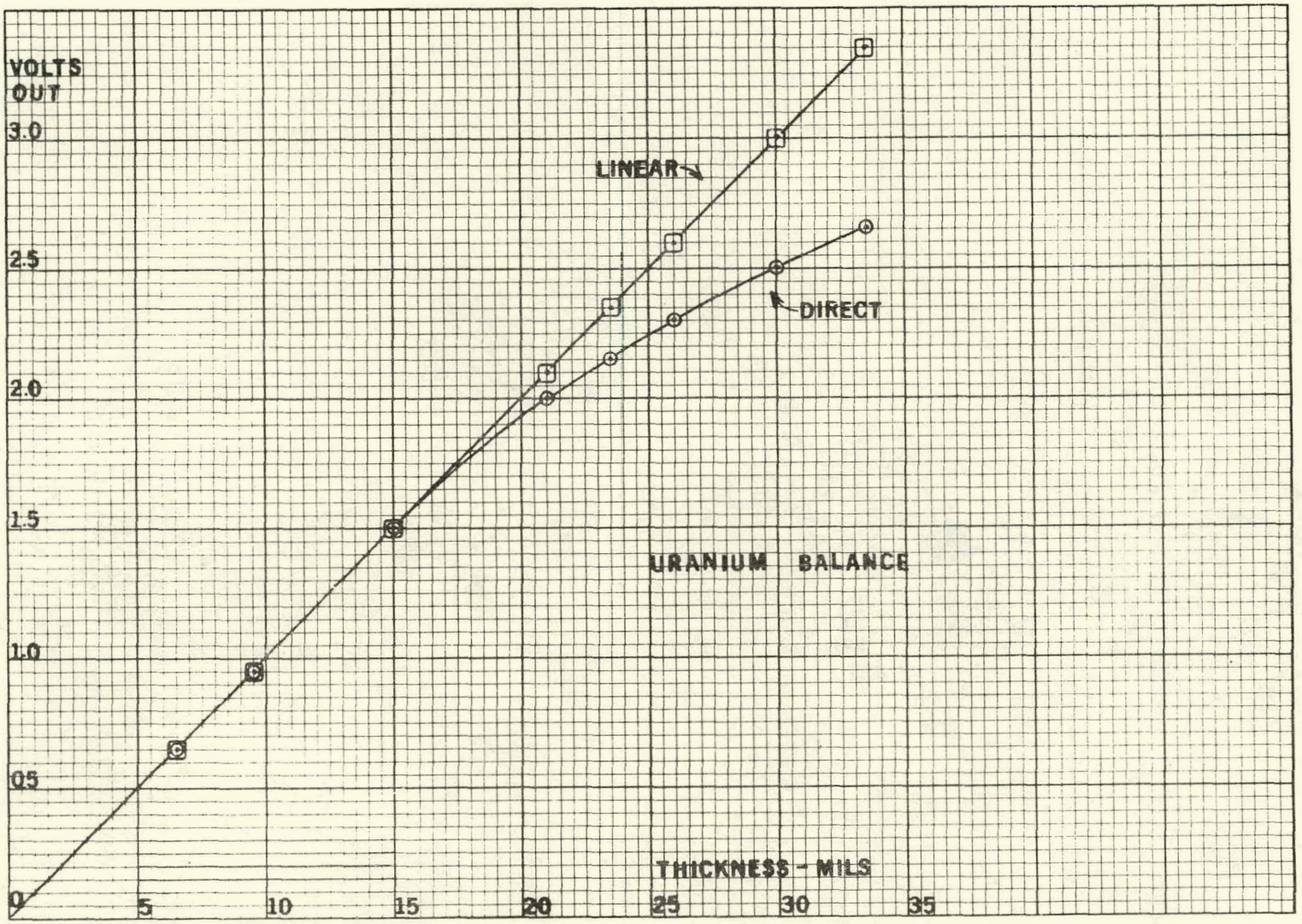


Figure 4. ET-12 responses for both direct and linear modes

1) $V = 0.1t$ for $\left.\right\} 0 \leq t \leq 15$ mils

and 2) $t = 5.2\,(2.0)^V$

which arranges to

$$V = \left(\frac{1}{\ln 2.0}\right) \ln \left(\frac{t}{5.2}\right) \Bigg\} \text{ for } t \geq 15 \text{ mils}$$

where t = thickness & V = direct mode output voltage

## Derivation of Equation 2

The function of Equation 2 was originally derived from plotting the response curve on semilog graph paper, as in Figure 5. For $t \geq 15$ mils, where actual nonlinearity exists, the curve plots as a straight line on semilog paper. This dictates a function of the form:

3) $\ln t = \ln A + V \ln B$ or $V = \left(\frac{1}{\ln B}\right)\left(\ln \frac{t}{A}\right)$

Where B is the slope and A is the thickness intercept for V = 0.

Rearrangement and antilogging yields the form of Equation 2, which is $t = AB^V$.

From direct examination of Figure 5, the zero intercept for the straightline portion of the curve ($t \geq 15$ mils) is A=5.2.

The value for B may be calculated by picking any two points on the curve (for $t \geq 15$ mils) and substituting their values into Equation 3. Picking $P_1$ = 2.5 volts, 30 mils, and $P_2$ = 1.5 volts, 15 mils, we have:

$$\ln 30 = \ln A + 2.5 \ln B$$

and $\ln 15 = \ln A + 1.5 \ln B$

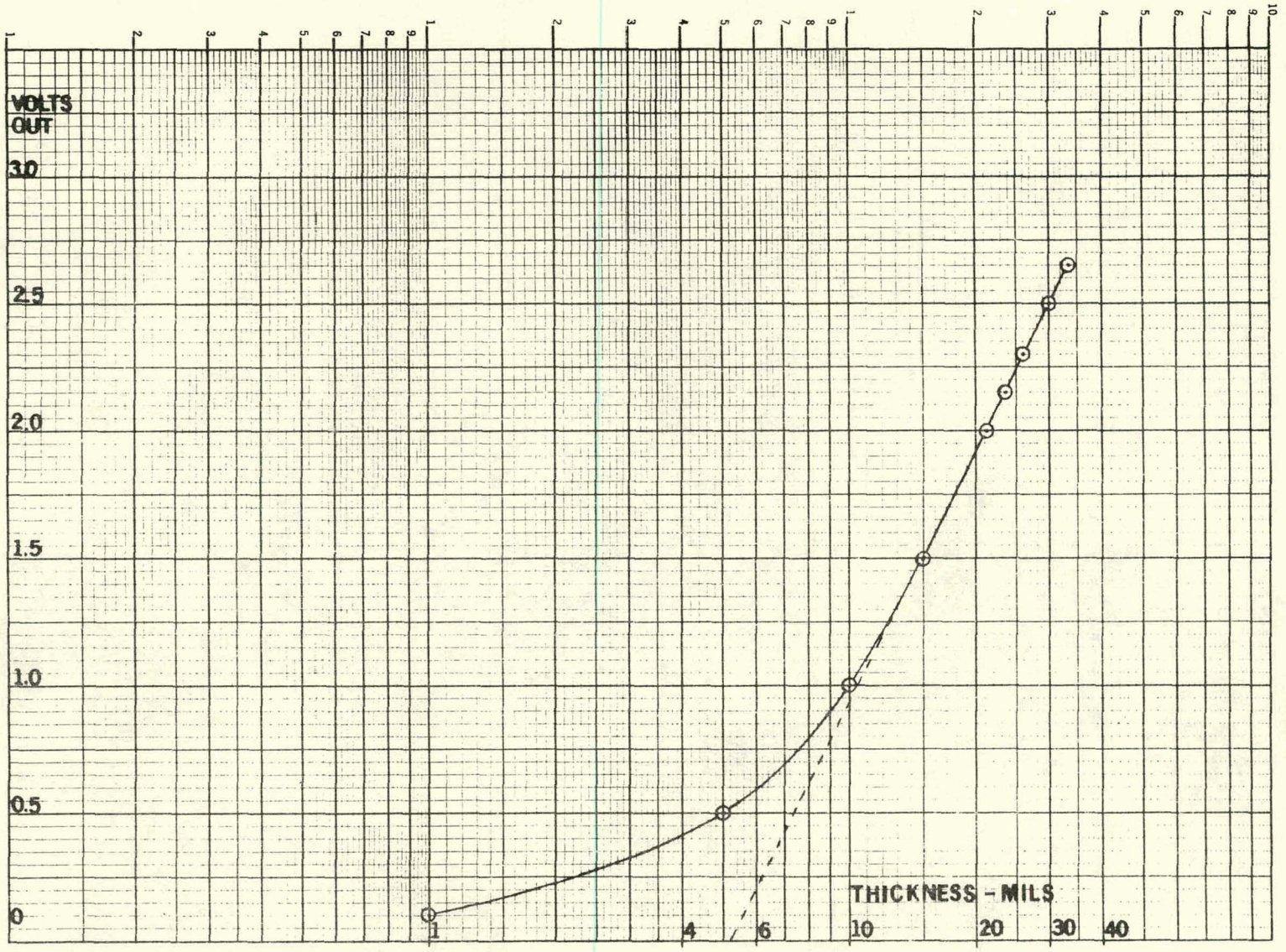


Figure 5. ET-12 direct response plotted on semi-log paper for derivation of curve constants.

Subtraction yields

$$\ln 30 - \ln 15 = \ln B$$

$$\ln \frac{30}{15} = \ln 2 = \ln B$$

$$\therefore B = 2.0$$

Substituting the value for A and B into Equation 3 yields

$$\ln t = \ln (5.2) + V \ln (2.0)$$

Rearranging and taking the antilog yields Equation 2, i.e.:

$$t = 5.2\ (2.0)^{V}$$

## Linearizer Operation

The ET-12 linearizer circuitry operates upon the direct mode voltage to produce

4) $V_{out} = 0.1t$

for all thicknesses in the testers range. This operation pre-supposes that the testers gain is set to produce Vout = 0.1 volt/mil in the naturally linear thickness range ($0 \leq t \leq 15$ mils).

The linearizer contains an analog switch which transfers the board's output to the input voltage for $V_{in} \leq 1.5$ volts, and to the linearized signal for $V_{in} \geq 1.5$ volts.

For $V_{in} \geq 1.5$ volts, the transfer function of the linearizer circuit is:

5) $V_{out}$ (linear) = .52 $\left[\text{alog}_{(2)} V_{in} \text{ (direct)}\right]$

from Equation 2 we have

$$V_{in\ (direct)} = \frac{1}{\ln 2.0} \ln \left[\frac{t}{5.2}\right]$$

Changing the base of the logarithm from naperian (e) to base 2 yields

$$V_{in\ (direct)} = \log_{(2)} \left[\frac{t}{5.2}\right]$$

since $\log_{(2)} (2) = 1$

Substituting this into Equation 5 yields

$$6) \quad \underline{\underline{V_{out\ (linear)}}} = .52 \left\{ a \log_{(2)} \left[\log_{(2)} \left(\frac{t}{5.2}\right)\right]\right\} \quad \underline{\underline{= 0.1t}}$$

which is the system response function in the linear mode for all values of t in the testing range.

The ET-12 linearizer board may be calibrated to straighten curves of the type $t = AB^V$ over a wide range of values for the constants A and B.

See Appendix I for instructions.

# APPENDIX I

## ET-12 CIRCUIT OPERATION

This appendix is divided into four sections. Each section covers the circuit operation for one of the four types of ET-12 circuit boards.

A signal processing block diagram appears in Figure I-1. Figure 1-2 is a complete circuit diagram of the tester, and is available from central files as #H-3-29499.

Primary design features of the ET-12 include:

A) 100% solid state circuitry.

B) No transformers. All balance and phase shift functions are performed with active RC networks. This eliminates the hand-wound transformers contained in original testers.

C) A total of only two chokes per chassis, with only one of these possibly requiring on-site fabrication. (L2 on the probe driver board requires 100 μh at less than 1 ohm dc resistance. This does not appear to be commercially available.) The other choke is in the oscillator tank circuit.

Low pass active RC filters on the balance amplifier board supply 30 DB of second harmonic suppression.

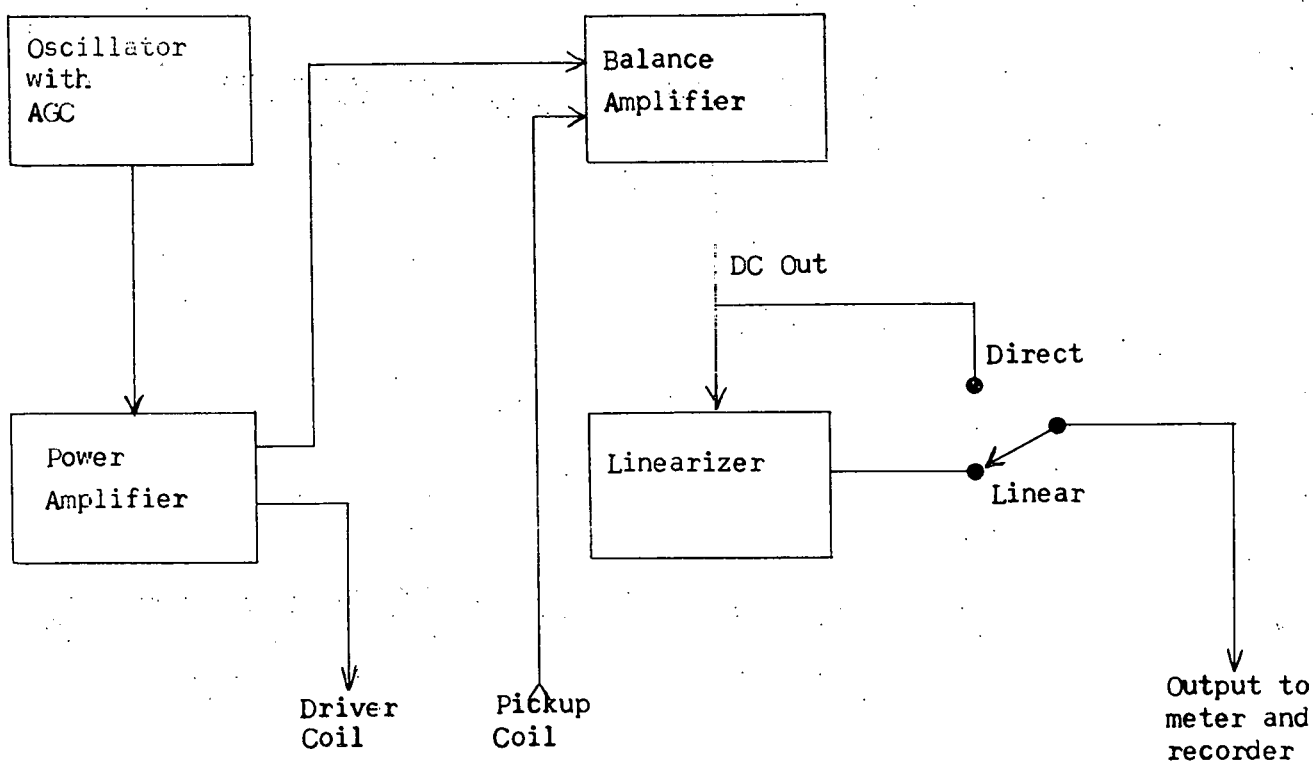


Figure I-1. ET-12 signal processing

D) Automatic Amplitude control of the oscillator output.

E) An integrated circuit driver coil amplifier capable of 15 watts output.

ET-12 OSCILLATOR BOARD

The oscillator is centered about one dual op amp integrated circuit. One of the op amps, A-1, is operated as an LC-tuned feedback oscillator with AGC. The other amplifier, A-2, is used as an output filter and driver.

Oscillator output is rectified in D1 and compared to the reference voltage of zener D2. The difference of these two voltages is fed to the gate of field effect transistor Q1. This transistor operates as a voltage controlled resistor to control the op amp's gain and consequently the amplitude of oscillation.

As D2 is a temperature compensated, sharp turn-on IC zener, very tight control of the loop gain is achieved. This results in ultra stable oscillation amplitude. Amplitude adjustment is made with P1, and should be set to 3 volts pk-pk at the board output.

Oscillation frequency is controlled with L1, and should be set to 20 KHz.

The oscillator output is doubly filtered in the input and feedback loops of the second op amp, which serves as an output driver. Clean waveform is essential at the board output, since harmonic content does not necessarily get nulled along with the fundamental in the balance amplifiers.

One ET-12 oscillator is capable of driving two chassis. This may be attained by pulling the oscillator board from one chassis and completing a connection between oscillator BNC jacks at the rear of each chassis. Two oscillators connected in this manner will not synchronize. Some beat-frequency interferency may appear if two chassis in the same console are operated independently with individual oscillators.

ET-12 POWER AMPLIFIER BOARD

The power amplifier employs a 15 watt IC audio amplifier to excite the driver coil. The design achieves a minimum of components for drive at this power level.

R95 is a critical component for the IC. With pins 4-5 open, the amplifier will draw quiescent current from the DC supply at a flow sufficient for self destruction within several minutes.

Oscillator input is attenuated by R96-R97 to produce approximately 600 ma pk-pk in the driver coil for a 3V pk-pk input at pin A. A heat sink is required to dissipate power lost in the IC so that stable amplifier gain is maintained.

Output circuitry (L2,C45) provides a novel yet obvious function. Coil L2 is needed in series with the driver coil to boost the equivalent load impedance presented to the amplifier. The driver coil impedance is approximately 12 ohms inductive, through which the 600 ma excitation current can easily be forced without loading the amplifier excessively.

The addition of C45 puts the total load presented to the amplifier in or very near to parallel resonance. Total current the amplifier must

supply is thereby greatly reduced and brought near to unity power factor.

ET-12 BALANCE & AMPLIFIER BOARD

The balance and amplifier board[a] contains active RC phase shifting circuitry, summing amplification, 30 DB of second harmonic suppression with active RC filters, and a precision rectifier-DC amplifier.

Reference input from the oscillator undergoes phase splitting in Q2, and switch S1 provides 180° of phase shift. Switch S2 provides 90° phase shift. Transistor Q3 and pot P4 form a transformerless, constant amplitude phase shift bridge for a continuously variable 90° phase shift. Thus the input to Q4 can be shifted a complete 360° around the reference oscillator input. Transistor Q4 provides emitter follower drive to pot P5, which establishes amplitude control of the balance voltage.

Pickup coil voltage is given a gain of 4.7 in Q5. From there it is fed to summing amplifier A3. The output of A3 is the sum of pickup coil and balance voltages. A3 performs the null balance function with a voltage gain of approximately 200.

The output of A3 is fed through two cascaded active RC low pass filters composed of Darlington pairs Q6-Q7 and Q8-Q9. These amplifiers with their twin-T feedback networks produce approximately 30 DB of second harmonic rejection. The composite bandpass characteristic for total system gain is shown in Figure I-3. See reference #2 for a further information on design of these active filters.

Transistor Q10 provides emitter follower output drive for the monitor scope. Q11 is an emitter follower which drives half wave

a) A component layout of this board is included as Figure I-3. All other boards have component locations labeled.

rectifier D4. Rectifier output to DC amplifier A4 contains only negative half cycles. The positive half cycles are conducted to ground through D5, R64 and C32. This is necessary to maintain the net charge on coupling capacitor C31 at zero. The rectified voltage, proportional to pickup coil input, is given a gain of two in A4, with feedback network R12-C35 providing low pass noise filtering.

The maximum net system gain, i.e. the change in DC output for a given change in pickup coil input, is 3200, or 70 DB. Maximum AC gain is 1/2 this value, 1600 = 64 DB.

Amplifier A4 provides DC drive to the recorder output and front panel meter in the direct output mode. It drives the linearizer board in both direct and linear modes.

## ET-12 LINEARIZER BOARD

### Introduction

The ET-12 linearizer board contains a temperature compensated anti-log circuit and a precision analog switch for transferring the board's output between linearized and input signals.

Anti-log circuitry is composed of amplifiers A5, A6 and A7, and transistors Q13 and Q14. Amplifier A8 and transistors Q15 and Q16 make up the switching circuitry.

### Analog Switching Circuitry

Assuming tester calibration as described in the main section of this manual, the tester's direct output voltage is linear up to 1.5 volts = 15 mils. No anti-logging is needed in this range, and the input at pin H

is transferred through switch Q15 directly to the output at pin A. Amplifier A8 is connected in a voltage comparator mode, and will switch when the input voltage becomes greater than the 1.5 volt bias on reference input pin 3. Voltage dividers R90, R91 and R84 establish the reference voltage.

When the input voltage becomes greater than 1.5 volts, the output of A8 drops from + Vcc to - Vcc. This simultaneously turns Q15 OFF and Q16 ON, transferring the board's output to the anti-logging circuitry. A very smooth transition is obtained at the output since both direct and anti-log voltages are equal (1.5 volts) at this point assuming proper linearizer calibration.

## Anti-Log Circuitry

The actual anti-log function is performed by Q14. Amplifier A7 performs as a current-to-voltage converter for output drive. Q14 is driven by voltage follower A6. Summing amplifier A5 drives A6 with the sum of the temperature compensated input voltage and the zero-bias temp-comping voltage from Q13.

It is well known that for almost any silicon transistor, the collector current is proportional to the anti-log of the base emitter voltage. (See references 1, 3, and 4). Stated differently, the base emitter voltage is proportional to the log of the collector current.

The collector current Ic of Q14, all of which flows in R82, produces an output voltage from A7 which is the product of Ic and the value of R82. Therefore the output voltage of A7 is proportional to the anti-log of Q14's base emitter drive voltage. As the base emitter drive is a

function of the tester's thickness voltage, the board's output is an anti-log function of the thickness voltage.

The circuitry between Q14 and the board's input provides temperature compensation for Q14 and conditions the input signal so that linear output is obtained for a given pair of constants A, B in the system thickness response function (Equation 3).

A mathematical analysis of the anti-logging function follows:

It has been shown [a] that log relationships exist in a silicon transistor over as many as nine decades according to the following equation:

7) $$I_c = I_o \exp\left(\frac{q\ Veb}{kt}\right)$$

Where Ic - dynamic collector current

Io = quiescent point collector current

e = natural log base, i.e. 2.718

Veb = base emitter voltage

T = absolute temperature

q = semiconductor constant

k = Boltzmann's constant

Expressed log form, this becomes:

$$Ic = Io\ \text{anti-log}_e \left(\frac{q\ Veb}{kt}\right)$$

In the ET-12 linearizer circuit, the output voltage is $R_{82} \times I_c$, where Ic = Q14 current. Therefore the linearizer output is:

8) $Vout = R_{82} \times I_o \text{ antilog}_e \left(\frac{qVeb}{kt}\right)$

It is desired to drive Q14 with a base emitter voltage Veb which is a function of thickness t so that:

$Vout = .1t$

where t is clad thickness in mils.

Equation 3, $t = AB^{Vin}$, can be written as $t = A \times \text{antilog}_B (Vin)$.

Converting to base e and multiplying by 0.1 yields:

9) $.1t = .1A \times \text{antilog}_e \left[Vin \times \log_e B\right]$

Rewriting Equation 8, we have:

8) $Vout = R_{82} \times Io \text{ antilog}_e \left(\frac{q\ Veb}{kt}\right)$

Comparing similar terms in equations 8 and 9, we see that if

10) $R_{82} \times Io = .1A$

and

11) $\frac{qVeb}{kt} = Vin \log_e B,$

the condition $Vout = .1t$ will be sustained. The ET-12 circuitry performs both of these functions with temperature compensation.

## Temperature Compensation

This type of logarithmic circuit requires two types of temperature compensation in that both the zero quiescent point and the dynamic response are temperature sensitive.

From Equation 10, we can define the quiescent output voltage $Voq = R_{82} \times I_o$. Voq is the output voltage from A7 at zero input voltage to the board. Voq is adjusted with potentiometer P2 which controls the forward bias drop in Q13.

As Q13 and Q14 are a differential pair in one case, they will be at equal temperatures. The voltage from Q13 is fed through to Q14 at a 1:1 ratio so that the quiescent collector current of Q14, and hence Voq, is regulated against temperature. The constant A is determined to be 5.2 from the clad thickness response. For this response then, Voq should be set to 0.520 volts.

From Equation 11, we see that the dynamic response will be temperature compensated if the base emitter input to Q14 is

$$Veb = \left(\frac{kT \log_e B}{q}\right) \quad Vin$$

$\frac{k}{q}$ is approximately $\frac{.0255}{298}$

and $\log_e$ (B=2) is .693

so that

12) $$Veb = \left(.01765\right)\left(\frac{T}{298°K}\right)Vin.$$

This function is provided by Tc1, R76, R77, R73, R78 and P3.

Thus the conditions of Equations 10 and 11 are met, and the anti-log output will be Vo = 0.1t for $t \geq 15$ mils.

Calibration

Calibration of the ET-12 linearizer board is a very simple matter and should only be required when bringing a newly fabricated board into use.

1. Connect a digital voltmeter to the output of amplifier A7 (pin 6). With zero volts input to the board, adjust the output quescent level via P2 to 0.520 volts. (0.1X curve constant A).

2. Adjust tester balance and gain controls to produce 25 microamps deflection on the front panel meter with output selector switch on Direct.

   Set the output selector switch to Linear and adjust P3 on the linearizer board to produce a panel meter reading of 30 microamps.

This completes the calibration procedure. Note that the two meter readings of step 2 correspond to the thickness response curves of Figure 4.

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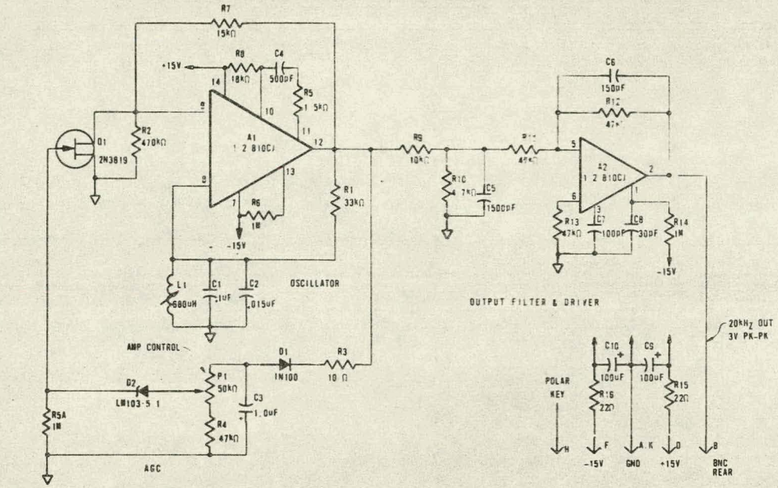
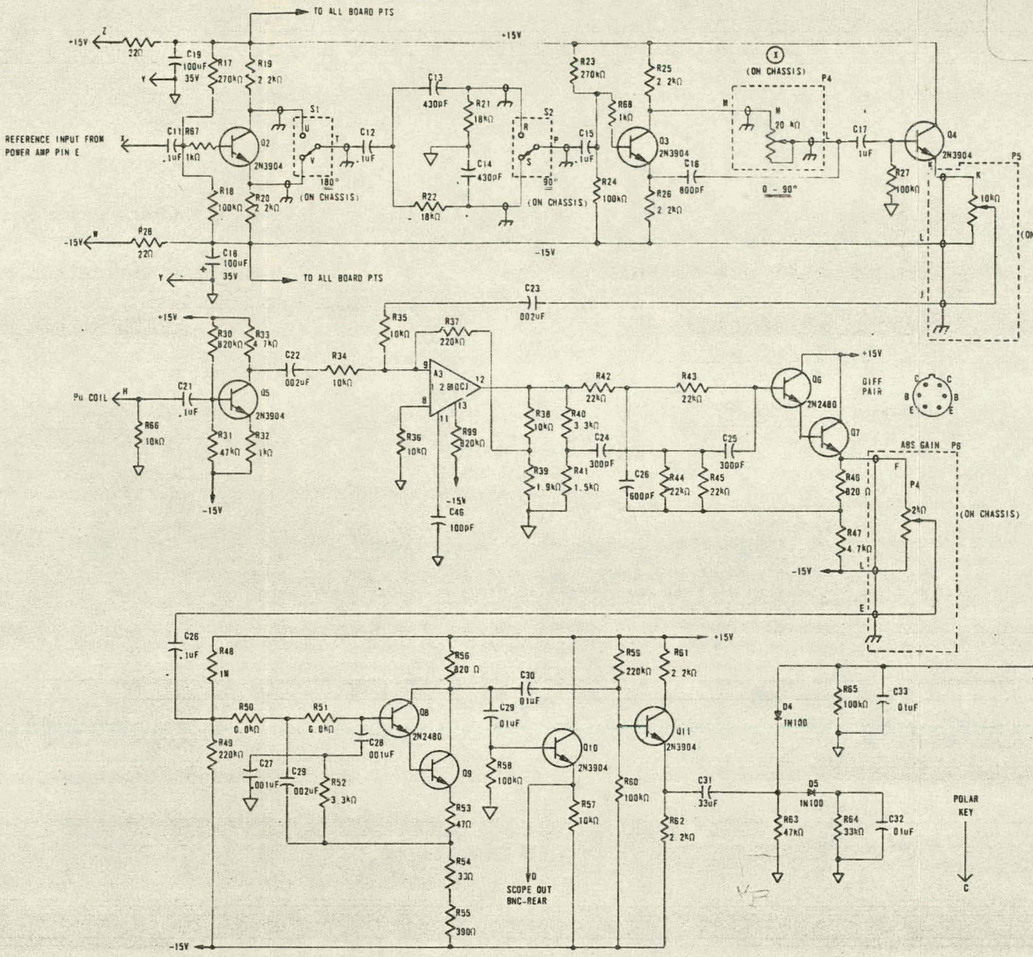
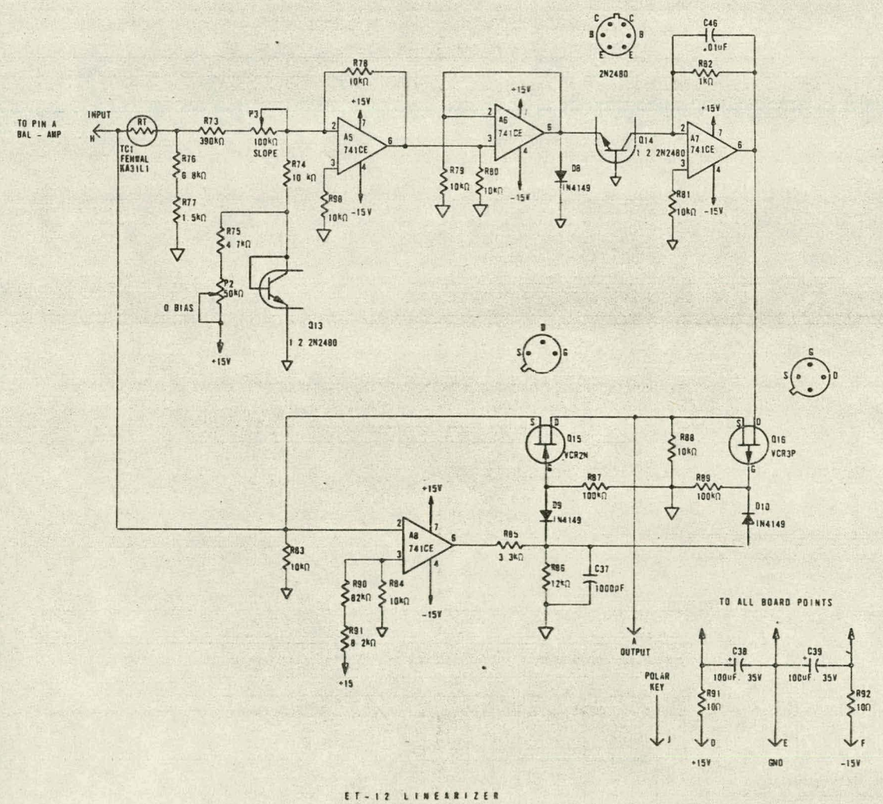
Figure I-2
ET-12 Circuit Diagram




ET-12 OSCILLATOR BOARD

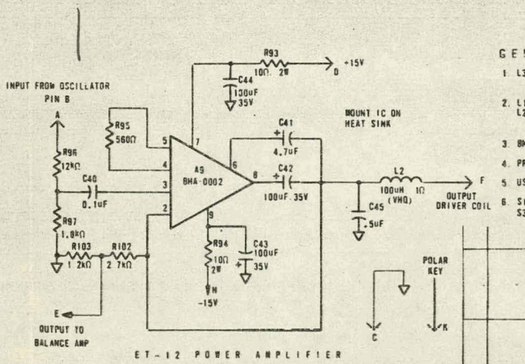



ET-12 LINEARIZER




ET-12 BALANCE & AMPLIFIER BOARD




ET-12 POWER AMPLIFIER

GENERAL NOTES

1. L3 - HOLDER, DIALCO 7545 (HAN STORES 16-1390-170)
   NEON CARTRIDGE, DIALCO 507-4537 (HAN STORES 16-0230-600)
2. L1 - PILOT LIGHT ASSY, RED, DIALCO 162-8430-931 (HAN STORES 16-1820-510)
   L2 - PILOT LIGHT ASSY, GREEN DIALCO 162-8430-932 (HAN STORES 16-1820-500)
   BULB, #327
3. BNC - CHASSIS CONNECTOR, DAGE CHASSES JACK 30517-10 (HAN STORES 16-0975-225)
4. PROBE CONNECTOR - MILITARY 4 PRONG
5. USE RG -174U FOR ALL INTERSOCKET 20 kHz CONNECTIONS
6. S1 S2 S4 - SWITCH, ALCO MINIATURE W ST-1150 (HAN STORES 16-4050-430)
   S3 - SWITCH, ALCO MINIATURE W ST - 215N (HAN STORES 16-4050-435)
7. CHASSIS - AL, 10 X 17 X 3
   FRONT PNL - AL, 1/8 X 19 X 8 3/4
8. ALL SIGNAL CAPACITORS TO BE MICA OR METALLIZED POLYCARBONATE DIELECTRIC FOR TEMPERATURE STABILITY. RECOMMENDED RANGES ARE:
   .0 - .05 μf — MICA
   .05 - .5 μf — POLYCARBONATE
   .5 - 100 μf — TANTALUM ELECTROLYTIC

| MICRO FICHE | BY-DATE | PDS | BY-DATE | PDS | REV BY DATE | DESCRIPTION | REV NO. |
|---|---|---|---|---|---|---|---|
| | | APPD FOR CONFORM WITH DESIGN CRIT | | APPD | | REVISIONS | |
| | | | | | | R107, R103, ZONE B7<br>E8, R67, ZONE F8; R68, ZONE F5,<br>R65, ZONE D4(D) ADDED R66, ZONE<br>VALUES C31, C32, C33, D4, D5, R63, R64<br>D3, D6, D7, R69, D10, ZONE D8, (C) REV<br>W0719 WAS 2.7K Ω, ZONE E6, (B) DELETED | 2 |
| | | | | | | ZONE C6, CHECKED FOR AS BUILT<br>NOTES, ZONE B4 (E) R54 WAS 3.3K Ω<br>ZONES E3, F3 R64 (D) ADDED GEN.<br>D10 + D8, ZONE B11, (C) IDENT POTS,<br>ZONE D12, A6, ZONE D11, A7 ZONE<br>(B) ADDED DIALS 4 & 7 TO AMPS A5,<br>A) ADDED AMP IDENT ZONE F12 F10 B6 | 1 |

| DWG. NO. | REV NO. | DRAWING TITLE OR INDEX NO. |
|---|---|---|
| REFERENCE DRAWINGS | | |
| NEXT USED ON | | |

COMMENT PRT ISSUE NO. | CHECK PRT ISSUE NO. | LAST REV 2
DRAWING STATUS

| | | |
|---|---|---|
| APPD. FOR CONFORMANCE WITH DESIGN CRITERIA | BY | DATE |
| | PDS | |
| APPD | | |
| APPD | J. J. Davis | 10-6-69 |
| DRWG | T. J. DAVIS | |
| DPTG APPD | | |
| CHECKED | | |
| DRAWN | J. MATEO | 6-11-69 |
| SCALE | NONE | |
| CLASSIFIED BY | J. W. Snider | 6-24-69 |
| CLASSIFICATION | NONE | |

U. S. ATOMIC ENERGY COMMISSION
RICHLAND OPERATIONS OFFICE
PACIFIC NORTHWEST LABORATORY
OPERATED BY BATTELLE MEMORIAL INSTITUTE

ET-12
CIRCUIT DIAGRAM

BLDG. NO. 326 | INDEX NO. 4801
DWG NO. H-3-29499 | SHEET NO. 1 | REV NO. 1

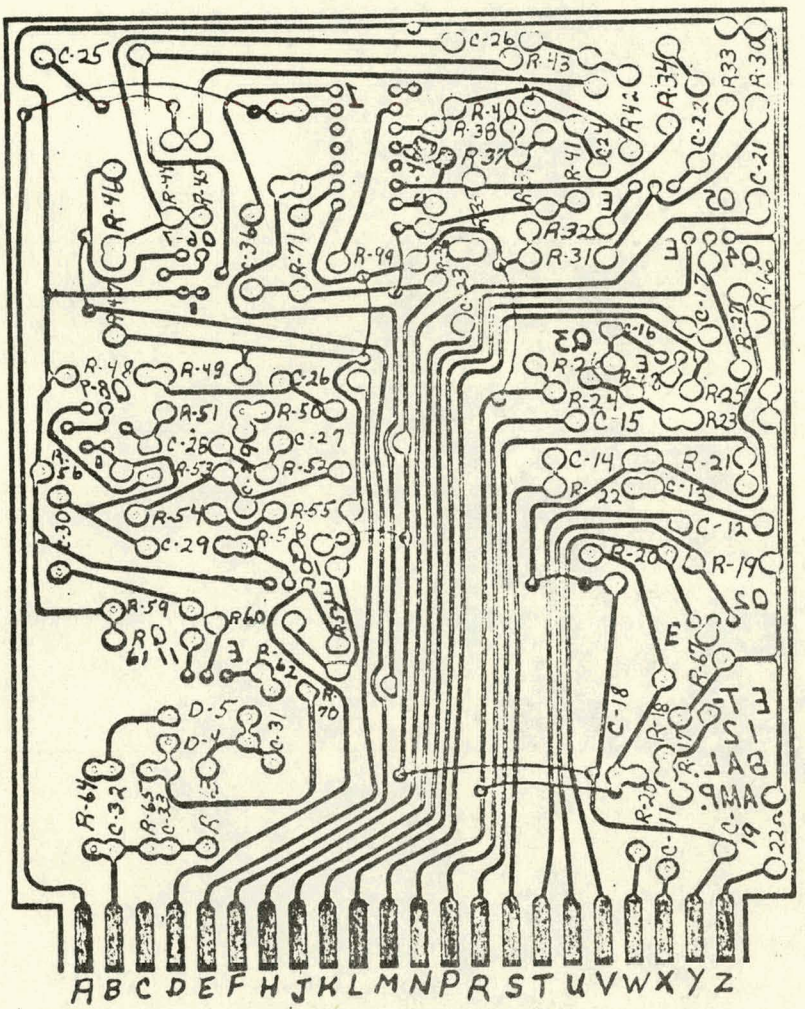



Figure I-3. Component layout for balance amplifier board. (FRONT VIEW) All other boards have component locations labeled.

# APPENDIX II

## ET-12 CIRCUIT SPECIFICATIONS

### INTEGRATED CIRCUITS

A1, A2, A3, A4.....Amelco type 810 CJ dual op amp. External compensation required. Slew rate can be increased 10X by 1M between pin 1 (or 13) to -Vcc.

A5, A6, A7, A8.....Amelco type 741CE internally compensated op amp.

A9.....Bendix type BHA-0002 audio power amplifier. 15 watts total output at room temperature.

D2, D11.....Sharp turn-on monolithic zener. 5.1 volts. National Semiconductor type LM103-5.1.

### TRANSISTORS

Q1.....N-Channel junction FET. 2N3819. HSS-16-3043-819.

Q2, Q3, Q4, Q5, Q10, Q11.....NPN Silicon general purpose. 2N3904 - HSS 16-3043-904.

Q6-Q7, Q8-Q9, Q13-Q14.....NPN Silicon dual transistor. 2N2480 - HSS-3042-400.

Q12.....PNP Silicon, Motorola 2N4126.

Q15, Q16.....Junction VCR FETS (low on-resistance). Siliconix VCR2N and VCR3P.

METER

Front panel thickness meter.....Simpson Wide-Vue, type 1329. 0-50 Micro amps, with type 1123 behind-panel bezel mount.

INDUCTORS

L1.....Nytronics Shielded variable inductor, 680 microhenry. Allied stock no. 54 F 0233. (V-L Weeductor)

L2.....Handwound on 1/3" ferrite core. 175 turns of AWG #28 coil wire. Must be greater than 100 microhenry at less than 1ΩDC.

POTS

P1, P2, P3.....Circuit board pots. Non-wire wound. Can be P1 & P2-50K HSS 16-1872; P3, 100K, HSS16-1872-200.

P4, P5, P6.....Minature 10 turn chassis pots. 20K, 10K and 2K. High resolution. Bourns 3507S-1.

CAPACITORS

All capacitors under 10,000 pf to be silvermica. All capacitors from 10,000 pf to .5μf to be metallized polycarbonate such as TRW Series x 463UW. Available from Washington Electronics, Seattle.

All capacitors equal or larger than 1μf to be solid tantalum

DO NOT USE CERAMIC CAPACITORS as they lack temperature stability.

Use of capacitors other than specified above will seriously degrade the tester's stability.

RESISTORS

All resistors to be 1/4 watt except where specified on drawing H-3-29499.