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LSI INTEGRATED CIRCUIT
TEST DEVELOPMENT

PDO 6984819

A. V. Grimm, Project Leader

Project Team:
J. C. Rustman

Internal Distribution March 1974

Prepared for the
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**Kansas City
Division**

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J. C. Rustman**

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Technical Communications

**Kansas City
Division**

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March 1974

Prepared by A. V. Grimm, D/863

Handling and testing techniques were investigated to prevent static electricity overstressing of metal-oxide semiconductor (MOS) integrated circuits. Six areas of testing were involved and automated testing procedures were developed.

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THE BENDIX CORPORATION

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SUMMARY

Methods for handling and testing metal-oxide semiconductor (MOS) integrated circuits to prevent overstressing by static electrical charge were investigated and developed. A Large Scale Integration (LSI) circuit presently used is the first application of the MOS technology.

Testing was performed in six areas: static charge damage; dc testing of process evaluation test circuits; dc testing of MOS LSI devices; functional testing of MOS devices; switching time testing of MOS devices; and fault testing of MOS devices. Static charge testing was performed to determine the conditions and levels at which the device is damaged by dc static charge. The test circuits were tested to determine if automatic equipment could be used to test MOS devices. Testing was then performed on MOS test circuits to establish possible problem areas with the actual product. Finally, function testing, switching time testing, and fault testing were attempted to determine requirements for test equipment, and the ability of the Fairchild 5000C tester to meet these requirements.

The Fairchild 5000C is capable of only limited testing of MOS LSI devices. Precautions must be taken to ensure that the MOS leads never encounter more than 110 volts, (for test devices evaluated). This voltage may be generated by line charging, or by any static charge buildup mechanisms such as friction or tester forced conditions. Limitations of the Fairchild 5000C require that the devices be tested at a low frequency. These limitations would not permit switching time tests. However, testers that will overcome such limitations are commercially available.

DISCUSSION

SCOPE AND PURPOSE

Handling and testing methods were required that would not generate sufficient static electricity to overstress MOS LSI devices. Methods were needed to test these devices at 250 kHz.

Methods investigated include the following:

- A test sequence to assure that the device under test is exercised through most or all possible usage functions (As many as 225,000 electrical tests per device may be required.);
- A method for handling and testing the integrated circuit without overstressing the device by static electrical charge;
- Static (dc) tests that do not overstress the integrated circuits;
- A method for functional testing of the integrated circuit at a frequency of 250 kHz; and
- A method for making switching time measurements at a functional test rate of 250 kHz.

ACTIVITY

Static Charge

The MOS LSI devices of concern consist of metal-oxide semiconductor field-effect transistors (MOSFET) with diode protection on the input terminals.

MOSFET gates are constructed with a metal layer (or conductive material other than aluminum) over a glass layer over silicon. This construction causes the gate to appear as a very small capacitor and an extremely high input-impedance structure. If a static charge is encountered from an external source, a charge will build up on the FET gate capacitor which is a function of the external source capacitance, original charge on the source capacitance, and the gate capacitance. If this charge exceeds the gate oxide breakdown voltage, permanent damage occurs, and the ruptured oxide will provide a low-impedance path from the gate to the substrate. The FET will therefore cease to function properly.

Input Diode Protection

Diode protection* on input gates provides a low-impedance discharge path for external charges. This protection consists of a resistance connected in series with a diode to substrate. When a charge is transferred from an external source to the FET gate, the voltage builds up to the diode breakdown voltage, creating a low-impedance path to the substrate. With proper diode characteristics, gate damage should not occur.

The principal problem with this type of gate protection is that the transient time of the protection diode is finite (not zero). The time constant of the input charge transfer is extremely short; therefore, there is always some possibility that the gate or the protection diode may be damaged. Unfortunately, this condition exists at the point of optimum design (the point of maximum signal transfer) or the lowest series impedance to the gate and highest parallel dynamic impedance to the substrate.

The inputs of the MOS LSI evaluated were protected by input diodes (Figure 1). Figure 2 is a cross-section and Figure 3 is a schematic of the diode. An oscillograph of the leakage current of one such input is shown in Figure 4, indicating that reverse breakdown occurs at approximately 48 volts. The Voltage-Current (V-I) characteristics of an input are shown in Figure 5. Since the input consists of a MOS gate in parallel with the input protection diode, the curve of Figure 5 is a close approximation of the input-protection diode. Figure 5 also shows that the effective series resistance is approximately 2000 ohms.

Two input diodes were taken to reverse breakdown and the light emitted during avalanche breakdown was photographed (Figure 6). Another input protection diode geometry is shown in Figure 7. In all instances, breakdown occurs at the PN junction at the leading edge of the field plate. Additional breakdown occurs at regions of high curvature in the field plate because of the high potential gradient.

Handling

An alternative solution to the problem of input gate damage is to ensure that the gate is never exposed to an external static charge. If all the pins of the device are shorted together, a potential difference between the substrate and

*"Gate Protection of MIS Devices" IEEE Transactions on Electronic Devices, Volume ED-18, No. 4, April 1971.

Figure 1. Two Input-Protection Diodes on the SA2143 MOS LSI

Figure 2. Cross Section Representation of Input Protection Diode

Figure 3. Schematic Representation of Input Protection Diode

Figure 4. Input-Protection Diode Reverse Leakage and Breakdown. SA2141/SA2143 MOS LSI

Figure 5. Input-Protection Diode V-I Characteristics. SA2141/SA2143 MOS LSI

Figure 6. Breakdown Avalanche Light Emission of Input-Protection Diodes, SA2143 MOS LSI

Figure 7. Breakdown Avalanche Light Emission of Input-Protection Diodes, SA2143 MOS LSI

any input is not possible. This is easily accomplished by a mechanical shorting ring; however, the shorting ring must be removed before testing. Handling conditions must be carefully controlled during these times. The following precautions are recommended.

- Ground the operator using low impedance wrist strips.
- Work on grounded tables.
- Ground all structural metal surrounding the test fixture.
- Control relative humidity at 50 percent minimum.
- Hold tester pins at ground potential while inserting devices into the test head.

A long length of cable is connected to each pin when devices are automatically tested. If sufficient static charge is present on the cable at the time of device insertion, it is possible for device failure to occur. Therefore, elimination of static charges on the cable is one requirement of the test program.

To determine the ability of the cable to hold static charge, measurements were made of the capacitance and resistance at each device pin. Access to the complete test system was not possible; therefore, measurements were made in two sections. Measurements were first made of only the tester lines, looking back into the tester. Secondly, the test socket was characterized (Figures 8 and 9).

From these measurements, the capacitance shunting the device under test ranged from 13 to 16 picofarads from pin to ground. The pin to pin capacitance seen by the device under test (Table 1) varies from an unmeasurable low value to 17 picofarads. The closer the pin spacing, the higher the pin to pin capacitance. All resistances were higher than the measurement capabilities of available meters. A megohm meter was considered, but the possibility of damage to the tester by the high voltages associated with such a meter eliminated this technique. It was concluded from these measurements that the tester was capable of holding a charge, even if for only a few micro-seconds. To determine the magnitude of this danger, a charge was established on the line, and the decay time was measured.

A tester power supply was used to apply a voltage to the cable to establish a charge. This required that the relays in the test head be switched to charge a given line from a voltage present on an adjacent line, then the relay was opened. This technique was used because the tester returns the power supply to zero output voltage before disconnecting it from the line. Prior to the

P1	S1	J1	P2	S1	J1	P3	S1	J1	P4	S1	J1
1-2	1	1	1-2	21	24	1-2	41	44	1-2	61	65
4-5	2	2	4-5	22	25	4-5	42	45	4-5	62	66
8-10	3	3	8-10	23	26	8-10	43	46	8-10	63	67
12-13	4	4	12-13	24	27	12-13	44	47	12-13	64	70
15-16	5	5	15-16	25	28	15-16	45	48	15-16	Banana Jack	71
18-20	6	7	18-20	26	29	18-20	46	49	18-20		72
22-23	7	8	22-23	27	30	22-23	47	50	22-23		73
25-26	8	10	25-26	28	31	25-26	48	51	25-26		74
28-29	9	11	28-29	29	32	28-29	49	52	28-29		75
31-32	10	12	31-32	30	33	31-32	50	53	31-32		76
34-35	11	13	34-35	31	34	34-35	51	54	34-35		77
37-38	12	14	37-38	32	35	37-38	52	55	37-38		78
40-41	13	15	40-41	33	36	40-41	53	56	40-41		J2-71
43-44	14	16	43-44	34	37	43-44	54	57	43-44		J2-72
46-47	15	17	46-47	35	38	46-47	55	58	46-47		J2-73
49-50	16	18	49-50	36	39	49-50	56	59	49-50		J2-74
52-53	17	20	52-53	37	40	52-53	57	60	52-53		J2-75
55-56	18	21	55-56	38	41	55-56	58	62	55-56		J2-76
58-59	19	22	58-59	39	42	58-59	59	63	58-59		J2-77
62-63	20	23	62-63	40	43	62-63	60	64	62-63		J2-78

P1-P4 F5000C Test Socket
 S1 SA2141 Test Socket
 J1, J2 External Load Socket

Figure 8. Wiring Diagram Socket 1 of the Test Adapter

S2	J2	S2	J2	S2	J2
1	1	27	30	53	56
2	2	28	31	54	57
3	3	29	32	55	58
4	4	30	33	56	59
5	5	31	34	57	60
6	7	32	35	58	62
7	8	33	36	59	63
8	10	34	37	60	64
9	11	35	38	61	65
10	12	36	39	62	66
11	13	37	40	63	67
12	14	38	41	64	70
13	15	39	42		
14	16	40	43		
15	17	41	44		
16	18	42	45		
17	20	43	46		
18	21	44	47		
19	22	45	48		
20	23	46	49		
21	24	47	50		
22	25	48	51		
23	26	49	52		
24	27	50	53		
25	28	51	54		
26	29	52	55

S2 SA2143 Test Socket
J2 External Load Socket

Figure 9. Wiring Diagram Socket 2 of the Test Adapter

Table 1. FST 5000C Tester Line Capacitance (C measure between Pin x and Pin 10)

Pin x	C	Pin x	C	Pin x	C	Pin x	C
1	1.02 picofarad	16	17.2	31	18.11	46	4.06
2	17.13	17	17.2	32	11.2	47	27.46
3	1.55	18	17.2	33	22.82	48	15.78
4	1.55	19	11.72	34	1.38	49	1.03
5	1.85	20	17.4	35	20.22	50	3.34
6	15.03	21	1.16 picofarad	36	4.62		
7	1.7	22	- - -	37	3.87		
8	1.15	23	- - -	38	3.85		
9	1.53	24	- - -	39	4.6		
10	- - -	25	- - -	40	3.15		
11	2.48	26	- - -	41	3.34 picofarad		
12	1.35	27	- - -	42	3.44		
13	6.0	28	- - -	43	10.64		
14	10.0	29	- - -	44	23.67		
15	14.45	30	1.36	45	7.66		
Capacitance of test socket ranges from 6.54 picofarad to 7.3 picofarad to pin 10. Capacitance of any tester line to frame ground varies from 13.2 picofarad to 18.7 picofarad.							

charging of the lines an electrostatic voltmeter was connected to the line being tested.

Voltage decay occurred; however, the decay time constant was very long, indicating that the capacitance of the line and the capacitance of the electrostatic voltmeter could maintain a charge for a considerable time.

A 10-picofarad capacitor was then connected between two pins, the electrostatic voltmeter connected between these pins, and finally the lines associated with these pins were charged to 190 volts. The 10-picofarad capacitor was used to simulate the removed test socket. Voltage was measured as a function of time. The time from the relay opening until 71 volts was reached (one time constant) was measured and found to be 320 seconds (Figure 10). The voltmeter was removed from the circuit and a capacitance of 60 picofarads was measured at the tester input.

The voltmeter capacitance varies with applied voltage as can be seen in the discharge curve of Figure 10. The measured capacitance at 85 volts was 50 picofarads and 220 picofarads at 300 volts. Assuming that the C-V relationship is linear:

$$C = AV + B \quad (1)$$

$$\begin{aligned} \text{Then: } 50 &= A(85) + B \\ 220 &= A(300) + B \end{aligned}$$

Solving both equations:

$$A = \frac{170}{215} \text{ picofarads/volt}$$

$$B = -17.2 \text{ picofarads}$$

Since the calculation of tester resistance to common is complicated by the variation of the voltmeter capacitance with voltage, the voltmeter capacitance will be assumed to be a constant, measured at 150 volts, to simplify calculations.

Therefore, at 150V

$$C = \frac{170}{215} (150) - 17.2 = 101.3 \text{ picofarads}$$

Then:

$$C_T = C_{(\text{tester})} + C_{(\text{voltmeter})} = 60 + 101$$

$$C_T = 161 \text{ picofarads}$$

The internal resistance of the voltmeter was 10^{15} ohms. From a RC calculation, the resistance of the tester input is approximately 2.0×10^{12} ohms. Using

Figure 10. RC Decay, FST 5000C Tester Cable

this resistance value and the tester input capacitance of approximately 60 picofarads, the time constant is 120 seconds. If a charge were introduced on the cable, it would take 360 seconds to decay (three time constants).

To determine the amount of charge required to damage an FET, the value of input capacitance of the FET was measured and was found to be approximately 3.5 picofarads (Table 2). By connecting the substrate, source, and drain terminals and applying a voltage between this node and the FET gate, the breakdown voltage of the gate oxide layer could be measured. A curve tracer was used. Breakdown was defined to be the point at which the current level reached one microamp. This test was performed on several devices and appeared uniform, the breakdown voltage being approximately 110 volts. Sufficient data was taken to predict a breakdown limit.

Since $C = Q/V$,

where:

V_B = FET Breakdown Voltage;

V_H = Voltage threshold beyond which damage is expected to occur due to static charge;

C_1 = Capacitance of the tester line, FET, and tester socket;

C_2 = Capacitance of the tester line only;

Q_F = Value of charge on the line after the device is connected; and

Q_T = Charge on the tester line prior to device connection;

Then:

$$C_1 = \frac{Q_F}{V_B}, \text{ and } C_2 = \frac{Q_T}{V_H} \quad (2)$$

Assuming no initial charge on the FET gate:

$$Q_F = Q_T, \quad (3)$$

$$C_1 V_B = V_H C_2, \quad (4)$$

$$V_H = \frac{C_1}{C_2} V_B. \quad (5)$$

Inserting measured values of C_1 , C_2 , and V_B

$$V_H = \frac{23.5}{20} (110) = 129.0 \text{ volts}$$

Table 2. Measured Capacitance of SGT-4 Test Circuit

Device Pin	Capacitance to Substrate (Pin 10)	Function	Device Pin	Capacitance to Substrate (Pin 10)	Function
2	17.13 picofarads	Small thin FET source	27	20.22	Poly AL contacts
6	15.02	Small thin FET drain	28	4.62	Thick metal drain
7	1.7	Small thin FET gate	29	3.87	Intermediate poly FET gate
10	- - -	Substrate	30	3.85	Intermediate poly drain
11	2.48	Gates shorts test structure	31	4.6	Intermediate poly source
12	1.35	Gates shorts test structure	32	3.15	Thin gate FET drain
13	6.0	Gates test, metal	33	3.34	Thin gate FET source
14	10.0	Gates test, Plate 1	34	3.34	Thick gate FET drain
15	14.45	Gate test, Plate 2	35	3.44	Thin Poly FET gate
16	17.2	Thin oxide capacitor	36	10.64	String of poly-AL contacts
18	11.72	Monolithic P+ capacitor	37	23.67	Poly P+ butting
19	17.4	High side small P+ resistor	38	7.66	100 buried poly P+ contacts
23	18.11	High side Poly Resistor	39	4.06	AL over poly P+ contacts
24	11.2	Intermediate oxide capacitor	40	27.46	Intermediate thin oxide capacitor
25	22.82	Poly P+ - Poly P+ contacts	41	15.78	High side poly resistor

This calculation shows that breakdown should occur when the static voltage on the cable is approximately 130 volts.

To test these calculations, a voltage was applied to the cable. A 100V potential was applied in the manner described, and an MOS device was inserted into the test socket. This test was performed on four good devices with no failures observed. A charge of 110 volts was then developed on the cable. After 50 insertions the device remained good. The charge was increased to 120 volts on the cable. Two of the five FET on each device failed during the first 120 volt insertion test. From this testing the observed breakdown potential was found to agree reasonably with the calculated value.

The importance of some of the parameters described must be emphasized.

- Capacitance of tester cable (the ability of a tester line to hold a charge) should be as low as possible.
- The parallel resistance of the tester line (the time constant associated with discharge of a static voltage) should be as low as possible without introducing measurement error.
- Holdoff voltage (the voltage to which a line may be charged without damage to a device under test) is a function of device design.

However, if handling precautions are observed and precautions are taken to keep the tester lines free of static charge, MOS devices can be inserted into test sockets without damage.

DC Testing

A test circuit was obtained from Fairchild Semiconductor to determine the requirements for dc testing on a MOS LSI type device. The Fairchild SGT-4 circuit contains a number of representative types of device structures normally encountered in MOS LSI devices. By performing various dc tests on this circuit, problems in testing MOS devices can be easily analyzed.

The SGT-4 circuit contains five independent FET, each with a different geometry. There also are four resistors with different geometries, five different types of contacts, four different capacitors, and a large-periphery gate-simulation structure. No diode protection is used on this test structure; therefore, any leakage measurement is a true indication of device parameters. Care must be taken because the gate structures are afforded no protection against static charge. A test sequence was written and performed by the Fairchild 5000C automatic tester. Each test is described and typical results are listed in Appendix A. It is possible to repeatedly test MOS-type devices

without damaging the device. Further, this testing appears to yield meaningful and repeatable results, providing the proper handling precautions are observed.

SA2141/SA2143 Breakdown Voltage and Input Leakage

Having established that MOS type devices can be tested on an automatic tester, the next step was to test an actual MOS LSI device to the device's dc test requirement. The SA2141 and the SA2143 devices were used to establish the limitation of the Fairchild 5000C tester to perform dc testing on MOS LSI devices. The SA2141 and SA2143 devices are packaged in 64 pin flatpack packages. A test adapter was constructed to facilitate the testing of these devices. The SA2141 and SA2143 are MOS LSI devices with diode input protection.

Breakdown voltage tests were established on inputs and outputs of both device types. Tests were then performed to determine the number of times breakdown testing can be performed and not significantly degrade the device. Since breakdown testing involves high voltage, a means of limiting the maximum voltage is required. Maximum voltage is a programmable function of the 5000C. For all testing performed on the 5000C, a 65 volt limit was set. This voltage is considerably lower than the danger level of 120 volts.

First, a series of breakdown voltage tests were performed on six different inputs of the SA2143. Breakdown is defined as the voltage at which 10 microamperes of current flowed. Testing was repeated up to 50 times. No significant degradation of the device occurred (Figure 11). One input was then taken into breakdown 150 times with no significant degradation (Figure 12).

Another input was taken to breakdown. This time the breakdown current level was varied from 10 microamperes to one milliamperere (Figure 13). No significant degradation occurred. It should be noted that all repetitions mentioned involve the removal and re-insertion of the devices. From this data it is concluded that the repeated performance of breakdown tests, with proper precautions, will not damage an MOS type device.

Similar tests were performed with input leakage current tests. The SA2141 MOS LSI was used. However, when repeated testing was performed, random failures occurred. The same tests were then performed on the SGT-4 FET gates and no such failure occurred. The leakage current test was viewed on an oscilloscope. A leading edge spike was observed which ranged from 0 to 60 volts. This spike apparently broke down the diode protection and once this occurred, a substantial period of time was required for the diode to recover. If leakage current measurements were made during this period

Figure 11. SA2143 Breakdown Voltage at 10 Microamps

Figure 12. SA2143 Breakdown Voltage at 10 Microamps

Figure 13. SA2143 Breakdown Voltage

of time, the current measured would be that flowing through the "broken-down" diode. The spike was due to the normal transient associated with the undamped, charged tester cable. The spike was eliminated by linearly increasing the power supply up to the operating voltage value. A protection diode on one input was purposely taken into breakdown with a 100-volt 100-microsecond pulse. Leakage current tests were performed every 100 microseconds thereafter. Leakage current readings did not stabilize until approximately 50 seconds after the initial breakdown.

It was concluded that two requirements are necessary in order to perform satisfactory leakage current measurements. The first is that it be well established that the protection diodes are not taken into breakdown before performing the leakage test. The second is that there is not a transient of sufficient amplitude to break down the diode while the test is being performed.

DC Parametric Testing, SA2141, SA2143

Nonclocked Tests

The SA2141 and SA2143 dc testing procedures are described in Appendices B and C. No significant problems were noted on tests which required the device to be in the unlocked state. If the test required clocking the device to obtain a prescribed state before testing, this test was not performed. A significant portion of the dc testing on each device was not done. The test routine takes approximately 2.5 minutes. About one minute of this time is used in eliminating the possibility of a broken-down input-protection diode. Although dc programming is extremely long, the tests are easily performed. Therefore, the through-put of an LSI tester is severely limited by the number of tests required and the speed with which the tests may be performed.

Clocking Tests

To fully test a MOS LSI device, it is necessary to verify that all outputs are in the correct state. The SA2143 requires more than 20,000 clocking pulses to obtain some output states. Since the device is intended to operate at 200 to 500 kHz, the tester must be capable of delivering a train of pulses at this rate. The Fairchild 5000C is capable of a minimum pulse cycle time of 250 microseconds which does not approach the desired 200 to 500 kHz rate.

Since the Fairchild 5000C has a cycle time of two microseconds, the available upper frequency is seriously limited. If the test routine were written in assembler language, it would be possible to reach a clocking frequency approaching the cycle time of the tester. An attempt was made to establish such a program. The task could not be accomplished in a reasonable time; therefore, the effort was discontinued.

An external pulse driver/counter was fabricated to perform the function of generating the pulse train. A set of front-panel-mounted digital switches allowed programming the maximum number of pulses to be delivered. This pulse driver/counter includes an internal 250 kHz multivibrator. The pulser is operated with three control inputs: set pulse, reset pulse, and trigger pulse. The inputs are brought to the front panel to allow an interface with the adapter box so that the tester can control timing. With these connections made, the pulser can deliver a preset number of pulses to the MOS LSI at a time determined by the tester, and as many times as required. The upper frequency range of these pulses is 1.0 MHz.

Using the adapter and a programmable pulse counter/driver, the SA2143 was exercised. The first five sequential outputs were obtained. However, because of the complexity of the circuit and the limitations of the 5000C in providing multiple clocking inputs, it became impossible to clock the SA2143 through the entire sequence without knowing in advance the precise sequence of operation. Clocking the SA2141 is even more difficult because more clocking inputs are required. Therefore, it became easier to program the SA2143 input and use it to drive the SA2141. The two devices were mounted in the test head, and the sockets jumpered together to form the interconnections in Table 3. The power supply is delivered through pins 56 and 55 in parallel with pins 57 and 58, eliminating the possibility that a transient caused by switching the information inputs would either be interpreted as a clocking pulse or a reset pulse.

In clocking a device to some prescribed state, a testing of the device's functioning ability is performed by virtue of arriving or not arriving at the prescribed state. Therefore, the order of testing was slightly revised: first, a technique of totally exercising the device was developed, then dc measurements were made.

A functional test series was designed to correctly exercise the LSI pair through most of the functional modes (Figure 14). The program runs properly if a good device is tested. If a bad device is inserted and one of the expected results is not obtained, the tester will not stop testing because of the lack of escape routines available in the 5000C programming language. A subroutine was written in assembler language to provide an escape function. Data was taken by inserting dc tests in the proper position of this functional test sequence. An extensive characterization of device performance was performed using this technique.

Table 3. Pin List for Pair Testing on FST 5000C

SA2141	SA2143	Signal	SA2141	SA2143	Signal
1	48	CDM	15	34	SCN
2	47	WSM	16	33	VCS
3	46	CCN	20	20	PFB1
4	45	CBN	21	21	PFB2
5	44	CAN	22	32	VG
6	43	UKN	57	56	VS
7	42	CEN	58	55	VD
8	41	F2LS	59	54	W14M
9	40	FOLS	60	53	W14R
10	39	PS	61	52	MLRN
11	38	F1LS	62	51	WSHM
12	37	SMGN	63	50	FDMN
13	36	KJSN	64	49	SABM
14	35	TMN

Figure 14. Block Diagram of the Functional Test Program

Switching-Time Tests and Fault Test Sequence

Switching-time testing was not attempted on the 5000C, since this tester requires a pulse train from an output to perform these measurements. Because of the complicated nature of the MOS LSI, pulse trains from a single output normally are not possible. In order to test switching time on MOS LSI it is necessary to take measurements from a single pulse. Testers of this type are commercially available.

A fault-test sequence was written for the 5000C in assembler language. Using this technique, a maximum clock period of 4.0 microseconds was obtained. Because of the development of the previously described functional test capability, a relatively small amount of new information might be obtained from the fault test sequence. Therefore, no attempt was made to complete the fault testing routine.

ACCOMPLISHMENTS

The capacitance and the charge-holding capability measurements of the 5000C tester indicate a possibility of MOS-type device damage due to tester cable charge. The threshold voltage level of this damage-causing charge was measured. Testing was performed, with proper handling techniques, and repeatable results were obtained. The conclusion was that testing MOS devices on automatic test equipment is possible.

A capability to test MOS LSI-type devices has been developed. The limitations and requirements of test systems follow.

- Damage may occur to MOS devices due to fast high-voltage transients which may be caused by charged tester cables. The maximum safe voltage needed on a tester cable and the tester cable capacitance are directly related.
- Nonclocked dc tests are accomplished relatively easily. Because of the large number of inputs and outputs associated with LSI, the test time becomes extremely long, and the through-put of the tester is significantly sacrificed.
- Using proper handling precautions, MOS LSI devices were tested as many as 160 times without significant damage, both with and without input protection circuits.

- DC tests that require an output to be taken to a particular state can be performed, but with difficulty. A functional test routine should first be established, then the clocking is stopped at the proper points and dc tests performed.
- Clocking multiple inputs at multiple harmonic rates is required.
- The tester should be capable of accurately controlling the total number of clock pulses delivered.
- The tester should be capable of clocking over a wide frequency range.
- Because of the large volume of testing required per device, a large tester memory must be available.
- Switching-time testing should be performed with only one-pulse strobing.

FUTURE WORK

The 5000C tester cannot satisfactorily test MOS LSI devices for the following reasons.

- The maximum clocking and functional testing frequency limit is between 1.0 and 4.0 kHz.
- Switching-time determination requires that repetitive pulses be measured. the MOS LSI can provide pulse trains with only a large volume of clocking information. The memory is not capable of retaining the large volume of information necessary, and the pulses to be measured can be several minutes apart because of the slow clocking speed.
- Clocking inputs are limited to five.
- Because of the datalogging format, the interpretation of data is difficult.

The Fairchild Sentry 600 tester overcomes all these problem areas. Therefore, it is recommended for all except very limited testing.

Appendix A

Figure A-1. Gate Shorts Test 1 (Test Number 1)

Figure A-2. Gate Structure Breakdown (Test Number 2)

Figure A-3. Gate Shorts Test 2 (Test Number 3)

50-ohm square resistor
 30 to 110 ohms per square
 $-0.666\text{mA} \geq I \geq -0.182\text{mA}$
 Open circuit -0.001mA
 Typical reading -0.2426mA

Figure A-4. Resistance of Poly 1 (Test Number 4)

20-ohm square resistor
 30 to 120 ohms per square
 $-0.417\text{mA} \geq I \geq -1.67\text{mA}$
 Open circuit -0.001mA
 Typical reading -0.660mA

Figure A-5. Resistance of Poly 2 (Test Number 5)

50-ohm square resistor
 25 to 55 ohms per square
 $-0.8\text{mA} \leq I \leq -0.364\text{mA}$
 Open Circuit -0.0001mA
 Typical reading -0.5870mA

Figure A-6. Resistance of Large P+ Resistor (Test Number 6)

20-ohm square resistor
 25 to 60 ohms per square
 $-2.0\text{mA} \leq I \leq -0.835\text{mA}$
 Open circuit -0.001mA
 Typical reading -1.7mA

Figure A-7. Resistance of Small P+ Resistor (Test Number 7)

7k to 19k ohms

$$-143.0\mu A \leq I \leq -52.6\mu A$$

Open circuit -0.000mA

Typical reading -0.060mA

Figure A-8. Resistance of String (Test Number 8)

10k to 26k ohms

$$-100\mu A \leq I \leq -38.5\mu A$$

Open circuit -0.0001mA

Typical reading -0.0600mA

Figure A-9. Resistance of 100 Buried Poly-P+ Contacts (Test Number 9)

$$-0.8mA \leq I \leq -0.100mA$$

Open circuit 0.000mA

Typical reading -0.180mA

Figure A-10. Resistance of Poly-AL Contacts (100 Contacts)
(Test Number 10)

$$-0.33mA \leq I \leq -0.05mA$$

Open circuit 0.0mA

Typical reading -0.120mA

Figure A-11. Resistance of Poly-P+ Butting Contacts (100 Contacts)
(Test Number 11)

Figure A-12. Resistance of P + AL Contacts (100 Contacts)
(Test Number 12)

Figure A-13. Monolythic Thin Oxide C (Test Number 13)

Figure A-14. Monolythic P+ Capacitor (Test Number 14)

Figure A-15. Interdigitated Intermediate Oxide Capacitor (Test Number 15)

27.5pF

$I = -5\mu\text{A}$ max

Open circuit -0.031 μA

Typical reading -0.060 μA

Figure A-16. Interdigitated Thin Oxide Capacitor (Test Number 16)

Input C = 3.44pF

$-2.2\text{V} \leq V \leq -1.2\text{V}$

Open circuit -14.59V

Typical reading -1.5V

Figure A-17. Thin Gate FET Threshold Voltage (Test Number 17)

$-3.8\text{V} \leq V \leq -2.1\text{V}$

Open circuit -16.38V

Typical reading -2.5V

Figure A-18. Thin Gate FET Delta V Gate (Test Number 18)

$-40\text{V} \leq V \leq -15\text{V}$

Open circuit -118.9V

Typical reading -22V

Figure A-19. Thin Gate Breakdown Voltage (Test Number 19)

$$-0.5\text{mA} \leq I \leq -0.15\text{mA}$$

Open circuit 0.0mA
Typical reading -0.28mA

Figure A-20. Thin Gate R on Test 1 (Test Number 20)

$$-700\mu\text{A} \leq I \leq -38.5\mu\text{A}$$

Open circuit 0.03μA
Typical reading 0.309μA

Figure A-21. Thin Gate on Test 2 (Test Number 21)

$$-300\mu\text{A} \leq I \leq -40\mu\text{A}$$

Open circuit 0.0mA
Typical reading 0.120mA

Figure A-22. Thick Gate on Test 1 (Test Number 22)

Figure A-23. Thick Gate on Test 2 (Test Number 23)

Figure A-24. Thick Gate Threshold Voltage (Test Number 24)

Figure A-25. Thick Gate FET Delta V Gate (Test Number 25)

Figure A-26. Thick Gate FET Breakdown Voltage (Test Number 26)

Figure A-27. Intermediate Poly FET Threshold Voltage (Test Number 27)

Figure A-28. Intermediate Poly FET Delta V Gate (Test Number 28)

Figure A-29. Intermediate Poly FET R on Test 1 (Test Number 29)

Figure A-30. Intermediate Poly FET R on Test 2 (Test Number 30)

Figure A-31. Intermediate Poly FET Breakdown Voltage (Test Number 31)

$$-50V \leq V \leq -20V$$

Open circuit -118.3V

Typical reading -36.0V

Figure A-32. Metal Gate FET Threshold V (Test Number 32)

$$-20V \leq V \leq -50V$$

Open circuit -118.3V

Typical reading -45.0V

Figure A-33. Metal Gate Delta V Gate (Test Number 33)

$$-0.5mA \leq I \leq -0.01mA$$

Open circuit -0.0

Typical reading -0.045mA

Figure A-34. Metal Gate R on Test 1 (Test Number 34)

Figure A-35. Metal Gate FET R on Test 2 (Test Number 35)

Figure A-36. Metal Gate FET Breakdown Voltage (Test Number 36)

Figure A-37. Small Metal FET Threshold V (Test Number 37)

$$-10V \leq V \leq -1V$$

Open circuit -16.38V
Typical reading -7.45V

Figure A-38. Small Metal FET Delta V Gate (Test Number 38)

$$-0.5mA \leq I \leq -0.01mA$$

Open circuit 0.0
Typical reading -0.0145mA

Figure A-39. Small Metal FET R on Test 1 (Test Number 39)

$$-0.5mA \leq I \leq 0.01mA$$

Open circuit -0.0
Typical reading -0.02mA

Figure A-40. Small Metal FET R on Test 2 (Test Number 40)

$$-10V \leq V \leq -1V$$

Open circuit -16.38V
Typical reading -7.45V

Figure A-38. Small Metal FET Delta V Gate (Test Number 38)

$$-0.5mA \leq I \leq -0.01mA$$

Open circuit 0.0
Typical reading -0.0145mA

Figure A-39. Small Metal FET R on Test 1 (Test Number 39)

$$-0.5mA \leq I \leq 0.01mA$$

Open circuit -0.0
Typical reading -0.02mA

Figure A-40. Small Metal FET R on Test 2 (Test Number 40)

$$-40V \leq V \leq -10V$$

Open circuit -119.0V
Typical reading -38.5V

Figure A-41. Small Metal FET Breakdown Voltage (Test Number 41)

$$-45V \leq V \leq -25V$$

Figure A-42. Thin Gate FET Gate Breakdown Voltage (Test Number 42)

$$-45V \leq V \leq -25V$$

Figure A-43. Thick Gate FET Gate Breakdown Voltage (Test Number 43)

Figure A-44. Intermediate Poly Gate Breakdown Voltage (Test Number 44)

Figure A-45. Metal Gate FET Gate Breakdown Voltage (Test Number 45)

Figure A-46. Small Metal FET Gate Breakdown Voltage (Test Number 46)

Figure A-47. Static Charge Eliminated (All Pins Grounded)
(Test Number 47)

Appendix B

Figure B-1. Input Breakdown Voltage

Figure B-2. Output Breakdown Voltage

Figure B-3. Source Current Test

Figure B-4. Input Pullup Characteristics

Figure B-5. Test Inverter Threshold

Figure B-6. Test Inverter Output Impedance, CN

Figure B-7. Test Inverter Output Impedance, OFF

Figure B-8. Test Inverter Output Voltage, OFF

$$100nA \leq I_m$$

$i = 1-5, 7, 12, 14, 20, 21$
45-55, 59-64

Figure B-9. Input Leakage Current

$$100nA \leq I$$

Figure B-10. Input Leakage Current

Figure B-11. Output Leakage Current

Figure B-12. Output Impedance OFF

Figure B-13. Output Impedance, OFF

Figure B-14. Output Voltage, Low

t	V_m Limit
6, 13, 15	4.3V
18, 19	3.5V

Figure B-15. Output Voltage, High

p = 33 - 43

$I_m > -30\mu A$

$E_F = 2.7V$

Figure B-16. Output Bit Drives (LBp)

Appendix C

Figure C-1. Input Breakdown Voltage

Figure C-2. Output Breakdown Voltage

$$I_m < -100nA$$

$i = 26, 27, 28, 33, 34, 36, 38, 39, 40, 41, 43$

Figure C-3. Input Leakage Current

$$I_m < -100nA$$

$k = 1, 3, 14-19, 22, 23, 24, 25, 29, 30, 31, 42, 47-49, 58-64$

Figure C-4. Output Leakage Current

Figure C-5. Source Current

Figure C-6. Input Pullup Characteristics

Figure C-7. Test Inverter Threshold

Figure C-8. Test Inverter Output Impedance

Figure C-9. Test Inverter Output Voltage, Off

Figure C-10. Gate Oxide Breakdown Voltage

Figure C-11. Input Resistor Characteristics

Figure C-12. Output Impedance, OFF

Figure C-13. Output Impedance, OFF

Figure C-14. Output Voltage, Low