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Westinghouse Astronuclear Laboratory

Operational Manual for XE-1 Experimental Controller No. 1 (ETS-1)

DISCLAIMER

Astronuclear Laboratory

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Operational Manual
for
XE-1 Experimental Controller No. 1 Chassis

1. GENERAL

1.1 INTRODUCTION

This operational manual covers the XE-1 Experimental Controller No. 1 Chassis located in Rack 48 and identified by the reference designation 48A6. This chassis contains fuses, test jacks, and the circuit boards for the various subsystem circuits in the chassis. Each subsystem circuit description is complete within the section for that subsystem. Test specifications, photographs, and drawings, which in some instances are common to more than one subsystem, are combined at the end of this manual.

1.2 DESCRIPTION

The chassis consists of a drawer as shown on Drawing 938J912 suitable for mounting in a standard 19" rack. The overall dimensions are 19" wide by 22 1/2" deep by 7" high.

1.2.1 Front Panel

The front panel of the Experimental Controller No. 1 chassis is 19" wide by 7" high. A handle is mounted on each side of the panel. The left handle is equipped with a spring operated mechanical latch to retain the chassis in the closed position in the rack. A button at the upper end of this handle releases the latch when pressed. The handle is equipped with a key lock. The key is removable only when the lock is in the LOCK

position. Five Master Specialties Series 70E fuseholders are located along the lower edge of the front panel.

1.2.2 Chassis

The chassis consists of a frame with chassis slides bolted to the sides. A component plate is bolted inside the frame. Printed circuit board guides and connectors for three rows of ten boards are mounted on the component panel. The guides and connectors accomodate 35 pin boards only. The rear center position is occupied by a grounding module.

On the rear of the chassis are two connector plates. On one plate are mounted the 16 pin power connector J1 and a 55 pin signal connector J2. On the second plate, there is mounted one 55 pin signal connector J3. A chassis ground terminal lug is mounted on the chassis frame between the two connector plates.

1.2.3 Component Panel

Bolted across the top of the chassis at the front is the component panel. This panel contains test point jacks and controls for the chassis circuitry.

2. INSTALLATION

2.1 INCOMING INSPECTION

The equipment was carefully inspected both mechanically and electrically before shipment. It should be physically free of mars, dents, or scratches and should be in perfect electrical order upon receipt. To confirm this, the equipment should be inspected for physical damage from transit and tested for electrical performance using the procedures of Section 5. If there is damage or deficiency, repairs should be made before final use.

2.2 MOUNTING

CAUTION: Before installation of the chassis make sure that all power and signals to the rack are tunred off to prevent possible damage to the equipment or injury to personnel.

The chassis is to be mounted in the lower-half of Rack 48 as the sixth drawer from the top. Mount the removable portion of the chassis slides at the desired level of the rack and insert the Experimental Controller No. 1 Chassis in the slides. Refer to Drawing 938J912 for mounting dimensions and construction details of the chassis, panel, and connectors. Connect the mating cables to the connectors at the rear of the chassis.

2.3 POWER REQUIREMENTS

Power is obtained from external sources and enters the unit through the rear-mounted 16-pin connector J1. The following are the nominal voltage and current requirements:

a. 28 VDC at 1 amp

b. +15 VDC (to I&C Common) at 1/2 amp

c. -15 VDC (to I&C Common) at 1/2 amp

d. +10 VDC (to I&C Common) at 1/2 amp

e. -10 VDC (to I&C Common) at 1/2 amp

3. EXPERIMENTAL TEMPERATURE CONTROLLER CIRCUITS

3.1 DESCRIPTION AND PRINCIPLES OF OPERATION

The Experimental Temperature Controller circuit is mounted on two printed circuit boards. These boards are located toward the front of the chassis in the left-hand row on the component plate. From front to rear, the circuit boards are:

1) A1 - Temperature Error - 910E314G01

2) A2 - Temperature Controller - 910E315G01

Selected test points are connected to test jacks mounted on the component panel at the top front of the chassis.

The Experimental Temperature Controller is a two stage circuit similar to the Temperature Controller circuit in the Log Power and Temperature Controller Chassis 48A1, but with a different compensation network. The transfer function for the Experimental Temperature Controller is:

$$\frac{\dot{\Theta}_{DD}}{T_D - T_M} = -1.80 \frac{(1+S/.02)\left[1+1.4\,(S/.223)+(S/.223)^2\right]}{(1+S/.0045)\,(1+S/5)^2\,(1+S/62.8)\,(1+S/200)} \quad v/v$$

where $\dot{\Theta}_{DD}$ is the control drum velocity demand in volts, T_D is the temperature demand signal in volts and T_M is the temperature measured signal in volts. The scaling is: $\dot{\Theta}_{DD}$ = 5 degrees per second per volt; T_D = 450°R per volt and T_M = 450°R per volt. A third input is provided for signals from the Frequency Analyzer where 15 vp-p signals are provided. These signals are divided to provide a signal equivalent to 100°R p-p.

The $T_D(+)$ and $T_M(-)$ signals are buffered signals from the Log Power and Temperature Controller Chassis 48A1 and the Frequency Analyzer signal is obtained from the Frequency Analyzer 01RA2 through the Printout Switching Chassis 01RA3. The output from

the Experimental Controller circuit, $\dot{\Theta}_{DD'}$ is applied to the Log Power and Temperature Controller integrator circuit through relay contacts.

Relays A2K1 and A2K2 provide the switching necessary to short the long time constant networks when the circuit is not in used. The DC gain of the circuits under these conditions is 0.415 volt/volt. The shorts are removed and the output of the Experimental Controller circuit is connected to the Log Power and Temperature Controller Chassis when temperature control and experimental control are selected at the console.

3.2 OPERATION

After the chassis has been installed and tested in accordance with the applicable sections of the Test Specification and Procedure, no further adjustments are required.

3.3 MAINTENANCE

3.3.1 Preventive Maintenance

The equipment is designed so that no special maintenance procedures are required other than the normal good housekeeping rules used for similar type electronic equipment.

3.3.3 Corrective Maintenance

Major corrective maintenance is performed at the factory or by a Westinghouse field representative. Alignment and replacement of obviously faulty components may be performed locally by a skilled technician. There are no specially selected or matched components used, therefore, components may be replaced by locally available parts of identical value and tolerance.

If there is any apparent or suspected failure or improper functioning of the equipment, the equipment should be checked-out in accordance with the Test Specification and Procedure.

3.4 TEST SPECIFICATIONS AND PROCEDURES

3.4.1 Chassis Tests

T-711889 - XE-1 Experimental Controller No. 1 (ETS-1)

T-711889-5 - Functional Tests for Temperature Controller Circuit

3.4.2 Printed Circuit Board Tests

T-711889-3 - Temperature Controller (910E315G01)

T-711889-4 - Temperature Error Amplifier (910E314G01)

3.5 DRAWING LIST

938J912 - Experimental Controller No. 1

938J913 - Schematic Diagram-Experimental Controller No. 1

938J914 - Wiring Diagram-Experimental Controller No. 1

910E314 - Temperature Error Amplifier

910E315 - Temperature Controller

979D442 - Fuseholder, Driven Indicator

3.6 PHOTOGRAPHS

Figure 1 - Experimental Controller No. 1

Figure 2 - Temperature Error Amplifier

Figure 3 - Temperature Controller

4. DRUM OVERRIDE

4.1 GENERAL

This section contains the general description, theory of operation, alignment procedures, maintenance and repair data for the Drum Override equipment.

4.1.1 Description

The Drum Override equipment in the Experimental Controller No. 1 Chassis is comprised of four plug-in printed circuit modules as listed below:

(1) A3 - Rate Limited Tracking Amplifier

(2) A4 - Comparator/Relay Driver/Buffer

(3) A5 - Relay Module

(4) A6 - Relay Module

(5) A7 - Buffer Amplifier

The component parts for the modules are mounted on printed circuit boards measuring 4.5 inches wide and 4.7 inches high. The 35 pin connector on each board mates with a 35 pin socket in the Experimental Controller No. 1 Chassis. Location of the modules in the Experimental Controller is shown in the photograph of Figure 1 and also on the Assembly Drawing 938J912.

4.1.2 Functional Design Specifications

The Drum Override has been designed to conform to the following electrical and functional specifications.

4.1.2.1 The Buffered Drums Demand is a zero to +10 volt buffered signal from the Power and Temperature Controller Chassis (R48).

4.1.2.2 The Manual Drums Position Demand is a 0 to +10V signal.

4.1.2.3 The Drums Override Threshold Set is a 0 to -10V signal with scaling to engine units of 2°/volt.

4.1.2.4 Reactor Auto Start Exponential Setpoint is a 3.34V to 6.67 volt signal scaled to 18°/volt.

4.1.2.5 Drum Override Active/Bypass 0 VDC input gives active condition, and +28VDC gives bypass condition.

4.1.2.6 Drum Override Reset. A +28V signal resets the override.

4.1.2.7 Engine Reset. A +28V signal resets the rate clamp.

4.1.2.8 Manual Drums Position Demand - Positive 0 -10VDC signal scaled to 18°/volt in engine units.

4.1.2.9 Tracking Circuit Time Constant - 0.1 seconds in Startup Mode and 2 seconds in Startup Completed Mode.

4.1.2.10 Rate limited max. velocity is defined by the rate clamp setpoint and is adjustable over the range $.5 < \dot{\Theta}_{set} < 3^{\circ}/\text{sec.} \pm 0.1^{\circ}/\text{sec.}$ in engine units.

4.1.2.11 Drums Demand Θ_T Rate Scaling is 3 volts/degree/sec.

4.1.2.12 Outputs

(a) Drums Override Position Demand. Signal range from -10 to 0 volts and is the sign inverted Manual Drums Position Demand with scaling of 18°/volt.

(b) Manual Drums Follow-Up Demand. Signal ranges from 0 to +10 volts, and is the output of the rate-limited tracking circuit.

(c) Drums Error Meter. Buffered BUFFERED DRUMS DEMAND Signal 0 to +10V.

(d) Drums Override Normal/Operate. In OPERATE position switch turns on to apply -15 volts to normal/operate relay on Power and Temperature Controller Chassis.

(e) Drums Override Operate Latch. Provides latching action for normal/operate relay using a contact closure on the normal/operate relay.

(f) Drums Override Active Indicate. Provides +28 VDC signal to the operate status indicator. The signal defines the simultaneous de-energized condition of the Drums Override Active/Bypass relay and energized condition of the Rate Clamp Activate relay.

(g) Drums Override Bypass Indicate. Provides +28 VDC signal to the bypass indicator. The signal defines the energized condition of the Drums Override Active/Bypass relay.

4.2 INSTALLATION OF OVERRIDE

4.2.1 Incoming Inspection

The equipment was carefully inspected both mechanically and electrically before shipment. It should be physically free of mars, dents, or scratches and should be in perfect electrical order upon receipt. To confirm this, the equipment should be inspected for physical demage from transit and tested for electrical performance using the procedures of Section 5. If there is damage or deficiency, repairs should be made before final use.

4.2.2 Mounting

CAUTION: *Before installation of the circuit boards make sure all power and* signals to the chassis are turned off to prevent possible damage to the equipment or injury to personnel.

The circuit board (Module A3) is to be mounted in the front of the chassis as shown on Drawing 938J912. Circuit Boards A4, A5, A6, and A7 are located adjacent to the rear of A3.

4.2.3 Power Requirements

Power is obtained from external sources brought into the chassis and enters the unit through the 35-pin connector at the bottom of the board. The following are the nominal voltage and current requirements:

(a) +15VDC (to I & C Common) at .02 amp

(b) -15VDC (to I & C Common) at .02 amp

(c) -10VDC (to I & C Common) at .02 amp

4.3 THEORY OF OPERATION

The following description is with reference to Schematic Drawing 938J913.

The Drum Override consists of a rate limited tracker and threshold comparator. The rate limited tracker follows the control drum position demand with the constraint that the rate of change of the tracking signal cannot exceed a preset positive rate. The rate limit is adjustable locally from 0.5 to 3.0 deg/sec (nominally set for 1.25 deg/sec). The difference between the demand control drum position and the tracked drum position demand is compared to a preset setpoint in an error detecting circuit. If the demanded control drum position exceeds the tracked position demand by the setpoint, the drum demand is switched

from the output of the power and temperature controller chassis to the control drum position demand pot. The setpoint is adjustable from 0 to 20 degrees. (Nominally set at 8.5 degrees.) The output of the tracker also drives the control drum position demand pot followup. The detailed circuit description follows.

4.3.1 Rate Limited Tracking Amplifier

The Rate Limited Tracking Amplifier is comprised of two amplifiers, A1 (a linear amplifier), the other in cascade, A2 (an integrating amplifier). By means of negative feedback to the + summing junction of Amplifier A1, a unity gain output from Amplifier A2 is obtained. Also, because Amplifier A2 is an integrator, the output of Amplifier A1 is proportional to the velocity or differentiated tracking signal, Θ_T. The transfer function from the input, Θ_D, to output, Θ_T, is given by, for startup mode,

$$\frac{\Theta_T(S)}{\Theta_D(S)} = \frac{1}{1+RCS} = \frac{1}{1+0.1S}$$

where RC is Module A3A2 reciprocal gain in the startup mode; and for startup completed mode,

$$\frac{\Theta_T(S)}{\Theta_D(S)} = \frac{1}{1+RCS} = \frac{1}{1+2S}$$

where RC is Module A3A2 reciprocal gain in the startup completed mode.

The output of Amplifier A2 is limited to 8.9 volts or 160° in engine units by means of Diode CR1 and adjustment pot R11. Zener Diode CR2 provides low impedance coupling to the amplifier output to enhance the clamping action.

The output of Amplifier A1, $\dot{\Theta}_T$, is related to the input, Θ_D, by the transfer function, for startup mode

$$\left(\frac{\dot{\Theta}_T(S)}{\Theta_D(S)}\right)_{SM} = \frac{-RCS}{1+RCS} = \frac{-25.5S}{1+0.1S}$$

and for startup completed mode

$$\left(\frac{\dot{\Theta}_T(S)}{\Theta_D(S)}\right)_{SM} = \frac{-RCS}{1+RCS} = \frac{-52.1S}{1+2S}$$

The full scale output of -10 volts corresponds to a tracker velocity of 71°/second in engine units, in the startup mode. In the startup completed mode the maximum positive velocity is set by the diode clamp, CR3, and pot R1 on the component panel, which provides for a clamp setpoint variable from 0.5 to 3°/sec (engine units) corresponding to output voltage range from 1.5 to 8.7 volts. The change in gain is accomplished by switching relay contacts A5K1A across resistors R5, R6, and R7.

4.3.2 Comparator/Relay Driver/Buffer

4.3.2.1 General

This card is comprised of two comparator amplifier, A1 and A2; two relay driver transistors, Q1 and Q2; and an inverting amplifier, A3.

4.3.2.2 Comparator Amplifier A1

The output of Amplifier A1 will be about 0.5 volts more positive than the AUTO STARTUP EXPONENTIAL SET input when the BUFFERED DRUMS DEMAND, Θ_D, is smaller, because Diode CR1 will be in forward conduction. When the Θ_D input is

larger, Diode CR1 operates in its Zener region with a drop of about 13 volts across it. The amplifier output voltage will be negative by the difference between the 13 volt Zener voltage and the positive input voltage to the + input point, which may be from 3.3 volts to 6.7 volts. Diode CR1 thus enables Amplifier A1 to operate between two stable states, with the amplifier operating in its active region at all times. This assures the speed of response of the comparator circuit. Input resistors R2 and R3 provide isolation between the inputs and the amplifier.

4.3.2.3 Relay Driver Q1. Transistor Q1 provides a switching action, to energize RATE CLAMP ACTIVATE relay A5K1 when the output of Comparator A1 goes negative. Resistor R4 provides base current drive to Transistor Q1 to hold the Collector-Emitter voltage saturated. Diode CR2 limits the base to emitter voltage on Transistor Q1 to a safe value when the comparator output voltage is positive.

4.3.2.4 Comparator Amplifier A2. The output of the Tracking Amplifier, Θ_T, is compared differentially with the BUFFERED DRUMS DEMAND, Θ_D, at the plus and minus inputs, respectively, of Comparator Amplifier A2.

The DRUMS OVERRIDE THRESHOLD SET POINT is combined with the Θ_D input signal in the resistor network comprised of resistors R5, R7, and R10. Up to 1.11 volts, or 20° in engine units, can be subtracted from the Θ_D signal at the comparator amplifier minus input. The set point is adjustable at the Setup Panel 01-L. When the combined signal exceeds (larger positive voltage) the Tracking Amplifier output, Θ_T, the output of Amplifier A2 will switch from a positive voltage output corresponding to Normal Mode, to a negative output voltage corresponding to Operate Mode. In the Normal Mode the output of Amplifier A2 is determined by the forward voltage drop across Diode CR3 plus

the voltage at the Amplifier A2 + input. The + input voltage is the Tracking Amplifier output, Θ_T, reduced by the voltage divider comprised of Resistors R6 and R9. In the Operate Mode the output of Amplifier A2 is a negative voltage equal to the difference between the zener voltage of Diode CR3 and the voltage at the + input.

4.3.2.5 Relay Driver Q2. Transistor Q2 provides a switching action to energize the DRUMS OVERRIDE NORMAL/OPERATE relay connected to Pins J2S and J2P from the Power/Temperature Controller Chassis. Energization occurs when the output of Amplifier A2 switches to negative output voltage. Resistor R11 provides base current to drive Transistor Q2 to hold the collector emitter voltage saturated.

4.3.2.6 Buffer Amplifier A2. Input signal to the Buffer Amplifier A3 is the MANUAL DRUMS POSITION DEMAND which is inverted to supply an output DRUMS OVERRIDE POSITION DEMAND signal of negative polarity.

4.3.3 Relay Module A5

4.3.3.1 General

This Module provides two 4PDT relays; one with a 15VDC coil, K1, and the other with a 28VDC coil, K2. Each coil is shunted by a silicon diode to prevent large voltage transients across the coil on de-energization.

4.3.3.2 Rate Clamp Activate Relay K1

Coil of Relay K1 is energized when Transistor Q1 switches into conduction. The closure of the NO (Normally Open) contact K1A couples the output of amplifier A1 on Module A3 to the rate limit clamp Diode A3CR3 through Resistor A3R4, thus limiting the voltage applied to Integrator A3A2 to the value of the SET POINT

on Diode A3CR3. The opening of NC (Normally Closed) contact K1B adds Resistors A3R6, and A3R7 in series with Amplifier A3A2 input. The closure of NO contact K1B locks up Relay K1 so that it remains energized until reset by opening of Contacts A6K2A. Closure of NO Contact K1C provides a +28VDC DRUMS OVERRIDE ACTIVE INDICATE output signal at Connector Pin J2-M.

4.3.3.3 Drums Override Active/Bypass Relay K2

The coil of Relay K2 is energized by +28VDC input to Connector Pin J2-DD, DRUMS OVERRIDE ACTIVE/BYPASS. Operation of NC Contact A5K2A prevents operation of Rate Clamp Activate relay by interrupting the -15V supply voltage. The closure pf MP Cpmtact K2B provides a +28V DRUMS OVERRIDE ACTIVE INDICATE output signal at Pin J2-N.

4.3.4 Relay Module A6

4.3.4.1 General

This module provides two 4PDT relays; both have 28VDC coils. Each coil is shunted by a silicon diode to prevent large transients across the coil on de-energization.

4.3.4.2 Drums Override Reset Relay, K1

The coil of Relay K1 is energized when a +28VDC DRUMS OVERRIDE RESET signal is received at Connector Pin J2-HH. Operation of NC Contact K1A de-energizes the DRUMS OVERRIDE NORMAL/OPERATE relay returning the Drums Override to Normal condition.

4.3.4.3 Engine Reset Relay, K2

Relay coil K2 is energized by a +28VDC ENGINE RESET input signal at Connector Pin J2-U. Operation of NC Contact K2A de-energizes the RATE CLAMP ACTIVATE relay.

4.4 OPERATION

4.4.1 General

After installing the Drum Overrides Modules in the Experimental Controller No. 1 Chassis, a mechanical and electrical checkout should be made. Controls, adjustments, and operational test procedures follow here.

4.4.2 Overrides Controls - Operational and Semi-Permanent

Amplifier zero alignment controls and other special circuit alignment controls are located on the individual overrides modules. One control, RATE CLAMP ADJUST, is located on the right rear of the Component Panel of the Experimental Controller No. 1.

4.4.3 Test Points

Voltages representing functional quantities involving inputs, outputs and system setpoints can be measured at test points located on the left side of the Component Panel of the Experimental Controller No. 1 Chassis. These are designated as follows:

TP13	RATE CLAMP
TP14	Θ_D (+)
TP15	Θ_D RATE
TP16	Θ_T (+)
TP17	OVRD SET PT
TP18	EXPON SET

TP19 MAN DEMAND

TP20 OVRD DEMAND

Additional test points for local measurements are located on the modules.

4.4.4 Operational Checkout

4.4.4.1 Test Equipment Needed

(1) Ohmmeter, Model 269 or equal

(2) Digital Voltmeter, Hewlett-Packard 3440A or equal

(3) Jumpers and Test Leads

4.4.4.2 Mechanical Checkout

Before application of power for the electrical checkout, examine gear carefully for mechanical rigidity of all mounted components, connectors, test points, knobs, and like.

4.4.4.3 Electrical Checkout

Turn on power and allow equipment to warmup for at least 30 minutes. Checkout in accordance with Experimental Controller No. 1 Checkout Procedure (see Appendix A).

4.4.5 Alignment Procedures

Place the module to be aligned on the extender board where necessary to reach pots adjusted from side.

4.4.5.1 Rate Limited Tracking Amplifier, A3, Alignment

Adjust Amplifier A1 offset to zero. Jumper Test Points TP3 to TP1, and TP8 to TP1 on A3. Adjust the voltage offset pot for minimum output ($<$ 1mv.) at

Test Point A3TP6.

Adjust Amplifier A2 offset to zero. Remove jumper between Test Points A3TP8 and A3TP1. Jumper A3TP5 to A3TP8 and A3TP4 to A5TP1. Adjust offset pot on Amplifier A2 for minimum output (<10mv.) at Test Point A3TP8. Remove jumpers and test leads and replace Module A5.

4.4.5.2 Comparator/Relay Driver/Buffer A4 Alignment

Adjust Amplifier A1 offset to zero. Jumper Test Points A4TP2 to A4TP3 and A4TP7 to A4TP1 and adjust the voltage offset for minimum output (< 1mv.) at Test Point A4TP3. Remove jumper.

Adjust Amplifier A2 offset to zero. Jumper Test Point A4TP6 to A4TP1 and A4TP2 to A4TP5 and adjust the voltage offset for minimum output (< 1mv.) at Test Point A4TP5. Remove jumper.

Adjust Amplifier A3 offset to zero. Jumper Test Point A4TP9 to A4TP1. Adjust the voltage offset for minimum output (< 1mv.) at Test Point A4TP8. Remove jumper.

Set Rate Clamp Adjust pot on component panel to desired setting.

The Drum Override is ready for use after above adjustments have been completed. Remove meter test leads from test jacks and close the drawer.

4.5 MAINTENANCE

4.5.1 Preventive Maintenance

The equipment is designed so that no special maintenance procedures are required other than the normal good housekeeping rules used for similar type electronic equipment.

4.5.2 Corrective Maintenance

Major corrective maintenance is performed at the factory or by a Westinghouse field representative. Alignment and replacement of obviously faulty components may be performed locally by a skilled technician. There are no specially selected or matched components used, therefore, components may be replaced by locally available parts of identical value and tolerance.

If there is any apparent or suspected failure or improper functioning of the equipment, the equipment should be checked-out in accordance with the Test Specification and Procedure.

4.6 TEST SPECIFICATION AND PROCEDURE

The proper Test Specification and Procedure is as follows:

4.6.1 Chassis Test

T-711889-6 Experimental Controller No. 1 - ETS-1, Drum Override Functional Tests

4.6.2 Printed Circuit Card Tests

T-711889-1 Comparator/Relay Driver/Buffer (910E312G01)

T-711888-2 Rate Limited Tracking Amplifier (910E313G01B)

T-711883-4 Standard Buffer Amplifier (910E318G02)

T-711883-5 Relay Module (979D576G01 & G02)

4.7 DRAWING LIST

938J912 - Experimental Controller No. 1

938J913 - Schematic Diagram-Experimental Controller No. 1

910E312 - Comparator/Relay Driver/Buffer

910E313 - Rate Limited Tracking Amplifier

910E318 - Standard Buffer Amplifier

979D576 - Relay Module, 4PDT

979D575 - Schematic Diagram, Relay Module 4PDT

980D916 - Standard Operational Amplifier

980D922 - Operational Amplifier

4.8 PHOTOGRAPH LIST

Figure 4 - Comparator/Relay Driver/Buffer

Figure 5 - Rate Limited Tracking Amplifier

Figure 6 - Buffer Amplifier

Figure 7 - Relay Module

EXPERIMENTAL CONTROLLER NO. 1 CHECKOUT PROCEDURE

1.0 SCOPE

This document contains the requirements to functionally checkout the modification to the nuclear subsystem control system for the addition of the first experimental controller chassis (WANL Drawing 938J912, schematic diagram WANL Drawing 938J913) which contains the drum override and the low range state programmed temperature controller.

The first experimental controller chassis has been checked at the chassis level at WANL.

These functional tests are designed to be performed at the system level.

2.0 APPLICABLE DOCUMENTS

2.1 WANL Drawing 938J912 - Experimental Controller No. 1

2.2 WANL Drawing 938J913 - Schematic Diagram - Experimental Controller No. 1.

3.0 EXPERIMENTAL CONTROLLER NO. 1

The Experimental Controller No. 1 contains two functions; the low range state programmed temperature controller and the drum override.

The low range state programmed temperature controller is that portion of the state programmed temperature controller which is designed to operate between 60 and 150 psia chamber pressure. The full state programmed temperature controller will be contained in Experimental Controller No. 2.

The drum override consists of a rate limited tracker and threshold comparator. The rate limited tracker follows the control drum position demand with the constraint that the rate of change of the tracking signal cannot exceed a preset positive rate. The rate limit is adjustable locally from 0.5 to 3.0 deg/sec (nominally set for 1.25 deg/sec). The difference between the demand control drum position and the tracked

drum position demand is compared to a preset setpoint in an error detecting circuit. If the demanded control drum position exceeds the tracked position demand by the setpoint, the drum demand is switched from the output of the power and temperature controller chassis to the control drum position demand pot. The setpoint is adjustable from 0 to 20 degrees. (Nominally set at 8.5 degrees.) The output of the tracker also drives the control drum position demand pot followup.

4.0 FUNCTIONAL TEST

4.1 Low Range State Programmed Temperature Controller

The low range SPTC is checked by placing the system in simulate and ramping the temperature demand. The temperature demand is then stepped from the frequency analyzer.

4.1.1 Place the control system in the simulate mode and establish T_c = 1100°R and P_c = 60 psia in normal temperature and pressure control.
Verify normal temperature control indication is "ON" _____
Verify experimental temperature control indication is "OFF" _____

4.1.2 Switch to experimental temperature control.
Verify experimental temperature control indication is "ON" _____
Verify normal temperature control indication is "OFF" _____

4.1.3 Ramp to T_c = 2000°R and P_c = 150 psia along normal operating line and allow system to reach steady state condition.

4.1.4 Step temperature demand 100°R from frequency analyzing equipment.

4.2 Drum Override

The function tests on the drum override calibrate the "Drums Override Threshold Setpoint" potentiometer. A drum roll out is then simulated to check the operation of the circuit.

4.2.1 Set the "Rate Clamp Adjust" pot, R1, in the experimental controller No. 1 chassis for a voltage of 0.177 VDC (1.25°/sec) at TP13.

4.2.2 Calibrate the "Drums Override Threshold Setpoint" pot in the following manner:

a) Place pot at the "0" position.

b) Remove card A3.

c) Apply voltage specified in column (2) of Table 1 to TP14.

d) Increase pot until drum override "operate" indication occurs.

e) Record pot divisions in Table 1.

f) Repeat to verify pot setting.

g) Complete Table 1 in above manner

h) Replace card A3

i) Plot curve of degrees versus pot setting.

TABLE 1

DRUMS OVERRIDE THRESHOLD SETPOINT POT CALIBRATION

(1) TRACK ERROR (DEGREES)	(2) VOLTAGE AT TP 14 (VDC)	(3) POT DIV
0	0.000	
1.0	0.055	
2.0	0.111	
3.0	0.167	
4.0	0.222	
5.0	0.278	
6.0	0.333	
7.0	0.389	
8.0	0.444	
9.0	0.500	

TABLE 1 (Cont.)

(1) TRACK ERROR (DEGREES)	(2) VOLTAGE AT TP 14 (VDC)	(3) POT DIV
10.0	0.555	
11.0	0.611	
12.0	0.667	
13.0	0.722	
14.0	0.778	
15.0	0.834	
16.0	0.890	
17.0	0.945	
18.0	1.000	
19.0	1.055	
20.0	1.111	

4.2.3 *Place control system in simulate with reactor shutdown.*

4.2.4 Reset drum override

Verify drum override active indication is "OFF" _____

Verify drum override bypass indication is "OFF" _____

4.2.5 Perform power auto-start to 400 watts

Verify drum override active indication is "ON" _____

4.2.6 Establish $T_c = 1100^{\circ}R$ and $P_c = 60$ psia.

4.2.7 Switch to experimental temperature control.

4.2.8 Activate reduced gain temperature control.

4.2.9 Set "Drums Override Threshold Setpoint" for 1 degree.

4.2.10 Step drums +2 degrees.

Verify drum override "operate" indication is "ON" _____

4.2.11 Remove drum step

4.2.12 Verify drums error meter on CTE console is zero _____

4.2.13 Reset Drum override

Verify drum override "operate" indication is "OFF". _____

Verify drum override "normal" indication is "ON". _____

4.2.14 Scram the system.

Verify drum override "active" indication is "OFF". _____

Verify drum override "bypass" indication is "OFF". _____

4.2.15 Bypass the drum override

Verify the drum override "active" indication is "OFF" _____

Verify the drum override "bypass" indication is "ON" _____

Astronuclear Laboratory
WANL-TME-1704

T-711889

ACCEPTANCE TEST SPECIFICATION AND PROCEDURE

XE-1 Experimental Controller No. 1 ETS-1

938J912G01

DATE: September, 1967

PREPARED BY:

K. Berthelsen 9/7/67

Circuits Design Date
Equipment Design

APPROVED BY:

R A Flemings 9/7/67

Supervisor, Circuits Design Date
Equipment Design

E J M. Jeaide 10-11-67

Quality Engineering Date

C. C. Murdock 10/4/67

Control Systems Engineering Date

INFORMATION CATEGORY

Unclassified

R. A. Flemings 9/9/67

Authorized Classifier Date

T-711889
ACCEPTANCE TEST SPECIFICATION AND PROCEDURE
XE-1 Experimental Controller No. 1 ETS-1
938J912G01

1. SCOPE

This document contains the requirements for the acceptance testing of the XE-1 Experimental Controller No. 1 Chassis.

2. REQUIREMENTS

2.1 The acceptance test shall consist of a Visual Examination (to be performed by Quality Control) and a Functional Test (to be performed by Electronics and Instrumentation and witnessed by Quality Control).

2.2 The acceptance test shall be performed in the order of and as specified in the procedure. Discrepancies found during the visual examination shall be corrected and reinspected before performing the functional test. Failure or inability to obtain a required measurement during formal functional testing shall result in establishing a "hold" on the test. The failure or inadequacy shall be recorded by Quality Control and shall be reviewed by the WANL Engineering Review Board (ERB). The equipment shall be repaired and sections of the test repeated as determined by the ERB. Visual examination shall be performed on the reworked or repaired areas before resuming testing.

T-711889

3. APPLICABLE DOCUMENTS

3.1 Drawing 938J912 - Experimental Controller No. 1

3.2 Drawing 938J913 - Schematic Diagram, Experimental Controller No. 1

3.3 Drawing 938J914 - Wiring Diagram, Experimental Controller No. 1

4. EQUIPMENT REQUIRED

4.1 +15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.2 -15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.3 0 to +10 VDC signal source with .01% resolution and 1 mv. max. ripple

4.4 0 to -10 VDC signal source with .01% resolution and 1 mv. max. ripple

4.5 +28±1VDC source with ±1% regulation and 1 volt max. ripple

4.6 Model 269 Simpson Ohmmeter or equal

4.7 Digital Voltmeter H-P 3440A or equal

4.8 Set of equipment to measure frequency response and phase shift between .001 cps and 50 cps. (Weston-Boonshaft and Fuchs DA410 or equal)

T-711889

5. VISUAL EXAMINATION

The equipment under test shall be presented in its final form together with the applicable schematic and assembly drawing. The visual examination shall consist of the following parts:

5.1 WORKMANSHIP, ASSEMBLY, AND FIT

The inspector shall inspect the equipment for workmanship to WANL requirements, and to assure that the overall board is of the proper dimensions per the assembly drawing.

Westinghouse Drawing Number_____Rev. _____

Workmanship OK _____

5.2 MATERIALS, PARTS, AND FINISHES

The equipment shall be inspected to assure that the materials, parts, and finishes are in accordance with the applicable assembly drawings. Incoming inspection records on materials, parts, and finishes shall be utilized to determine conformance to the assembly drawings where possible.

Materials OK _____

5.3 MARKING

The markings on the equipment shall be inspected to ensure conformance to the applicable drawings and to assure that they are acceptable as to permanence and readibility.

Marking OK _____

T-711889

6. FUNCTIONAL TESTS

The Temperature Controller and NSS Drum Override Circuits are separate circuits which operate independent of each other and, therefore, are approved and tested separately.

6.1 TEMPERATURE CONTROLLER - USE T-711889-5

6.2 NSS DRUM OVERRIDES - USE T-711889-6

Astronuclear Laboratory

WANL-TME-1704

T-711889-1

ACCEPTANCE TEST SPECIFICATION AND PROCEDURE

Experimental Controller No. 1

Comparator/Relay Driver/Buffer

910E312G01

DATE: September, 1967

PREPARED BY: N. E. Brush 9/20/67

Circuits Design Date
Equipment Design

APPROVED BY: R. A. Flanigan 9/20/67

Supervisor, Circuits Design Date
Equipment Design

E. J. McDonald 9-26-67

Quality Engineering Date

C. C. Merchant 9/27/67

Control Systems Engineering Date

INFORMATION CATEGORY

Unclassified

R. A. Flanigan 9/20/67

Authorized Classifier Date

T-711889-1
ACCEPTANCE TEST SPECIFICATION AND PROCEDURE
Experimental Controller No. 1
Comparator/Relay Driver/Buffer
910E312G01

1. SCOPE

This document contains the requirements for the acceptance testing of the Comparator/Relay Driver/Buffer Board prior to incorporating the board into the Experimental Controller No. 1 Chassis 938J912G01.

2. REQUIREMENTS

2.1 The acceptance test shall consist of a Visual Examination (to be performed by Quality Control) and a Functional Test (to be performed by Electronics and Instrumentation and witnessed by Quality Control).

2.2 The acceptance test shall be performed in the order of and as specified in the procedure. Discrepancies found during the visual examination shall be corrected and reinspected before performing the functional test. Failure or inability to obtain a required measurement during formal functional testing shall result in establishing a "hold" on the test. The failure or inadequacy shall be recorded by Quality Control and shall be reviewed by the WANL Engineering Review Board (ERB). The equipment shall be repaired and sections of the test repeated as determined by the ERB. Visual examination shall be performed on the reworked or repaired areas before resuming testing.

3. APPLICABLE DOCUMENTS

3.1 Drawing 910E312 - Comparator/Relay Driver/Buffer

3.2 Drawing 928F953 - Printed Circuit Board

4. EQUIPMENT REQUIRED

4.1 +15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.2 -15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.3 Positive signal source, variable 0-10 VDC with .01% resolution and 1 mv. max. ripple

4.4 Negative signal source, variable 0-10 VDC with .01% resolution and 1 mv. max. ripple

4.5 Model 269 Simpson Ohmmeter or equal

4.6 Digital Voltmeter H-P 3440A or equal

4.7 Oscilloscope, Tektronix 585 or equal

4.8 Signal Generator H-P 241A or equal

4.9 200 Ohm Resistor, 2 Watt

5. VISUAL EXAMINATION

The equipment under test shall be presented in its final form together with the applicable schematic and assembly drawing. The visual examination shall consist of the following parts:

5.1 WORKMANSHIP, ASSEMBLY, AND FIT

The inspector shall inspect the equipment for workmanship to WANL requirements, and to assure that the overall board is of the proper dimensions per the assembly drawing.

Westinghouse Drawing Number _____ Rev. _____

Workmanship OK _____

5.2 MATERIALS, PARTS, AND FINSIHES

The equipment shall be inspected to assure that the materials, parts, and finishes are in accordance with the application assembly drawings. Incoming inspection records on materials, parts, and finishes shall be utilized to determine conformance to the assembly drawings where possible.

Materials OK _____

5.3 MARKING

The markings on the equipment shall be inspected to ensure conformance to the applicable drawings and to assure that they are acceptable as to permanence and readibility.

Marking OK _____

6. FUNCTIONAL TESTS

6.1 COMPARATOR A1 AND RELAY DRIVER Q1

6.1.1 Alignment

6.1.1.1 Jumper Test Points TP2 to TP3 and TP7 to TP1 and adjust the voltage offset for minimum output ($<$ 1 mv.) at Test Point TP3. Record offset voltage: _____.

Remove all jumpers from test points.

6.1.2 Input Balance Check

6.1.2.1 Apply +3.300 volts to Pin 9. Apply the same polarity voltage to Pin 8 and adjust it to make the output voltage of Test Point TP3 change in negative direction. Measure the voltage at Pin 8. It should be 3.300$\pm$0.1 volts. Record test result.

Voltage at Pin 8: _____ volts.

6.1.2.2 Increase voltage at Pin 8 an amount just sufficient to cause output to reach maximum voltage (where further increase of voltage at Pin 8 does not cause further rapid increase of output at Test Point TP3). Measure and record voltage at Pin 8 and at Test Point TP3. Voltage at Pin 8 should be $3.3\ ^{+0.1}_{-0}$ volts and at TP3(-) 9.1 $\pm$0.7 volts.

Voltage at Pin 8: _____ volts.

Voltage at TP3: _____ volts.

6.1.2.3 Subtract voltage at Pin 8 determined in Steps 6.1.2.2 from that determined in Step 6.1.2.1. The difference should be less than 0.1 volts. Record the test result. Difference voltage at Test Point TP8: _____ volts.

6.1.2.4 Repeat Step 6.1.2.1, except apply voltage at Pin 9 of 6.600 volts. Voltage at Pin 8 should be 6.600$\pm$.100 volts. Record test results. Voltage at Pin 8: _____ volts.

6.1.2.5 Repeat Step 6.1.2.2, except voltage at Pin 9 shall be 6.600 volts. Voltage measured at Pin 8 should be $6.6^{+0.1}_{-0}$ volts and at Test Point TP3 (-) 5.8±0.7 volts.

Voltage at Pin 8: _____ volts.

Voltage at Test Point TP3: _____ volts.

6.1.3 Relay Driver Q1 Test

6.1.3.1 Connect the 200 ohm resistor from Pin 31 to (-) 15 VDC. With voltage at Test Point TP3 as in Step 6.1.2.5 voltage measured at Pin 31 should be less than (-) 0.5 volt. Voltage at Pin 31: _____ volts.

6.1.3.2 Set voltage at Pin 8 to zero. Voltage measured at Pin 31 should be (-) 15 volts. Record test result. Voltage at Pin 31: _____ volts.

6.1.3.3 Measure voltage from base to emitter of Transistor Q1. It should be less than 0.75 volts. Record result. Base-emitter voltage of Q1: _____ volt. Remove test sources, resistor and meters.

6.2 COMPARATOR A2 AND RELAY DRIVER Q2

6.2.1 Alignment

6.2.1.1 Jumper Test Point TP6 to TP1 and TP2 to TP5 and adjust the voltage offset for minimum output ($<$ 1 mv.) at Test Point TP5. Record offset voltage: _____. Remove all jumpers from points.

6.2.2 Input Balance Check

6.2.2.1 Ground Pin 28 and Pin 24. Apply a negative polarity voltage to Pin 8 and adjust it to make the output voltage of Test Point TP5 change in negative direction. Measure the voltage at Pin 8. It should be $<$ -.01 volt. Record test result.

Voltage at Pin 8: _____ volts.

6.2.2.2 Change voltage at Pin 8 in positive direction an amount just sufficient to cause output to reach maximum negative voltage (where further increase of voltage at Pin 8 does not cause further rapid increase of output at Test Point TP5). Measure and record voltage at Pin 8 and at Test Point TP5. Voltage at Pin 8 should be $<$ +.01 volts and at TP5(-) 12.6±0.7 volts.

Voltage at Pin 8: _____ volts.

Voltage at TP5: _____ volts.

6.2.2.3 Subtract voltage at Pin 8 determined in Step 6.2.2.2 from that determined in Step 6.2.2.1. The difference should be less than 0.01 volts. Record the test result. Difference voltage at Test Point TP8: _____ volts.

6.2.2.4 Apply (-) 10.00 volts to Pin 24 and observe that output voltage at Test Point TP5 becomes positive. Increase voltage at Pin 8 an amount just sufficient to cause the output voltage at Test Point TP5 to reach maximum. Measure and record the voltage at Pin 8. It should be 1.111±0.1 volts. Voltage at Pin 8: _____ volts.

6.2.2.5 Ground Pin 24 and apply voltage at Pin 28 of +10.00 volts. Apply positive voltage at Pin 8 until output at TP5 starts negative. Voltage at Pin 8 should be 10.00±.05 volts. Record test results.

Voltage at Pin 8: _____ volts.

6.2.2.6 Repeat Step 6.2.2.2, except voltage at Pin 28 shall be +10.00 volts. Voltage measured at Pin 8 should be $\leq$ 10 mv. more than result in 6.2.2.5 and at Test Point TP5(-) 7.9±0.7 volts.

Voltage at Pin 8: _____ volts.

Voltage at Test Point TP5: _____ volts.

6.2.3 Relay Driver Q2 Test

6.2.3.1 Connect the 200 ohm resistor from Pin 30 to (-) 15 VDC. With voltage at Test Point TP5 as in Step 6.2.2.6 voltage measured at Pin 30 should be less than (-) 0.5 volts.

Voltage at Pin 30: _____ volts.

6.2.3.2 Set voltage at Pin 8 to zero. Voltage measured at Pin 30 should be (-) 15 volts. Record test result voltage at Pin 30: _____ volts.

6.2.3.3 Measure voltage from base to emitter of Transistor Q2 it should be less than 0.75 volts. Record result. Base emitter voltage of Q2: _____ volt.

6.3 BUFFER A3 TEST

6.3.1 Gain and Linearity Check

6.3.1.1 Ground Pin 35.

6.3.1.2 Adjust the voltage offset for minimum output ($<$ 1 mv.) at Pin 33. Record offset voltage: _____.

6.3.1.3 Remove ground from Pin 35. Connect the DC voltage source to Pin 35. Measure gain and linearity by using input signal at Pin 35 and output at Pin 33. Record results.

Input VDC	Output VDC
0	0±.01 _____
+5	-5±.1 _____
+10	-10±.2 _____
-5	+5±.1 _____
-10	+10±.2 _____

6.3.2 Frequency Response Check

6.3.2.1 Disconnect the voltage source from Pin 35 and connect the function generator. Determine the break frequency of the amplifier by using input Pin 35 and output Pin 33. The break frequency (-3 db point) should be greater than 1000 cps. Record the following frequencies:

-1 db _____ KHz

-3 db _____ KHz

-6 db _____ KHz

6.3.3 Output Noise

6.3.3.1 Remove the function generator. Ground Pin 35 and connect the oscilloscope to Pin 33. The observed a-c waveform should be less than ten millivolts peak. Record the value oscilloscope waveform peak at Pin 33: _____ mv. Remove jumpers and test leads.

6.4 RESISTANCE AND CONTINUITY CHECKS

6.4.1 Verify continuity between the following points:

TP1 and Pin 3 _____

TP2 and Pin 8 _____

TP4 and Pin 24 _____

TP8 and Pin 33 _____

TP9 and Pin 35 _____

6.4.2 Remove Module A2. Measure resistance between TP6 and TP1: _____ ohms. Value should be 10K±3%.

6.4.3 Remove Module A1. Measure resistance between TP7 and Pin 9: _____ ohms. Value should be 100K±3%.

T-711889-2

ACCEPTANCE TEST SPECIFICATION AND PROCEDURE

Experimental Controller No. 1

Rate Limited Tracking Amplifier

910E313G01B

DATE: October, 1967

PREPARED BY: W. E. Bush 10/24/67
Circuits Design Date
Equipment Design

APPROVED BY: R A Elmyer 10/24/67
Supervisor, Circuits Design Date
Equipment Design

F. Stella Jr. 10-25-67
Quality Engineering Date

C. C. Merchant 10/30/67
Control Systems Engineering Date

INFORMATION CATEGORY

Unclassified
R G Elmyer 10/24/67
Authorized Classifier Date

T-711889-2
ACCEPTANCE TEST SPECIFICATION AND PROCEDURE
Experimental Controller No. 1
Rate Limited Tracking Amplifier
910E313G01B

1. SCOPE

This document contains the requirements for the acceptance testing of the Comparator/Relay Driver/Buffer Board prior to incorporating the board into the Experimental Controller No. 1 Chassis 938J912G01.

2. REQUIREMENTS

2.1 The acceptance test shall consist of a Visual Examination (to be performed by Quality Control) and a Functional Test (to be performed by Electronics and Instrumentation and witnessed by Quality Control).

2.2 The acceptance test shall be performed in the order of and as specified in the procedure. Discrepancies found during the visual examination shall be corrected and reinspected before performing the functional test. Failure or inability to obtain a required measurement during formal functional testing shall result in establishing a "hold" on the test. The failure or inadequacy shall be recorded by Quality Control and shall be reviewed by the WANL Engineering Review Board (ERB). The equipment shall be repaired and sections of the test repeated as determined by the ERB. Visual examination shall be performed on the re-worked or repaired areas before resuming testing.

3. APPLICABLE DOCUMENTS

3.1 Drawing 910E313 - Comparator/Relay Driver/Buffer

3.2 Drawing 928F954 - Printed Circuit Board

4. EQUIPMENT REQUIRED

4.1 +15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.2 -15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.3 Positive signal source, variable 0-10 VDC with .01% resolution and 1 mv. max. ripple

4.4 Negative signal source, variable 0-10 VDC with .01% resolution and 1 mv. max. ripple

4.5 Model 269 Simpson Ohmmeter or equal

4.6 Digital Voltmeter H-P 3440A or equal

4.7 Oscilloscope, Tektronix 585 or equal

4.8 Ramp Generator, ±0 to 4 volts/sec.

4.9 Test Leads and Jumpers

4.10 X-Y Recorder, H-P 136A or equal

4.11 Recorder, Brush Mark II or equal

T-711889-2

5. VISUAL EXAMINATION

The equipment under test shall be presented in its final form together with the applicable schematic and assembly drawing. The visual examination shall consist of the following parts:

5.1 WORKMANSHIP, ASSEMBLY, AND FIT

The inspector shall inspect the equipment for workmanship to WANL requirements, and to assure that the overall board is of the proper dimensions per the assembly drawing.

Westinghouse Drawing Number _____ Rev. _____

Workmanship OK _____

5.2 MATERIALS, PARTS, AND FINISHES

The equipment shall be inspected to assure that the materials, parts, and finishes are in accordance with the application assembly drawings. Incoming inspection records on materials, parts, and finishes shall be utilized to determine conformance to the assembly drawings where possible.

Materials OK _____

5.3 MARKING

The markings on the equipment shall be inspected to ensure conformance to the applicable drawings and to assure that they are acceptable as to permanence and readibility.

Marking OK _____

T-711889-2

6. FUNCTIONAL TESTS

6.1 Remove Amplifiers A1 and A2. Make the following resistance checks:

From	To	Ohms	Check
Pin 3	TP1	< 1	_____
Pin 5	TP2	< 1	_____
Pin 8	TP3	< 1	_____
Pin 20	TP4	< 1	_____
Pin 22	TP1	< 1	_____
Pin 24	TP5	< 1	_____
Pin 30	Pin 31	< 1	_____
TP4	TP6	90.9K±3%	_____
TP1	TP8	1.013M±3%	_____
TP5	TP7	36.5K±3%	_____

Reinstall Amplifiers A1 and A2.

6.2 ALIGNMENT CHECK

6.2.1 Ground Pin 3 and Pin 8. Connect +15VDC to Pin 1 and -15 VDC to Pin 2.

6.2.2 Amplifier A1

Jumper Test Points TP7 to TP8. Ground TP7 and adjust the voltage offset for minimum output (< 1 mv.) at TP6. Record offset voltage:_____. Verify that offset pot > 1/2 turn from ends:_____.

6.2.3 Amplifier A2

6.2.3.1 Remove ground from TP8, and remove jumper between TP7 and TP8, Jumper TP4 to TP1, and TP5 to TP8. Adjust the voltage offset for minimum output (< 1 mv.)

at TP8. Record offset voltage: _____. Verify that offset pot > 1/2 turn from ends: _____.

6.2.3.2 Apply +10VDC to Pin 8 and adjust pot R11 to give +8.9 volts output at TP8. Record result: _____. Verify that pot R11 > 1/2 turn from ends: _____.

6.3 GAIN AND LINEARITY CHECK

6.3.1 Remove ground from Pin 8; remove jumpers from TP4 to TP1, and TP5 to TP8.

Measure gain and linearity by using input at Pin 8 and output at TP8. Record results.

Input VDC	Output VDC
0	0±.01 _____
+2.0	+2.0±.05 _____
+4.0	+4.0±.10 _____
+6.0	+6.0±.13 _____
+8.0	+8.0±.17 _____

6.4 TIME CONSTANT CHECK

6.4.1 Remove 10VDC input from Pin 8. Measure time constant by using input at Pin 8 and output at TP8, using the Oscilloscope.

6.4.2 Startup Completed Mode

6.4.2.1 Apply a positive step voltage of 0.5VDC to Pin 8. Exponential rise of output voltage at TP8 should have a time constant (time to reach 63.2% point) of 2.1±.4 seconds. Record time constant: _____ sec

6.4.3 Startup Mode

6.4.3.1 Jumper TP4 to TP5. Apply a positive step voltage of 0.5VDC to Pin 8. Exponential rise of output voltage at TP8 should have a time constant (63.2% point) of 0.1±.015 seconds. Record time constant: _____sec.

6.5 AVAILABLE TRACK VELOCITY CHECK

6.5.1 Startup Mode

6.5.1.1 Leave jumper connected from TP4 to TP5. Measure available track velocity by using input at Pin 8 and output at TP6.

6.5.1.2 Connect the Ramp Generator to Pin 8 and adjust it to +3.9v/sec. Measure the output on the Recorder. It should be -9.9±.2v. Record result: _____.

6.5.1.3 Adjust the Ramp Generator to -3.9v/sec and apply it to Pin 8. Measure the output on the Recorder. It should be +9.9±.2v. Record result:_____.

6.5.2 Startup Completed Mode

6.5.2.1 Remove jumper from TP4 to TP5. Set Ramp Generator output to -1/6v/sec, and apply it to Pin 8. Measure the output at TP6 on the Digital Voltmeter. It should be +8.9±.2 volts. Record result:_____.

6.5.2.2 Set Ramp Generator output to +1/6v/sec and apply it to Pin 8. Measure the output at TP6 on the Digital Voltmeter. It should be -8.9±.2 volts. Record result:_____.

6.6 RATE CLAMP CHECK

6.6.1 Ground Pin 5. Jumper Pin 4 to Pin 20. Apply a +10V step to Pin 8. Measure voltage at Pin 20 on Digital Voltmeter and rate of change (slope) at TP8 on the X-Y recorder. Record results.

Voltage at Pin 20 should be between 0 to -1VDC:_____

Slope at TP8 should be $<$ 19mv/sec:_____

6.6.2 Remove ground from Pin 5. Apply -10VDC to Pin 5. Apply a +10V step to Pin 8. Measure as in 6.6.1, above, and record results.

Voltage at Pin 20 should be from -10VDC to -11VDC_____

Slope at TP8 should be $>$ .19V/sec:_____

6.6.3 Apply voltage to Pin 5 and adjust it to make voltage at TP4 read -3.73 volts when step voltage of +5 volts is applied to Pin 8. Measure voltage at Pin 5. Voltage at Pin 5. should be -3.2$\pm$.2V:_____. Measure output rate of change at TP8. It should be 69$\pm$3mv/sec:_____.

Astronuclear Laboratory

WANL-TME-1704

T-711889-3

ACCEPTANCE TEST SPECIFICATION AND PROCEDURE

Experimental Controller No. 1

Temperature Controller

910E315G01

DATE: August, 1967

PREPARED BY:

Circuits Design Date
Equipment Design

APPROVED BY:

Supervisor, Circuits Design Date
Equipment Design

Quality Engineering Date

Control Systems Engineering Date

INFORMATION CATEGORY

Unclassified

Authorized Classifier Date

T-711889-3
ACCEPTANCE TEST SPECIFICATION AND PROCEDURE
Experimental Controller No. 1
Temperature Controller
910E315G01

1. SCOPE

This document contains the requirements for the acceptance testing of the Temperature Controller PCB prior to incorporating the board into the Experimental Controller Chassis.

2. REQUIREMENTS

2.1 The acceptance test shall consist of a Visual Examination (to be performed by Quality Control) and a Functional Test (to be performed by Electronics and Instrumentation and witnessed by Quality Control).

2.2 The acceptance test shall be performed in the order of and as specified in the procedure. Discrepancies found during the visual examination shall be corrected and reinspected before performing the functional test. Failure or inability to obtain a required measurement during formal functional testing shall result in establishing a "hold" on the test. The failure or inadequacy shall be recorded by Quality Control and shall be reviewed by the WANL Engineering Review Board (ERB). The equipment shall be repaired and sections of the test repeated as determined by the ERB. Visual examination shall be performed on the reworked or repaired areas before resuming testing.

T-711889-3

3. APPLICABLE DOCUMENTS

3.1 Drawing 910E315 - Temperature Controller

3.2 Drawing 928F978 - Printed Circuit Board

3.3 Drawing 947C087 - Schematic, Amplifier

4. EQUIPMENT REQUIRED

4.1 +15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.2 -15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.3 0 to +10 VDC signal source with .01% resolution and 1 mv. max. ripple

4.4 0 to -10 VDC signal source with .01% resolution and 1 mv. max. ripple

4.5 Model 269 Simpson Ohmmeter or equal

4.6 Digital Voltmeter H-P 3440A or equal

4.7 Set of equipment to measure frequency response and phase shift between .001 cps and 50 cps. (Weston-Boonshaft and Fuchs DA410 or equal)

T-711889-3

5. VISUAL EXAMINATION

The equipment under test shall be presented in its final form together with the applicable schematic and assembly drawing. The visual examination shall consist of the following parts:

5.1 WORKMANSHIP, ASSEMBLY, AND FIT

The inspector shall inspect the equipment for workmanship to WANL requirements, and to assure that the overall board is of the proper dimensions per the assembly drawing.

Westinghouse Drawing Number _____ Rev. _____

Workmanship OK _____

5.2 MATERIALS, PARTS, AND FINISHES

The equipment shall be inspected to assure that the materials, parts, and finishes are in accordance with the applicable assembly drawings. Incoming inspection records on materials, parts, and finishes shall be utilized to determine conformance to the assembly drawings where possible.

Materials OK _____

5.3 MARKING

The markings on the equipment shall be inspected to ensure conformance to the applicable drawings and to assure that they are acceptable as to permanence and readibility.

Marking OK _____

T-711889-3

6. FUNCTIONAL TESTS

6.1 RELAY AND RESISTANCE CHECKS

6.1.1 With the relays and amplifier de-energized, make the following resistance measurements using the Simpson Model 269:

From (+)	To (-)	Ohms Required	Ohms Measured
Pin 13	Pin 6	500±10%	
*Pin 6	Pin 13	< 100	
Junction of K1A & C1	Pin 4	> 10 Meg	
Junction of K1A & C1	Pin 3	33.2K±10%	
Junction of R6 & C6	Junction of R8 & R9	< 1	
Pin 5	Pin 8	> 10 Meg	
Pin 5	Pin 9	< 1	
Pin 12	Pin 10	> 10 Meg	
Pin 12	Pin 11	< 1	
Pin 21	Pin 19	1030±10%	
*Pin 19	Pin 21	< 100	
Pin 17	Pin 15	> 10 Meg	
Pin 17	Pin 14	< 1	
Pin 20	Pin 16	> 10 Meg	

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From (+)	To (-)	Ohms Required	Ohms Measured
Pin 20	Pin 18	< 1	
Pin 3	TP1	< 1	
Pin 4	TP2	< 1	
Pin 35	TP3	< 1	

* Use X1 scale on Simpson Model 269.

6.1.2 Energize Relays K1 and K2 from the 28 VDC source and make the following resistance measurements:

From (+)	To (-)	Ohms Required	Ohms Measured
Junction of K1A & C1	Pin 4	1.2Meg±10%	
Junction of K1A & C1	Pin 3	>1 Meg	
Junction of R6 & C6	Junction of R8 & R9	> 1.2 Meg	
Pin 5	Pin 8	< 1	
Pin 5	Pin 9	>10 Meg	
Pin 12	Pin 10	< 1	
Pin 12	Pin 11	>10 Meg	
Pin 17	Pin 15	< 1	
Pin 17	Pin 14	>10 Meg	
Pin 20	Pin 18	> 10 Meg	
Pin 20	Pin 16	<1	

T-711889-3

6.2 GAIN AND LIMIT CHECK

6.2.1 Energize Relay K1 from the 28 VDC supply and apply the plus and minus 15 VDC to the board.

6.2.2 Ground Pin 4 and adjust the voltage offset of A1 for minimum output at Pin 35 ($<$ 1 mv.). Record offset voltage: _____. Remove ground.

6.2.3 Apply a signal to Pin 4 of approximately 1 VDC of either polarity and measure the output at Pin 35 with the DVM. Determine the DC gain and record: (K = 1.80$\pm$.036) _____.

6.2.4 Apply positive and negative signals to Pin 4 of sufficient amplitude to measure the output limits at Pin 35 and record the voltage limits.

Positive Limit (4$\pm$.5 VDC) _____

Negative Limit (-4$\pm$.5 VDC) _____

6.3 FREQUENCY RESPONSE CHECK

6.3.1 Run a frequency response between input Pin 4 and output Pin 35 with K1 energized and K2 de-energized. Plot gain in db and phase in degrees on Figure 1. The following tolerances shall be met in the range indicated:

.01 rad/sec $\leq$ W $\leq$ 4 rad/sec

GAIN$\pm$2db from nominal

PHASE$\pm$10° from nominal

T-711889-3

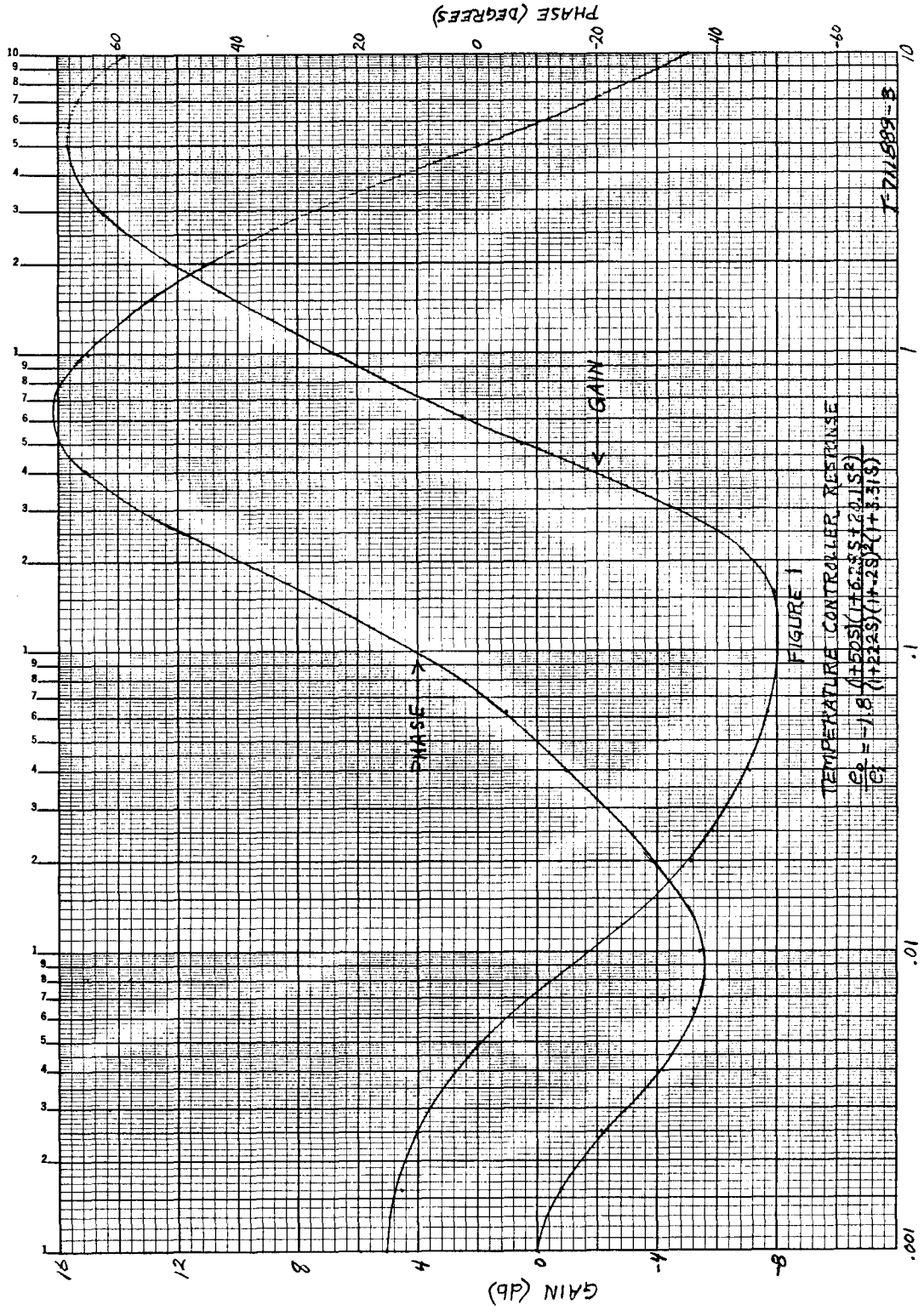

Figure 1
Temperature Controller Response

Astronuclear Laboratory

WANL-TME-1704

T-711889-4

ACCEPTANCE TEST SPECIFICATION AND PROCEDURE

Experimental Controller No. 1

Temperature Error Amplifier

910E314G01

DATE: August, 1967

PREPARED BY:

Circuits Design Date
Equipment Design

APPROVED BY:

Supervisor, Circuits Design Date
Equipment Design

Quality Engineering Date

Control Systems Engineering Date

INFORMATION CATEGORY

Authorized Classifier Date

T-711889-4
ACCEPTANCE TEST SPECIFICATION AND PROCEDURE
Experimental Controller No. 1
Temperature Error Amplifier
910E314G01

1. SCOPE

This document contains the requirements for the acceptance testing of the Amplifier Circuit Board prior to incorporating the board into the Experimental Controller Chassis.

2. REQUIREMENTS

2.1 The acceptance test shall consist of a Visual Examination (to be performed by Quality Control) and a Functional Test (to be performed by Electronics and Instrumentation and witnessed by Quality Control).

2.2 The acceptance test shall be performed in the order of and as specified in the procedure. Discrepancies found during the visual examination shall be corrected and reinspected before performing the functional test. Failure or inability to obtain a required measurement during formal functional testing shall result in establishing a "hold" on the test. The failure or inadequacy shall be recorded by Quality Control and shall be reviewed by the WANL Engineering Review Board (ERB). The equipment shall be repaired and sections of the test repeated as determined by the ERB. Visual examination shall be performed on the reworked or repaired areas before resuming testing.

3. APPLICABLE DOCUMENTS

3.1 Drawing 910E314 - Temperature Error

3.2 Drawing 928F960G01 - Printed Circuit Board

4. EQUIPMENT REQUIRED

4.1 +15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.2 -15±.05 VDC source with ±0.05% regulation and 1 mv. max. ripple

4.3 Positive signal source, variable 0-10 VDC with .01% resolution and 1 mv. max. ripple

4.4 Negative signal source, variable 0-10 VDC with .01% resolution and 1 mv. max. ripple

4.5 Model 269 Simpson Ohmmeter or equal

4.6 Digital Voltmeter H-P 3440A or equal

4.7 Set of equipment to measure frequency response and phase shift between .001 cps and 50 cps. (Weston-Boonshaft and Fuchs DA410 or equal)

T-711889-4

5. VISUAL EXAMINATION

The equipment under test shall be presented in its final form together with the applicable schematic and assembly drawing. The visual examination shall consist of the following parts:

5.1 WORKMANSHIP, ASSEMBLY, AND FIT

The inspector shall inspect the equipment for workmanship to WANL requirements, and to assure that the overall board is of the proper dimensions per the assembly drawing.

Westinghouse Drawing Number_____Rev._____

Workmanship OK _____

5.2 MATERIALS, PARTS, AND FINISHES

The equipment shall be inspected to assure that the materials, parts, and finishes are in accordance with the applicable assembly drawings. Incoming inspection records on materials, parts, and finishes shall be utilized to determine conformance to the assembly drawings where possible.

Materials OK_____

5.3 MARKING

The markings on the equipment shall be inspected to ensure conformance to the applicable drawings and to assure that they are acceptable as to permanence and readibility.

Marking OK_____

T-711889-4

6. FUNCTIONAL TESTS

6.1 RESISTANCE CHECKS

6.1.1 Make the following resistance measurements using the Simpson Model 269 as an ohmmeter.

From	To	Required	Measured
Pin 3	TP1	< 1 ohm	_____
Pin 8	TP2	< 1 ohm	_____
Pin 22	TP3	< 1 ohm	_____
Pin 24	TP4	< 1 ohm	_____
Pin 26	TP5	< 1 ohm	_____
Pin 22	Pin 24	200K±5%	_____
Pin 24	Pin 26	183K±5%	_____
Pin 26	TP1	33.7K±5%	_____

6.2 BALANCE AND DC GAIN CHECK

6.2.1 Apply power to the board. (+15 VDC to Pin 1 and -15 VDC to Pin 2; GND to Pin 3)

6.2.2 Ground Pins 22, 24, and 26 and adjust the voltage offset of A1 for minimum output (< 1 mv.) at Pin 8. Record offset voltage: _____. Verify that offset pot < 1/2 turn from ends: _____.

6.2.3 Measure gain using each input separately with other inputs grounded. Apply +10±.01 VDC inputs and record outputs below:

At Pin 22, (V = +10±.03)_____

At Pin 24, (V = +10±.03)_____

At Pin 26, (V = +.148±.01)_____

6.2.4 Apply opposite polarity signals to Pins 22 and 24 of about 5 VDC and equal in magnitude. The output at Pin 8 should be within $\pm$20 mv of the difference in magnitudes of the input signals. Record:

Input Voltage to Pin 22 _____ V

Input Voltage to Pin 24 _____ V

Output Voltage at Pin 8 _____ V

6.3 FREQUENCY RESPONSE CHECK

6.3.1 Determine the frequency response of the amplifier by using Pin 22 for input and grounding Pins 24 and 26. Plot gain in db and phase in degrees on Figure 1. The following tolerances shall be met in the range indicated:

a) $0.010 \leq W \leq 4$ rad/sec
Gain $\pm$2db from nominal
Phase $\pm 10^{\circ}$ from nominal

b) $4 \leq W \leq 314$ rad/sec
Gain $\pm$5db from nominal
Phase $\pm 20^{\circ}$ from nominal

T-711889-4

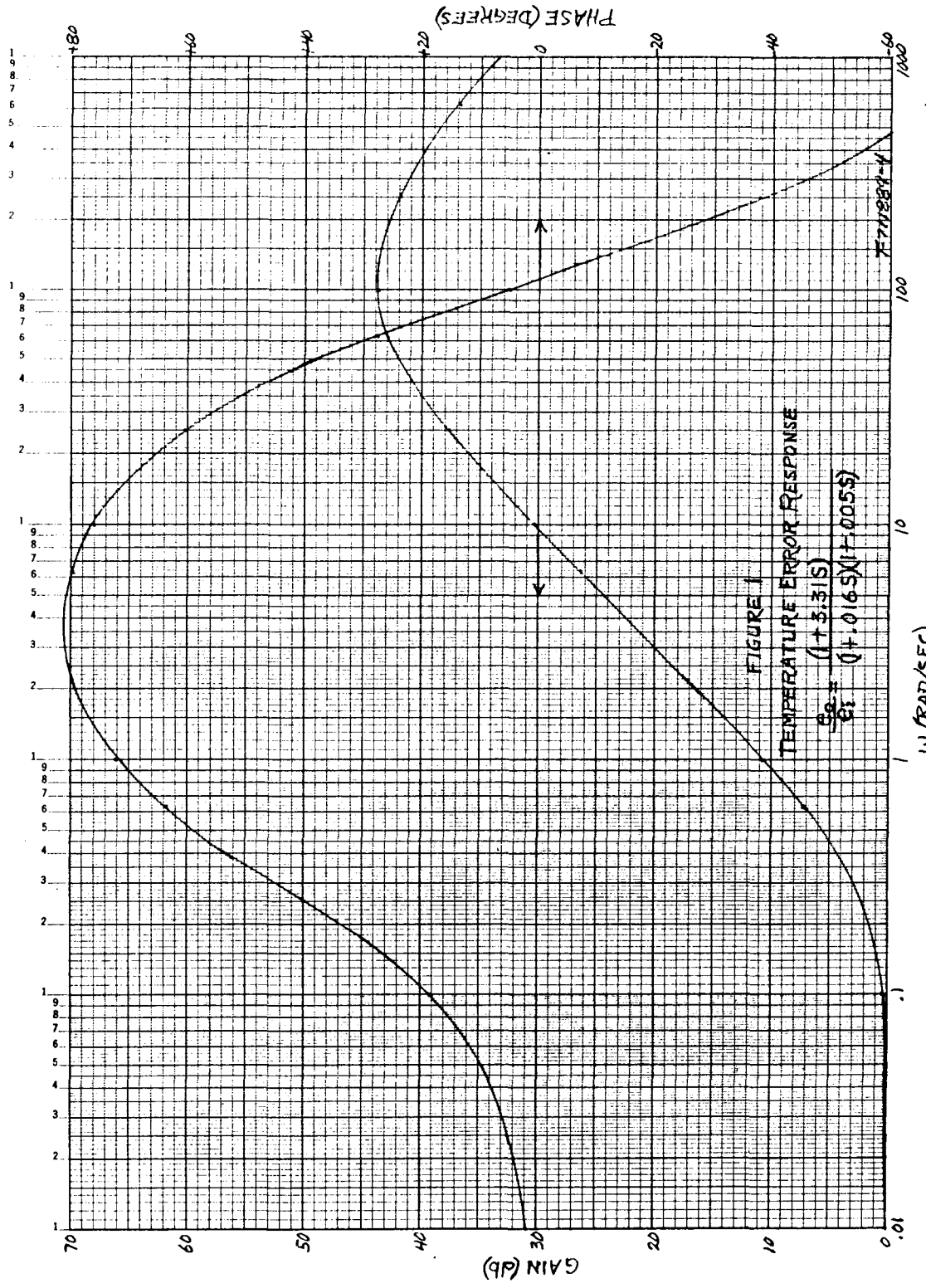

Figure 1
Temperature Error Response

T-711889-5

FUNCTIONAL TESTS FOR

XE-1 Experimental Controller No. 1 ETS-1
938J012G01
TEMPERATURE CONTROLLER CIRCUIT

DATE: September, 1967

PREPARED BY:

Circuits Design Date
Equipment Design

APPROVED BY:

9/7/67

Supervisor, Circuits Design Date
Equipment Design

10-6-67

Quality Engineering Date

Control Systems Engineering Date

INFORMATION CATEGORY

Unclassified

9/7/67

Authorized Classifier Date

T-711889-5
FUNCTIONAL TESTS FOR
XE-1 Experimental Controller No. 1 ETS-1
TEMPERATURE CONTROLLER CIRCUIT

1. SCOPE

This document contains the requirements for the functional tests for the XE-1 Experimental Controller No. 1 Acceptance Test Specification and Procedure, T-711889, Paragraph 6.1.

2. FUNCTIONAL TESTS

2.1 RESISTANCE AND CONTINUITY CHECKS

2.1.1 Before applying power to the chassis, make the following resistance checks using the Simpson Model 269:

From (+)	To (-)	Ohms Required	Ohms Measured
J1-R	TP1	< 2 Ohms	_____
J1-S	TP2	< 2 "	_____
J1-L	TP3	< 2 "	_____
J1-M	TP4	< 2 "	_____
J1-A	TP5	< 1 "	_____
J1-B	TP6	< 1 "	_____
J1-F	TP7	< 1 "	_____
J1-E	Chassis	< 1 "	_____
A1TP3	TP8	< 1 "	_____

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From (+)	To (-)	Ohms Required	Ohms Measured
TP7	J3-EE	< 1	_____
TP7	J3-CC	< 1	_____
TP7	J3-AA	< 1	_____
TP7	J3-W	< 1	_____
TP7	J3-Q	< 1	_____
TP8	J3-FF	< 1	_____
TP9	J3-DD	< 1	_____
TP10	J3-BB	< 1	_____
J3-X	J3-P	< 1	_____
J3-P	TP-12	< 1	_____

From (+)	To (-)	Ohms Required	Ohms Measured
A1TP4	TP9	< 1 Ohm	_____
A1TP5	TP10	< 1 "	_____
A1TP2	TP11	< 1 "	_____
A2TP3	TP12	< 1 "	_____
A1TP1	TP7	< 1 "	_____
A2TP2	TP11	< 1 "	_____
A2TP1	TP7	< 1 "	_____

2.2 OFFSET ADJUSTMENT, DC GAIN AND LIMIT CHECK

2.2.1 Apply +15VDC to J1-L, -15VDC to J1-M and Common to J1-F.

2.2.2 Jumper TP8 (T_D), TP9 (T_M), and TP10 (Freq Anal) to TP7 (Common). Connect the DVM between TP11 (T_E) and TP7. Adjust the offset pot on board A1 to obtain a minimum reading on the DVM (< 1 mv.). Record offset voltage: _____.

2.2.3 Move the DVM from TP11 to TP12 ($\dot{\Theta}_D$). Jumper TP11 to TP7. Adjust the offset pot on board A2 to obtain a minimum reading on the DVM (< 1 mv.). Record offset voltage: _____.

2.2.4 Remove the jumpers from between TP8 and TP11 and TP7. Apply a signal to TP8 of approximately 4 VDC of either polarity and measure the output at TP12 with the DVM. Determine the DC gain and record (K = 0.415±.008): _____.

2.2.5 Move the jumper to TP9 from TP9 to TP8. Apply a signal to TP9 of approximately 4 VDC with the polarity opposite to that used in Paragraph 2.2.4 and measure the output at TP12 with the DVM. Determine the DC gain and record (K = 0.415±.008): _____.

2.2.6 Apply positive and negative signals to TP9 of sufficient amplitude to measure the output limits at TP12 and record the voltage limits:

Positive Limit (4±.5VDC) _____

Negative Limit (-4±.5VDC) _____

2.2.7 Move the jumper to TP10 from TP10 to TP9. Apply a signal to TP10 of approximately 10VDC of either polarity and measure the output at TP12 with the DVM. Determine the DC gain and record (K = .00616±.00013_____. Move jumper to TP8 from TP8 to TP10.

2.2.8 Apply +28VDC to J3-HH and J3-Y and +28VDC return to J3-GG and J3-Z. Apply a signal to TP8 of approximately 2VDC of either polarity and measure the output at TP12 with the DVM five minutes after application of the signal. Determine the DC gain and record (K = 1.80±.036): _____.

2.3 FREQUENCY RESPONSE CHECK

2.3.1 Apply +28VDC to J3-HH and J3-Y and +28VDC return to J3-GG and J3-Z. Run a frequency response between input TP8 and output TP12 with TP9 and TP10 jumpered to TP7. Plot gain in db and phase in degrees on Figure 1. The following tolerances shall be met in the range indicated:

$.01 \text{ rad/sec} \leq W \leq 4 \text{ rad/sec}$

GAIN ±2db from nominal Curve (Figure 1)

PHASE $\pm 10^{\circ}$ from nominal Curve (Figure 1)

2.4 FUSE INDICATOR CHECK

2.4.1 Remove fuses F1 through F5. With the appropriate power supplies energized, fuse indicators F1 through F5 shall illuminate. When the fuses are replaced, the fuse indicators shall go out.

T-711889-6

ACCEPTANCE TEST SPECIFICATION AND PROCEDURE
(Checkout Procedure)

Experimental Controller No. 1

Drum Override

1. SCOPE

This document contains the requirements to functionally checkout the Drum Override on the Experimental Controller No. 1 Chassis (WANL Drawing 938J912, Schematic Diagram WANL Drawing 938J913).

These tests assume the individual P/C cards have been checked per the appropriate Accetpance Test Procedure and all card adjustments have been made per these Acceptance Test Procedures. The functional tests specified are to be performed as chassis checks.

2. DRUM OVERRIDE FUNCTIONAL TESTS

The following functional tests are to be performed to confirm proper operation of the Drum Override.

2.1 RESISTANCE AND CONTINUITY CHECKS

Before applying power to the chassis, make the following resistance checks:

From (+)	To (-)	Ohms Required	Ohms Measured
J2-FF	TP14	2 Ohms	_____
J2-EE	TP7	2 "	_____

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From (+)	To (-)	Ohms Required	Ohms Measured
J2-K	TP2	2 Ohms	
J2-BB	TP17	2 "	
J2-AA	TP7	2 "	
J2-Z	TP18	2 "	
J2-Y	TP7	2 "	
J2-W	TP19	2 "	
J2-V	TP7	2 "	
J2-U	TP16	2 "	
J2-T	TP7	2 "	
J2-Q	TP7	2 "	
J2-J	TP20	2 "	
J2-I	TP7	2 "	
J2-DD	A5TP6	2 "	
J2-CC	A5TP6	100 "	
J2-X	A5TP4	2 "	
J2-HH	A6TP1	2 "	
J2-GG	A6TP1	100 "	
J2-S	A6TP2	2 "	
J2-P	TP4	2 "	
J2-R	A6TP2	2 "	
J3-S	A7TP2	2 "	

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From (+)	To (-)	Ohms Required	Ohms Measured
J3-T	TP7	2 "	_____
J3-U	A6TP6	2 "	_____
J3-V	A6TP6	100 "	_____
A5TP2	J6-24	2 "	_____
TP15	A3TP6	2 "	_____

Connect Ohmmeter between A3TP6 and A3TP8 of the "Rate Limited Tracker" checkout card. Adjust A3R7 to CCW position

Adjust R1, "Rate Clamp Adjust", to 500 divisions (mid-range).

Apply power to the chassis.

2.2 BUFFER AMPLIFIER CHECKS

This test checks the proper operation of the buffered drum demand signal to the drums error meter, the buffered manual drum position signal, and the manual drums followup demand.

2.2.1 Connect a +5.00VDC voltage source between TP14 and TP7, the buffered drum demand input. Measure the output voltage between A7TP2 and TP7, the drums error meter output. This voltage should be +5.00±.1VDC.

Voltage between A7TP2 and TP7 _____ VDC

Measure the output voltage between TP16 and TP7, the manual drums followup demand output. This voltage should be +5.00±.1 VDC.

Voltage between TP16 and TP7 _____ VDC

2.2.2 Connect a +5.00 VDC voltage source between TP19 and TP7, the manual drums position demand input. Measure the output between TP20 and TP7, the drum override position demand. This voltage should be -5.00±.1 VDC.

Voltage between TP20 and TP7 _____ VDC

2.3 RATE CLAMP ACTIVATE CIRCUIT

This test checks the proper pickup of the "Rate Clamp Activate" Relay, A5K1, the latching of this relay, and the unlatching of A5K1.

2.3.1 Connect a +5 VDC voltage source between TP18 and TP7, the Auto Startup Exponential Setpoint input. Connect a +5.50 VDC voltage source between TP14 and TP7, the the Buffered Drums Demand input. Measure resistance between A5TP4 and J2-M. This resistance should be less than 2 ohms.

_____ Ohms

Remove the Checkout Card A3 and measure the resistance from TP15 to J6-4. This resistance should be $<$ 2 ohms.

_____ Ohms

2.3.2 Disconnect voltage source from TP14. Measure the resistance between A5TP4 and J2-M. This impedance should be $<$ 2 ohms.

2.3.3 Connect +28 VDC voltage source between J3-U and J3-V, the Engine Reset input. Measure the resistance between A5TP4 and J2-M. This resistance should be $>$ 100 megohms.

_____ Ohms

Insert Card A3.

T-711889-6

2.4 DRUM OVERRIDE NORMAL/OPERATE CIRCUIT

This test checks the proper operation of the Drum Override Circuit, "Rate Limited Tracker" card and the pickup, latching and unlatching of the drum override normal/operate function.

2.4.1 Connect checkout circuit as shown in Figure 1.

2.4.2 Connect a DVM between TP13 and TP7. Adjust R1 "Rate Clamp Adjust" until the DVM reads -3.2 VDC (1.25°/sec).

_____ DVM Reading

2.4.3 Remove Card A3

2.4.4 Connect DVM between TP17 and TP7. Adjust 5K external pot until DVM reads -4.29 VDC.

_____ DVM Reading

2.4.5 Connect +5.00 VDC (90°) to TP16 by closing S2.

2.4.6 Connect +5.50 VDC (99°) to TP14 by closing S3.

Verify DVM connected as in Figure 1 reads +10VDC_____

2.4.7 Close and Open S1. Verify DVM reads +10VDC _____

2.4.8 Open S3. Verify DVM read 0 _____

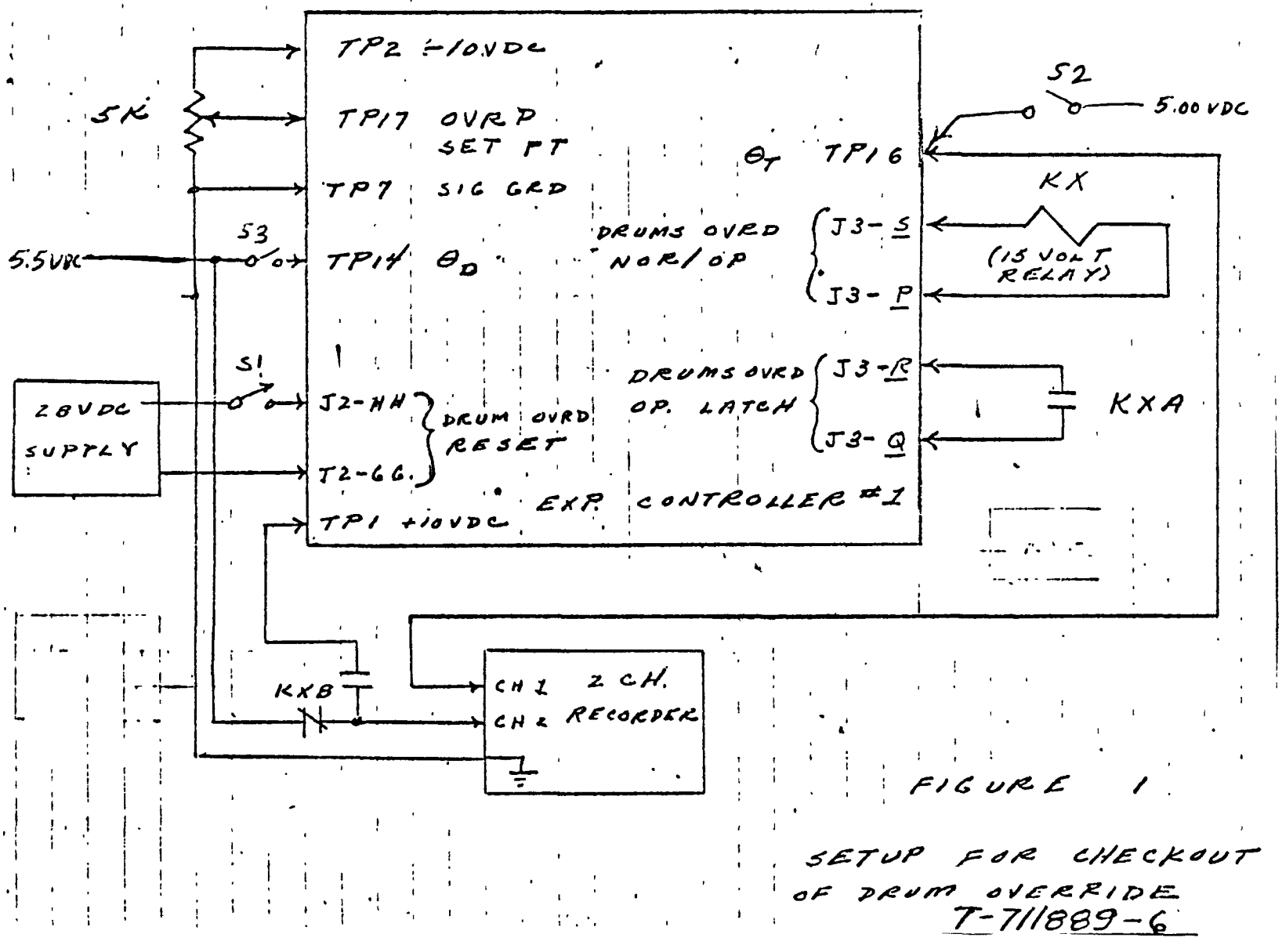


Figure 1

Setup for Checkout of Drum Override

T-711883-5

ACCEPTANCE TEST SPECIFICATION AND PROCEDURE

Relay Module, 4PDT, 2 Unit

979D576G01-G02

DATE: September, 1967

PREPARED BY: H. Kowalchuck 9-26-67
Circuits Design Date
Equipment Design

APPROVED BY: R. G. Lewis 9/27/67
Supervisor, Circuits Design Date
Equipment Design

[illegible] 10/2/67
Quality Engineering Date

C. C. Merchant 9/27/67
Control Systems Engineering Date

INFORMATION CATEGORY
Unclassified
R. G. Lewis 9/28/67
Authorized Classifier Date

T-711883-5
ACCEPTANCE TEST SPECIFICATION AND PROCEDURE
Relay Module, 4PDT, 2 Unit
979D576G01-G02

1. SCOPE

This document contains the requirements for the acceptance testing of the Relay Module Circuit Board prior to incorporating the board into a chassis.

2. REQUIREMENTS

2.1 The acceptance test shall consist of a Visual Examination (to be performed by Quality Control) and a Functional Test (to be performed by Electronics and Instrumentation and witnessed by Quality Control).

2.2 The acceptance test shall be performed in the order of and as specified in the procedure. Discrepancies found during the visual examination shall be corrected and reinspected before performing the functional test. Failure or inability to obtain a required measurement during formal functional testing shall result in establishing a "hold" on the test. The failure or inadequacy shall be recorded by Quality Control and shall be reviewed by the WANL Engineering Review Board (ERB). The equipment shall be repaired and sections of the test repeated as determined by the ERB. Visual examination shall be performed on the reworked or repaired areas before resuming testing.

3. APPLICABLE DOCUMENTS

3.1 Drawing 979D576 - Relay Module, 4PDT, 2 Unit

3.2 Drawing 928F423 - Printed Circuit Board

3.3 Drawing 979D575 - Schematic, Relay Module

4. EQUIPMENT REQUIRED

4.1 Model 269 Simpson Ohmmeter or equal

4.2 $+15 \pm 1$ VDC Power Source

5. VISUAL EXAMINATION

The equipment under test shall be presented in its final form together with the applicable schematic and assembly drawing. The visual examination shall consist of the following parts:

5.1 WORKMANSHIP, ASSEMBLY, AND FIT

The inspector shall inspect the equipment for workmanship to WANL requirements, and to assure that the overall board is of the proper dimensions per the assembly drawing.

Westinghouse Drawing Number_____Rev._____

Workmanship OK _____

5.2 MATERIALS, PARTS, AND FINISHES

The equipment shall be inspected to assure that the materials, parts, and finishes are in accordance with the applicable assembly drawings. Incoming inspection records on materials, parts, and finishes shall be utilized to determine conformance to the assembly drawings where possible.

Materials OK_____

5.3 MARKING

The markings on the equipment shall be inspected to ensure conformance to the applicable drawings and to assure that they are acceptable as to permanence and readibility.

Marking OK_____

6. FUNCTIONAL TESTS

6.1 RESISTANCE CHECK - RELAY DE-ENERGIZED

6.1.1 Make the following resistance checks:

From (+)	To (-)	Ohms	Check
TP1	Pin 4	< 1	
TP2	Pin 3	< 1	
TP3	Pin 5	< 1	
TP4	Pin 13	< 1	
TP5	Pin 11	< 1	
TP6	Pin 25	< 1	
TP7	Pin 24	< 1	
TP8	Pin 26	< 1	
TP9	Pin 34	< 1	
TP10	Pin 32	< 1	
Pin 4	Pin 12	500±10%(G01)	
Pin 4	Pin 12	206±10%(G02)	
*Pin 12	Pin 4	< 30	
Pin 3	Pin 2	> 100 Meg	
Pin 3	Pin 7	< 1	
Pin 5	Pin 6	> 100 Meg	
Pin 5	Pin 8	< 1	
Pin 13	Pin 14	> 100 Meg	
Pin 13	Pin 1	< 1	
Pin 11	Pin 10	> 100 Meg	
Pin 11	Pin 9	< 1	
Pin 25	Pin 33	500±10%	
*Pin 33	Pin 25	< 30	

From (+)	To (-)	Ohms	Check
Pin 24	Pin 23	> 100 Meg	_____
Pin 24	Pin 28	< 1	_____
Pin 26	Pin 27	> 100 Meg	_____
Pin 26	Pin 29	< 1	_____
Pin 34	Pin 35	> 100 Meg	_____
Pin 34	Pin 22	< 1	_____
Pin 32	Pin 31	> 100 Meg	_____
Pin 32	Pin 30	< 1	_____

*Use X1 scale on Ohmmeter.

6.2 RESISTANCE CHECK - RELAY ENERGIZED

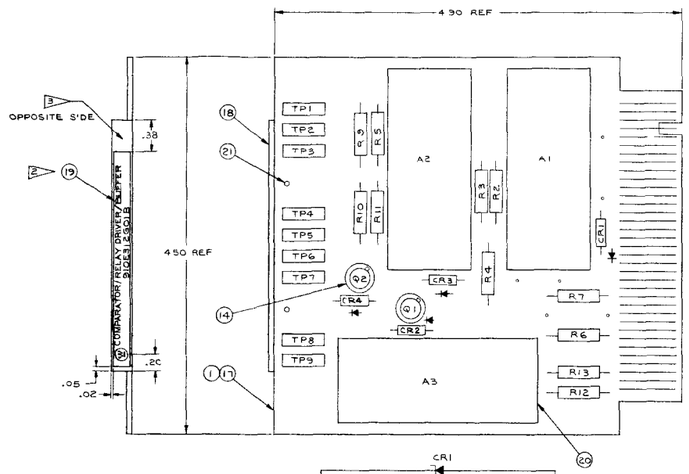
6.2.1 Ground Pin 12 and Pin 33.

6.2.2 Energize Relays K1 and K2 by applying +15 VDC to Pin 4 and Pin 25.

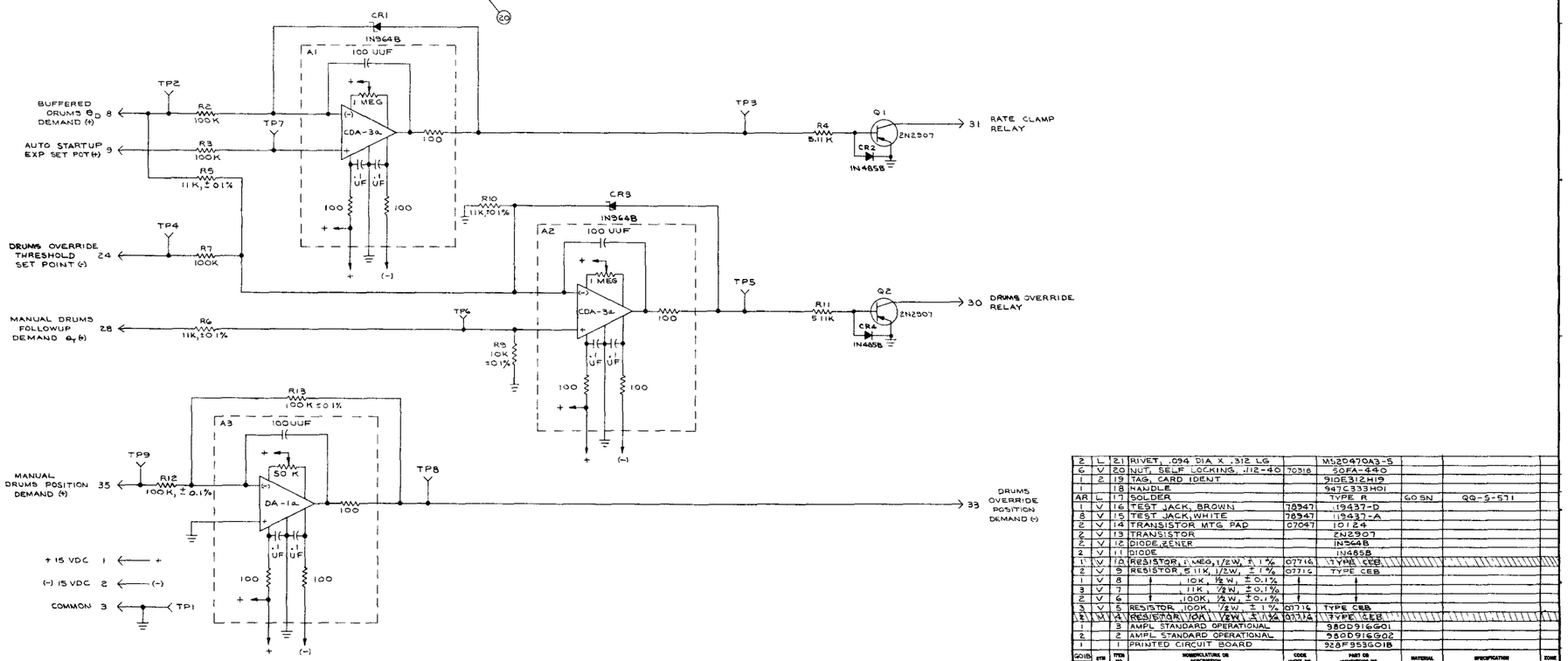
6.2.3 Make the following resistance checks:

From	To	Ohms	Check
Pin 3	Pin 2	< 1	_____
Pin 3	Pin 7	> 100 Meg	_____
Pin 5	Pin 6	< 1	_____
Pin 5	Pin 8	> 100 Meg	_____
Pin 13	Pin 14	< 1	_____
Pin 13	Pin 1	> 100 Meg	_____
Pin 11	Pin 10	< 1	_____
Pin 11	Pin 9	> 100 Meg	_____
Pin 24	Pin 23	< 1	_____
Pin 24	Pin 28	> 100 Meg	_____
Pin 26	Pin 27	< 1	_____
Pin 26	Pin 29	> 100 Meg	_____
Pin 34	Pin 35	< 1	_____
Pin 34	Pin 22	> 100 Meg	_____
Pin 32	Pin 31	< 1	_____
Pin 32	Pin 30	> 100 Meg	_____

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED PER ECO 15022	8-3-67 WALKUP	MED 8-4-67 [illegible] 8-4-67 [illegible] [illegible]
	B	REVISED PER ECO 15982	5-13-67 JTP	WBP 9-14-67 [illegible] 9/14/67 [illegible]



REFERENCE DESIGNATION	ITEM NO
A1, A2	2
A3	3
R1, R8	4
R2, R3, R7	5
R12, R13	6
R5, R6, R10	7
R9	8
R4, R11	9
CR2, CR4	11
CR1, CR3	12
Q1, Q2	13
TP2 THRU TP3	15
TP1	16



QTY	LTR	ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO.	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
2	L	21	RIVET, .094 DIA X .312 LG		MS20470A3-5			
6	V	20	NUT, SELF LOCKING, .112-40	70318	50FA-440			
1		19	TAG, CARD IDENT		910E312H19			
1		18	HANDLE		947C333H01			
AR	L	17	SOLDER		TYPE R	60 SN	QQ-S-571	
1	V	16	TEST JACK, BROWN	78947	19437-D			
8	V	15	TEST JACK, WHITE	78947	19437-A			
2	V	14	TRANSISTOR MTG. PAD	07047	10124			
2	V	13	TRANSISTOR		2N2907			
2	V	12	DIODE, ZENER		IN964B			
2	V	11	DIODE		IN4858			
1	V	10	RESISTOR, 1 MEG, 1/2W, ± 1%	07716	TYPE CEB			
2	V	9	RESISTOR, 5.11K, 1/2W, ± 1%	07716	TYPE CEB			
1	V	8	" 10K, 1/2 W, ± 0.1%	"	"			
3	V	7	" 11K, 1/2W, ± 0.1%	"	"			
2	V	6	" 100K, 1/2W, ± 0.1%	"	"			
3	V	5	RESISTOR, 100K, 1/2W, ± 1%	07716	TYPE CEB			
2	V	4	RESISTOR, 10K, 1/2W, ± 1%	07716	TYPE CEB			
1		3	AMPL STANDARD OPERATIONAL		880D916G01			
2		2	AMPL STANDARD OPERATIONAL		880D916G02			
1		1	PRINTED CIRCUIT BOARD		928F853G01B			

LIST OF MATERIALS

3. APPLY WANL SERIAL NO. WITH INDELIBLE INK OR MARKING ENAMEL.
4. MAKE FROM 947C086H12. LETTERING TO BE WHITE ON BLACK BACKGROUND.

1. INTERPRET SYMBOLS IN L/M SYMBOL COLUMN AS FOLLOWS:
   L = ITEM STOCKED BY CONTROL SYSTEMS LABORATORY
   N = ITEM STOCKED BY NERVA STORES
   V = VENDOR ITEM

NOTES:

UNLESS OTHERWISE SPECIFIED — INTERPRET DWG PER MIL-D-1000 — DIM IN INCHES MARKED OR NOT — TOLERANCES — DO NOT SCALE — 2PL DEC ± .02 — 3PL DEC ± — ANGLES ± — MATL — FINISH — BREAK SHARP EDGES

CONTRACT NO. NP-1

938J512G01	XE-1 (ECS)	T-711889-1	TEST		
		P294517-1	IDENT		
NEXT ASSY.	USED ON	P294656	PL. IDENT	INFORMATION CATEGORY	
B	APPLICATION	SPECIFICATION	TYPE		
DWG CODE NO		0751588-BS	NE 1530	AUTHENTICATED CLASSIFIER	DATE

WANL [illegible]

Westinghouse Astronuclear Laboratory, Pittsburgh, Pennsylvania

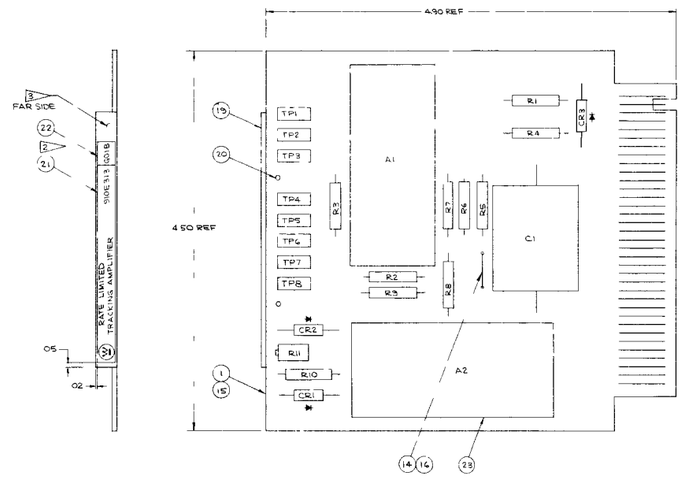
COMPARATOR / RELAY DRIVER / BUFFER

SIZE	CODE IDENT NO.	DWG. NO.
E	14683	910E312

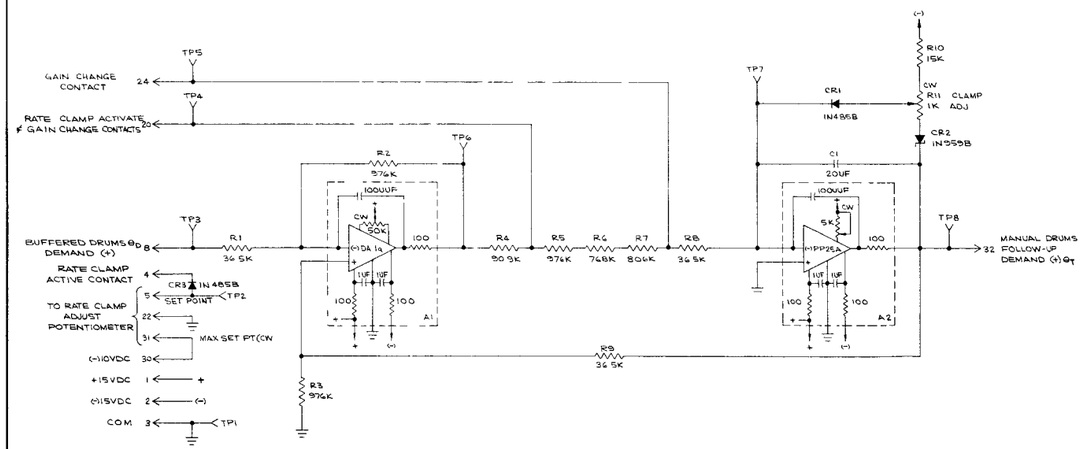
SCALE 2/1 — WT ACT — SPF CALC — SHEET 1 OF 1

Drawing 1
910E312
Comparator/Relay Driver/Buffer

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REDRAWN PER ECO 15995	7-28-67	7-28-67



REFERENCE DESIGNATION	ITEM NO
R1, R8, R9	2
R2, R3, R5	3
R4	4
R6	5
R7	6
R10	7
R11	8
CR1, CR3	9
CR2	10
C1	11
A1	12
A2	13
TP2 THRU TP8	17
TP1	18



QTY REQD	SYM	ITEM NO	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO	PART OR IDENTIFYING NO	MATERIAL	SPECIFICATION	ZONE
4	V	23	NUT, SELF LOCKING, 112-40	70318	SCFA-440			
1		22	TAG, GROUP IDENT		910E313H22B			
1		21	TAG, CARD IDENT (LARGE)		910E313H21B			
2	L	20	RIVET, .094 DIA x .312 LG		MS20470A3-5			
1		19	HANDLE		947C333H01A			
1	L	18	TEST JACK, BROWN	78947	112437-D			
7	L	17	TEST JACK, WHITE	78947	112437-A			
AR	V	16	TUBING, NATURAL	52194	TFT-200/24	TEFLON		
AR	L	15	SOLDER		TYPE R	60 SN	QQ-S-571	
AR	L	14	WIRE, AWG NO 24 BARE		TYPE S		QQ-W-343	
1		13	AMPL OPERATIONAL		980D922G01A			
1		12	AMPL STANDARD OPERATIONAL		980D516G01A			
1	V	11	CAPACITOR, 20UF ±1%, 50VDC	09134	315P-206A			
1		10	DIODE, ZENER		IN5539B			
2		9	DIODE		IN485B			
1		8	POTENTIOMETER, 1K ±5%, 1W	80294	53RW-44-102			
1	L	7	RESISTOR 15K ±1%, ½W	07716	TYPE CEB			
1		6	806K					
1		5	74.8K					
1		4	90.9K					
3		3	57.6K					
3	V	2	RESISTOR, 36.5K ±1%, ½W	07716	TYPE CEB			
1			PRINTED CIRCUIT BOARD		928F354G01B			

LIST OF MATERIALS

3> APPLY WANL SERIAL NO WITH INDELIBLE INK OR MARKING ENAMEL

2> MAKE FROM 346C760H02 ¢H03 LETTERING TO BE WHITE ON BLACK BACKGROUND

1 INTERPERT SYMBOLS IN L/M SYMBOL COLUMN AS FOLLOWS
L= ITEM STOCKED BY CONTROL SYSTEMS LABORATORY
N= ITEM STOCKED BY NERVA STORES, V= VENDOR ITEM

NOTES

UNLESS OTHERWISE SPECIFIED
INTERPRET DWG PER MIL-D-1000 FOR IN INCHES BASED ON 80°F
TOLERANCES — DO NOT SCALE
2PL DEC ± .02 | 3PL DEC ± | ANGLES ±

CONTRACT NO NPR
DEPT
APPROVED
DRAWN
CHECKED
ENG APPR
MFG
MATL

Westinghouse Astronuclear Laboratory
Pittsburgh, Pennsylvania

RATE LIMITED TRACKING AMPLIFIER

938J92Q01	XE-1(ECS)	D7516B865-2	TEST	
938J92Q01	XE-1(ECS)	D7516B865-1	IDENT	
NEXT ASSY	USED ON	P2S4496	PL IDENT	
R APPLICATION		SPECIFICATION	TYPE	
DWG CODE NO	1	D7516B865	4-81530	

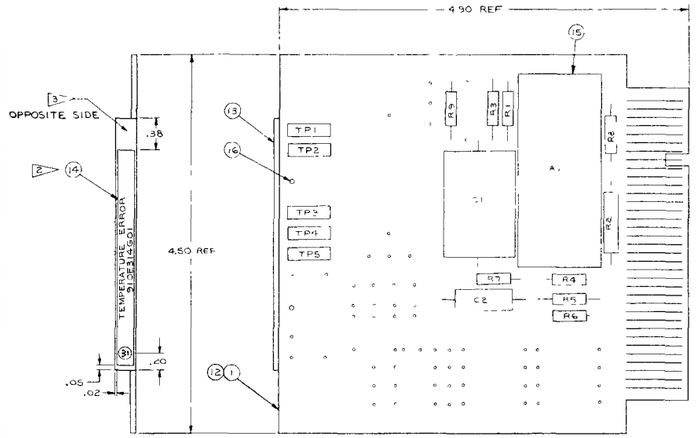
INFORMATION CATEGORY
AUTHORIZED CLASSIFIER — DATE 10/16/67

WANL
C.C. MERCHANT 7-26-67

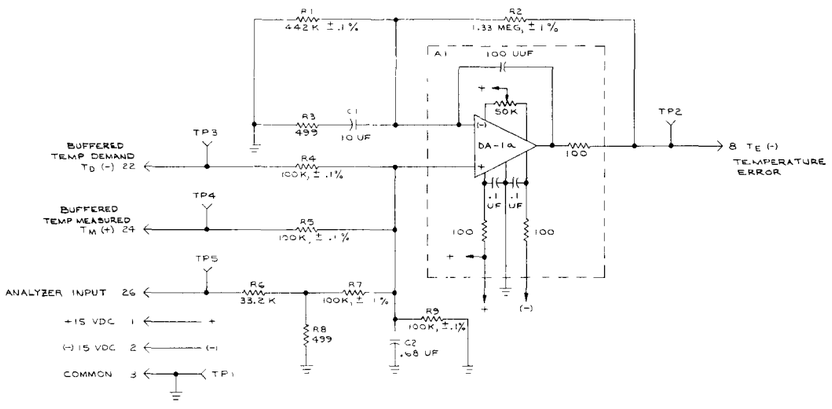
DWG SIZE E | CODE IDENT NO 14683 | DWG NO 910E313
SCALE 2/1 | WT ACT — | WT CALC — | SHEET 1 OF 1

Drawing 2
910E313
Rate Limited Tracking Amplifier

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



REFERENCE DESIGNATION	ITEM NO
A1	2
C2	3
C1	4
R1	5
R4, R5, R7, R9	6
R2	7
R3, R8	8
R6	9
TP2 THRU TP5	10
TP1	11



3 APPLY WANL SERIAL NO. WITH INDELIBLE INK OR MARKING ENAMEL.

2 MAKE FROM 947C086H12. LETTERING TO BE WHITE ON BLACK BACKGROUND.

1. INTERPRET SYMBOLS IN L/M SYMBOL COLUMN AS FOLLOWS:
   L - ITEM STOCKED BY CONTROL SYSTEMS LABORATORY
   N - ITEM STOCKED BY NERVA STORES
   V - VENDOR ITEM

NOTES:

QTY REQD	SYM	ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO.	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
2	L	16	RIVET .094 DIA X .312 LG		MS20470A3-5			
2	V	15	NUT, SELF LOCKING, 112-40	70318	50FA-440			
1	2	14	TAG, CARD IDENT		910E314H14			
1		13	HANDLE		947C333H01			
AR	L	12	SOLDER		TYPE R	60 SN	QQ-S-571	
1	V	11	TEST JACK, BROWN	78947	11937-D			
4	V	10	TEST JACK, WHITE	78947	11937-A			
1	V	9	RESISTOR, 33.2 K, 1/2W ± 1%	07716	TYPE CEB			
2	V	8	RESISTOR, 499 OHM, 1/2W, ± 1%	07716	TYPE CEB			
1	V	7	RESISTOR, 1.33 MEG, 1 W, ± 1%	07716	TYPE CEC			
4	V	6	RESISTOR, 100 K, 1/2 W, ± .1%	07716	TYPE CEB			
1	V	5	RESISTOR, 442 K, 1/2 W, ± 1%	07716	TYPE CEB			
1	V	4	CAPACITOR, .10 UF, 50 VDC ± 1%	09134	315F-106A			
1	V	3	CAPACITOR, .68 UF, 50 VDC ± 1%	09134	315F-684A			
1		2	AMPL, STANDARD OPERATIONAL		8300916G01			
1		1	PRINTED CIRCUIT BOARD		928F960G01			

LIST OF MATERIALS

				UNLESS OTHERWISE SPECIFIED	CONTRACT NO. NP-1
				INTERPRET DWG PER MIL-D-1000 DIM IN INCHES BASED ON MFT	DRAWN 10-29-63
				TOLERANCES – DO NOT SCALE	CHECKED 10-29-63
				DEC. ± .02 / ANGLES ± 1	APPROVED 10-29-63
		T-711883-4	TEST		MATL.
938.9(260)	XE - (ECS)	P294617-1	IDENT		
NEXT ASSY	USED ON	P294696	SL. IDENT	INFORMATION CATEGORY	WANL
S APPLICATION		SPECIFICATION	TYPE		
DWG CODE NO	1	0751588-85	NE1430	AUTHORIZED CLASSIFIER / DATE	

Westinghouse Astronuclear Laboratory
Pittsburgh, Pennsylvania

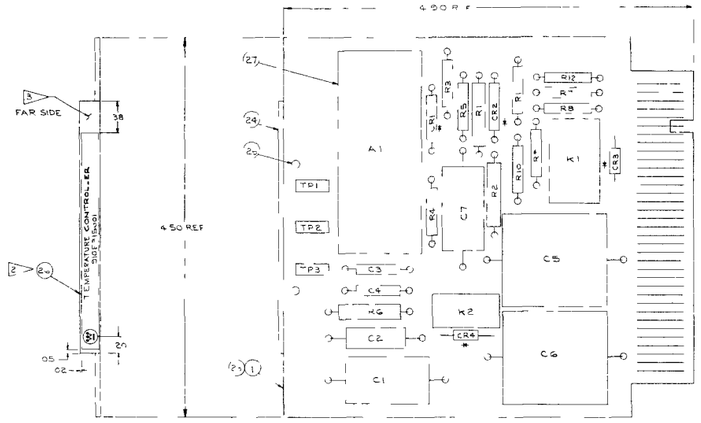
TEMPERATURE ERROR

SIZE	CODE IDENT NO	DWG. NO.
E	14683	910E314

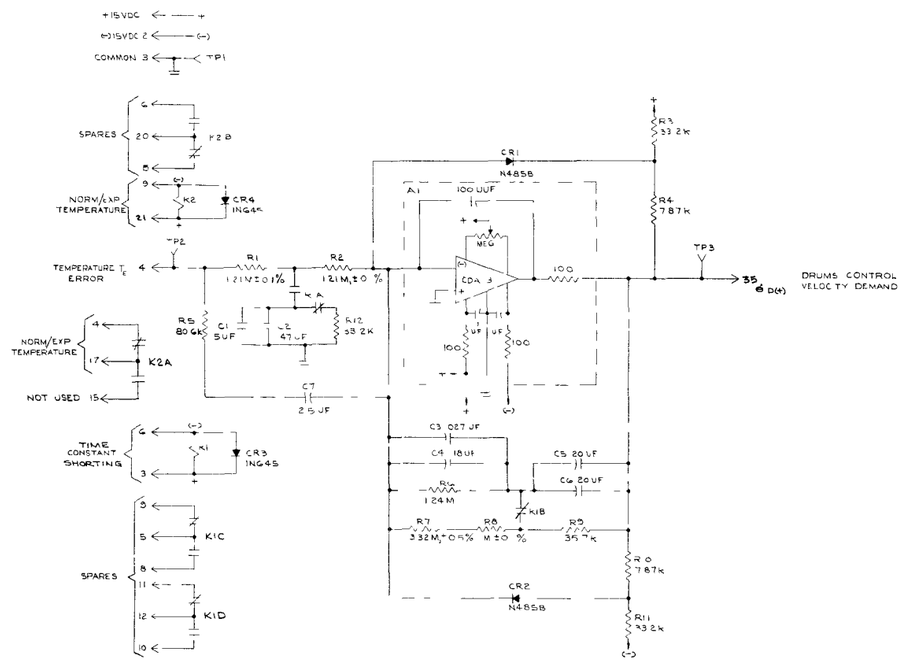
SCALE 2/1 | WT ACT — | WT CALC — | SHEET 1 OF 1

Drawing 3
910E314
Temperature Error Amplifier

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



REFERENCE DESIGNATIONS	ITEM NO
R1, R2	3
R3, R11, R12	2
R4, R10	4
R5	5
R6	6
R7	7
R8	8
R9	9
CR3, CR4	10
CR1, CR2	11
C1	12
C2	13
C3	14
C4	15
C5, C6	16
C7	17
TP2, TP3	18
TP1	19
K1	20
K2	21
A1	22



3 ⇒ APPLY WANL SERIAL NO WITH INDELIBLE INK OR MARKING ENAMEL

6 ⇒ MAKE FROM .51 OBNIC LETTERING TO BE WHITE ON BLACK BACKGROUND

1 INTERPRET THIS COLUMN AS FOLLOWS
ITEM STOCKED BY CONTROL SYSTEMS LABORATORY
ITEM STOCKED BY NEA STORES V VENDOR ITEM

NOTES

QTY REQD	STR	ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
1		28	AMPLIFIER STANDARD OPERATIONAL		880D816G02			
2	V	27	NUT, SELF LOCKING, 112-40	70318	MSFA-440			
1	Z	26	TAG, CARD IDENT		910E315H26			
2	L	25	RIVET, .094 DIA X .312 LG		MS20470A3 5			
1		24	HANDLE		847C333H01			
AR	L	23	SOLDER		TYPE R	60SN	QQ-S-571	
1		22	AMPLIFIER, STANDARD OPERATIONAL		880D816G02			
1	V	2	RELAY, 2PDT (24-35VDC)	01526	*SAV5005K1			
1	V	20	RELAY, 4PDT (20-34VDC)	0 526	*SAH5005K1			
1	L	19	TEST JACK, BROWN	78547	19437-D			
2	L	18	TEST JACK, WHITE	78547	19437 A			
1	V	17	CAPACITOR, 2.5 UF, 50VDC ±1%	09134	315F-255A			
2	V	16	" .20UF, 50 VDC, ±1%		315F-206A			
1	V	15	" .18UF, 50VDC ±1%		315F-184A			
1	V	14	" .027UF 50 VDC, ±1%		315F-273A			
1	V	13	" .47UF, 50VDC ±1%		315F-474A			
1	V	12	CAPACITOR, 5UF 50VDC ±1%	09134	315F-505A			
2	V	11	DIODE		N4858			
2	V	10	DIODE		IN645			
1	V	9	RESISTOR, 35.7K, 1/2W ±1%	07716	TYPE CEB			
1	V	8	" 1M, 1/2W, ±.01%		TYPE CEB			
1	V	7	" 3.32M, 1/2W ±.05%		TYPE DCC			
1	V	6	" 24M, 1W ±1%		TYPE CEC			
1	V	5	" 80.6K, 1/2W, ±1%		TYPE CEB			
2	V	4	" 7.87K 1/2W, ±1%		TYPE CEB			
2	V	3	" 12.1M, 1W, ±.01%		TYPE CEC			
3	V	2	RESISTOR, 33.2K 1/2W, ±1%	07716	TYPE CEB			
1		1	PRINTED CIRCUIT BOARD		928F978G01			

LIST OF MATERIALS

								UNLESS OTHERWISE SPECIFIED	CONTRACT NO NR
								INTERPRET DWG PER MIL-D-1000 DIM IN INCHES BASIS OF MFT	DATE LE HARDESTY 10/31/62
								TOLERANCES — DO NOT SCALE	DRAWN J. D. 10/31/62
								SPL DEC ± SPL DEC ± ANGLES ±	CHECKED [illegible] 11/1/62
									ENGR [illegible] 11/1/62
				T711B83-3	TEST	± .02	±	±	MATL
933/912G01	XE (ECS)		PP545 7 1		IDENT	—	⊥	⊕	
NEXT ASSY	USED ON		PP545G5G		PL DENT	INFORMATION CATEGORY			WANL
B	APPLICATION		SPECIFICATION		TYPE				
	DWG CODE NO		07515B85		NE 1530	AUTHORIZED CLASSIFIER	DATE		

Westinghouse Astronuclear Laboratory
Pittsburgh, Pennsylvania

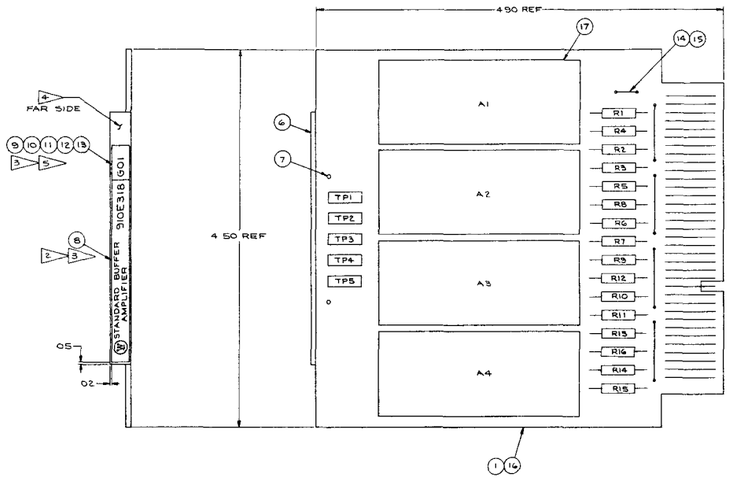
TEMPERATURE CONTROLLER

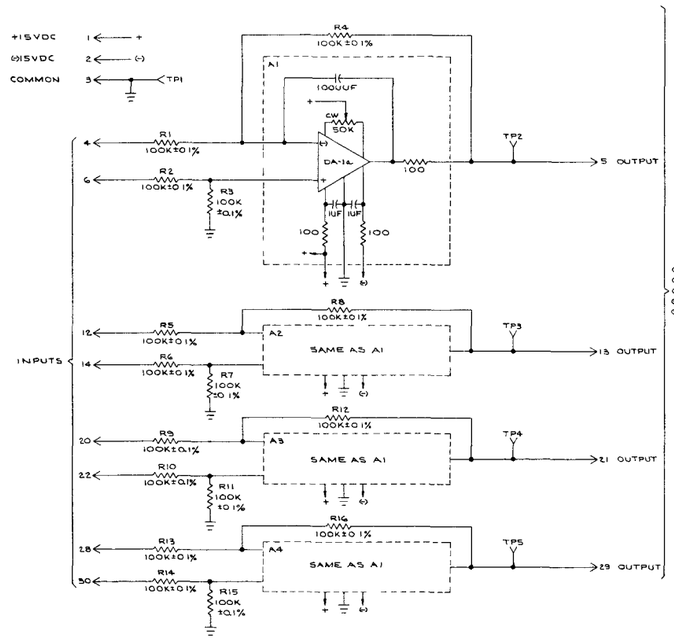
SIZE	CODE IDENT NO	DWG NO
E	14683	910E315

SCALE 2/1 — WT ACT — WT CALC — SHEET 1 OF 1

Drawing 4
910E315
Temperature Controller

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED





G01 AS SHOWN EXCEPT A1-A4 ARE REMOVED
G02 AS SHOWN EXCEPT A2 A4 ARE REMOVED
G03 AS SHOWN EXCEPT A3 (A4 ARE REMOVED
G04 AS SHOWN EXCEPT A4 IS REMOVED
G05 AS SHOWN

REFERENCE DESIGNATION	ITEM NO				
	G01	G02	G03	G04	G05
A1		2	2	2	2
A2			2	2	2
A3				2	2
A4					2
R1 THRU R16	3	3	3	3	3
TP1	4	4	4	4	4
TP2 THRU TP5	5	5	5	5	5

5. MAKE FROM 946C760H03 LETTERING TO BE WHITE ON BLACK BACKGROUND
4. APPLY WANL SERIAL NO WITH INDELIBLE INK OR MARKING ENAMEL.
3. ITEMS 8 & 9 ARE WORDED AS SHOWN, ITEMS 10, 11, 12 AND 13 BECOME 602, 603, 604 AND 605 RESPECTIVELY
2. MAKE FROM 946C760H02 LETTERING TO BE WHITE ON BLACK BACKGROUND.
1. INTERPRET SYMBOL IN L/M SYMBOL COLUMN AS FOLLOWS
   L= ITEM STOCKED BY CONTROL SYSTEMS LABORATORY
   N= ITEM STOCKED BY NERVA STORES
   V= VENDOR ITEM

NOTES

605	604	603	602	601	SYB	ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO.	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
8	6	4	2			V	17	NUT, SELF LOCKING, .112-40	70518	50FA-440			
AR	AR	AR	AR	AR	L	V	16	SOLDER		TYPE R	60SN	QQ-S-571	
AR	AR	AR	AR	AR	L	V	15	WIRE, AWG NO 24, BARE		TYPE S		QQ-W-343	
AR	AR	AR	AR	AR	L	V	14	TUBING, TEFLON, NATURAL	92194	TFT-200/24			
1							13	TAG, GROUP IDENT		910E318H13			
	1						12			910E318H12			
		1					11			910E318H11			
			1				10			910E318H10			
				1			9	TAG, GROUP IDENT		910E318H09			
1	1	1	1	1			8	TAG, CARD IDENT		910E318H08			
2	2	2	2	2	L		7	RIVET, .094 DIA x 312 LG		MS20470AB-5			
1	1	1	1	1			6	HANDLE		947C353H01			
4	4	4	4	4	L		5	TEST JACK, WHITE	78947	119437-A			
1	1	1	1	1	L		4	TEST JACK, BROWN	78947	119437-D			
16	16	16	16	16	V		3	RESISTOR, 100K ± 0.1%, 1/2W	07716	TYPE CEB			
4	3	2	1				2	AMPLIFIER, STANDARD OPERATIONAL		880D916G01			
1	1	1	1	1			1	PRINTED CIRCUIT BOARD		928F983G01			

LIST OF MATERIALS

				UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS ARE ON MACH. SURF. ON FRACT. ON BORES ON OTHER SURF.	CONTRACT NO. NP-1
				TOLERANCES — DO NOT SCALE	DRAWN W. WALKUP 4-24-67
				FRACT. DEC. ANGLES	CHECKED 4-24-67
		T-711883-4	TEST	± .02 ± ±	ENGINEER 4-24-67
	XE-1(ECS)	P234517-1	IDENT		QUALITY
NEXT ASSY	USED ON	P234G36	PL IDENT	INFORMATION CATEGORY	MATL
B	APPLICATION	SPECIFICATION	TYPE		
DWG CODE NO		D751588-BR	NE1550	AUTHORIZED CLASSIFIER DATE	

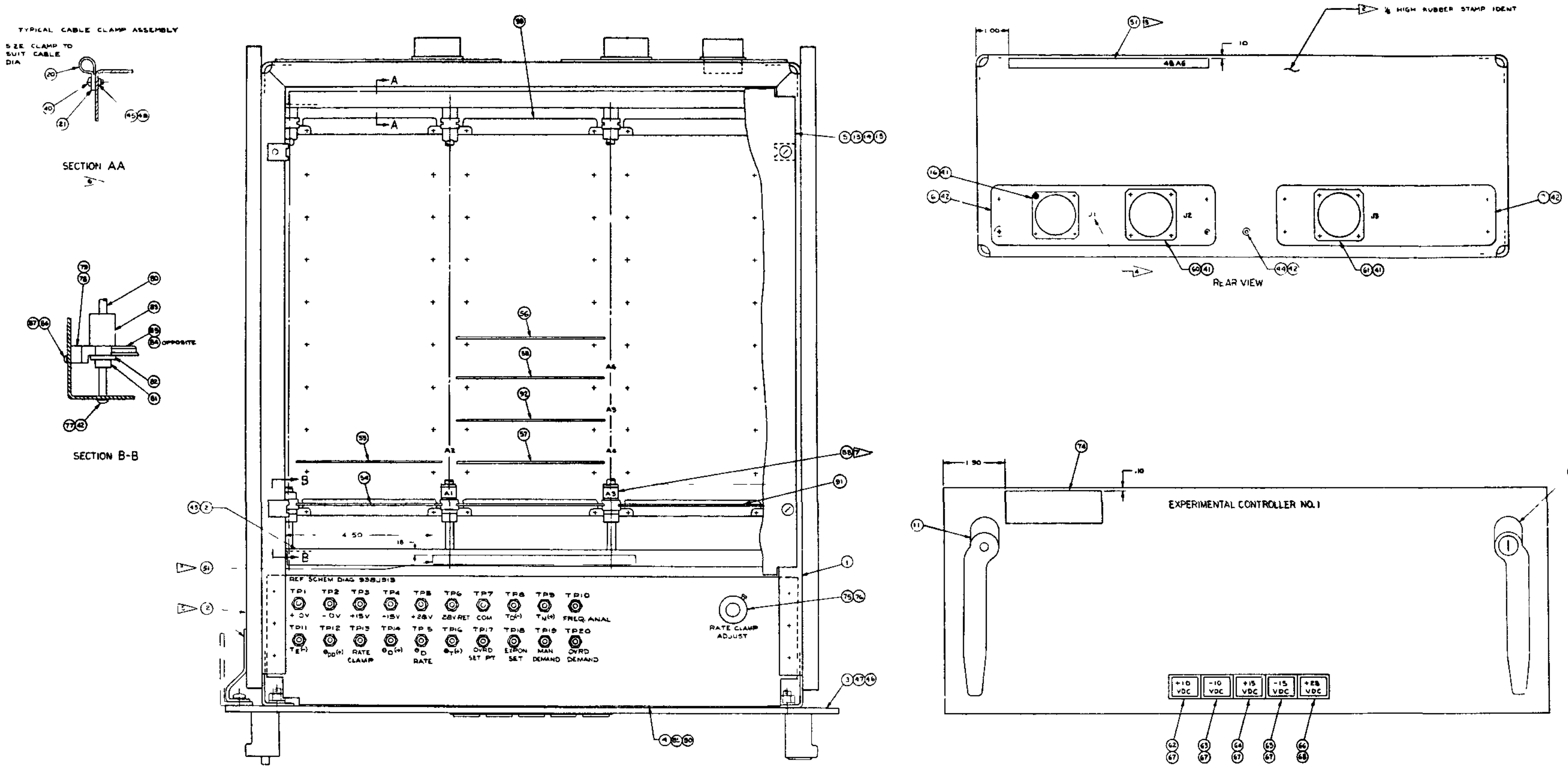
Westinghouse Astronuclear Laboratory
Pittsburgh, Pennsylvania

STANDARD BUFFER AMPLIFIER

CODE IDENT NO. 14683 | DWG. NO. 910E318

SIZE E | SCALE 2/1 | WT ACT — WT CALC — | SHEET 1 OF 1

Drawing 5
910E318
Standard Buffer Amplifier



TOP VIEW

FRONT VIEW

TP CHART

ITEM	TEST POINT
69	TP1 TP3 & TP5
70	TP2 & TP4
71	TP7
72	TP6
73	TP8 THRU TP20

NOTES

7. APPLY IDENT TAG ITEM 88 TO SPACER PER REFERENCE DESIGNATION AS SHOWN.
6. IF ADDITIONAL CABLE CLAMPS (ITEM 20) ARE REQUIRED AT OTHER THAN THE STANDARD LOCATIONS PROVIDED DRILL A .159 ± .005/.000 DIA HOLE AND SECURE CLAMP WITH ITEMS 2, 40 45 AND 48
5. ALL HARDWARE TO ASSEMBLE SLIDES AND BRACKETS TO CHASSIS AND CABINET IS FURNISHED WITH ITEM 12.
4. RUBBER STAMP REFERENCE DESIGNATIONS AS SHOWN IN .12 HIGH BLACK INK CHARACTERS OVER SPRAY WITH CLEAR LACQUER
3. SUFFIX OF IDENTIFICATION TAG ITEM 51, TO BE AS SHOWN
2. GROUP 1 (G01) IDENTIFIED BY 938J912G01
1. INTERPRET SYMBOL IN L/M SYMBOL COLUMN AS FOLLOWS V=VENDOR ITEM L=ITEM STOCKED BY CONTROL SYSTEMS LAB, N=ITEM STOCKED BY NERVA STORES

F1 938J912 REV SH 1 NR

LIST OF MATERIALS

G01 QTY REQD	SYM	ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO.	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
1		92	RELAY MODULE, 4PDT		979D576G02			
1		91	EXTENDER, PC BOARD 35 PIN		979D182G02			
4	N	90	SCREW, PAN HD .138 X 1.00 LG		MS35206-234			
4	V	89	SPACER .25 DIA X .62 LG	06540	9230-A 40 16			
6		88	TAG, IDENTIFICATION		947C086H03			
60	N	87	WASHER, LOCK, INTERNAL TOOTH .112		MS35333-36			
60	N	86	SCREW PAN HD, .112-40 X .62 LG		MS35206-218			
30	N	85	CARD GUIDE	13910	B 306-45XR			
30	N	84	CARD GUIDE	13910	B 306-45XL			
72	N	83	CARD SPACER	13910	B-102-1000			
16	N	82	CARD SPACER	13910	B-102-125			
16	N	81	SPACER STOP	13910	B-302			
8	N	80	SIDE ROD	13910	B 901 13 625			
AR	N	79	INSERT, POLARIZING	91662	50 5006 3414			
29	N	78	CONNECTOR, RECEPTACLE	91662	00 7008 035-163 001			
16	N	77	WASHER, LOCK, INTERNAL TOOTH .164		MS35333-38			
1	V	76	DIAL, 15 TURN	80740	2606			
1	V	75	POTENTIOMETER, 500 Ω	80294	3500S-2-501			
1		74	NAMEPLATE		964B163H01			
13	L	73	JACK, TIP, WHITE		MS16108-1A			
1	L	72	JACK, TIP, BLACK		MS16108-3A			
1	L	71	JACK, TIP, BROWN		MS16108-4A			
2	L	70	JACK, TIP, ORANGE		MS16108-6A			
3	L	69	JACK, TIP, RED		MS16108-2A			
	V	68	FUSE, 1A, 250V		F02B250V1AS		MIL-F-15160/02	
4	V	67	FUSE, 1/2A, 250V		F02B250V1/2AS		MIL-F-15160/02	
1		66	FUSE, DRIVEN IND, +28V DC		979D442G07			
1		65	FUSE, DRIVEN IND -15V DC		979D442G04			
1		64	FUSE, DRIVEN IND, +15V DC		979D442G03			
1		63	FUSE, DRIVEN IND, -10V DC		979D442G02			
1		62	FUSE, DRIVEN IND, +10V DC		979D442G01			
1	V	61	CONNECTOR, RECEPTACLE	77820	PT02A-22-55PW			
1	V	60	CONNECTOR, RECEPTACLE	77820	PT02A-22-55P			
1		59	GROUNDING MODULE		979D181G02			
1		58	RELAY MODULE, 4PDT		979D576G01			
1		57	COMPARATOR/RELAY DRIVER		910E312G01			
1		56	BUFFER AMPLIFIER, STANDARD		910E318G02			
1		55	TEMP CONTROLLER		910E315G01			
1		54	TEMP ERROR		910E314G01			

LIST OF MATERIALS

G01 QTY REQD	SYM	ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO.	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
AR	L	53	LACQUER, SPRAY		13 OZ			
AR	L	52	INK, BLACK (37038)				TT-I-558	
6		51	TAG, IDENTIFICATION		947C086H04			
AR	L	50	FERRULE, SHIELD GROUNDING		MS25311-20			
AR		49	FERRULE, SHIELD GROUNDING		MS25311-30			
AR	N	48	NUT HEX .138 [illegible]		MS35649-262			
4		47	NUT HEX .250 [illegible]		[illegible]			
[illegible]	N	46	WASHER LOCK INTERNAL TOOTH [illegible]		MS35333-40			
AR	N	45	WASHER LOCK INTERNAL TOOTH .138		[illegible]			
[illegible]		44	TERMINAL LUG [illegible] .164		[illegible]			
14		43	SCREW [illegible]		MS24693-C272			
25		42	SCREW PAN HD [illegible]		[illegible]			
12		41	SCREW PAN HD [illegible]		[illegible]			
AR	N	40	SCREW PAN HD [illegible]		[illegible]			
AR		39	CABLE 2 C SHIELD, AWG 16	06090	44/42 [illegible]			
AR		38	WIRE, AWG 16 POLYALKENE [illegible]		M81044 [illegible]		MIL-W-81044/4	
AR	N	37	AWG 20 VIO		20-7		MIL-W-81044/4	
AR	N	36	GRN		20-5			
AR		35	RED		2			
AR		34	YEL		[illegible]			
AR		33	BLU		[illegible]			
AR	N	32	BLK		[illegible]			
AR	N	31	OR		20-3			
AR	N	30	BR		2			
AR	N	29	[illegible]		20-94			
AR	N	28	WHT/RED		20-92			
AR	N	27	[illegible]		2 97			
AR	N	26	WHT BLU		96			
AR	N	25	[illegible]		93			
AR	N	24	AWG 20 WHT/BRN		[illegible] 91		[illegible]	
AR	V	23	AWG 20 WHT/RED	06090	[illegible]			
AR	N	22	WIRE, AWG 24 POLYALKENE WHT		81044/[illegible] 24 9		MIL-W-81044/4	
AR	L	21	WASHER [illegible]	[illegible]	TYPE [illegible]			
AR	L	20	CLAMP CABLE	55987	TYPE [illegible]	NYLON		
AR	L	19	TUBING SHRINKABLE	[illegible]	[illegible] 3 32			
AR	L	18	TAPE LACING FLAT		TYPE P	NYLON	[illegible]	
AR	L	17	SOLDER		TYPE R	60SN	QQ-S-571	
	V	16	CONNECTOR RECEPTACLE	[illegible]	PT02A 20 [illegible]			
8	L	15	RECEPTACLE, CLIP ON	94222	[illegible] 47-191 15			
8	L	14	RETAINER	94222	60 2-93			
8	L	13	FASTENER, 1/4 TURN	94222	2-5-200			
	N	12	SLIDE CHASSIS, PR	06175	AT 2FN 20 2			
	N	11	HANDLE LEFT HAND	06666	HP-0			
1	N	10	HANDLE RIGHT HAND	06666	[illegible] (HP 0-MOD)			
X		9	WIRING DIAGRAM		938J914			
X		8	SCHEMATIC DIAGRAM		938J913			
		7	PLATE CONNECTOR		976D443G03			
		6	PLATE, CONNECTOR		976D443G02			
2	N	5	COVER, CHASSIS		928F727H01			
		4	PANEL COMPONENT		980D976G01			
		3	FRONT PANEL		928F981G01			
		2	PLATE, COMPONENT		910E316G01			
		1	FRAME, CHASSIS		909E953G01			

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

909E771G01	XE-1 (CCS)	T7 1889	TEST
NEXT ASSY	USED ON	[illegible]	IDENT
B APPLICATION		SPECIFICATION	TYPE
DWG CODE NO	1	0751588 BS	NE1538

UNLESS OTHERWISE SPECIFIED
INTERPRET DWG PER [illegible]
TOLERANCES - DO NOT SCALE
2PL DEC | 3PL DEC | ANGLES

INFORMATION CATEGORY: Unclassified

CONTRACT NO NP-1
DRAWN P TIETZ
CHECKED M J D

Westinghouse Astronuclear Laboratory
Pittsburgh, Penna.

EXPERIMENTAL CONTROLLER NO. 1

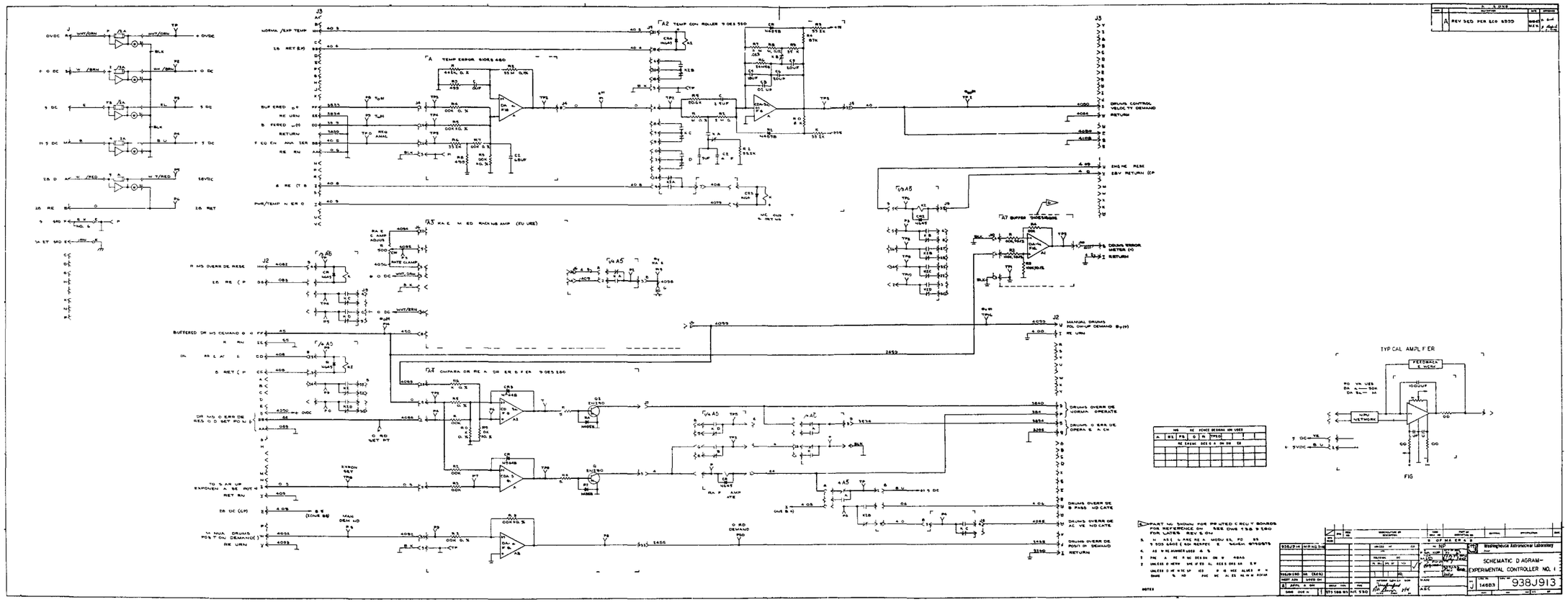
DWG SIZE J | CODE IDENT NO 14683 | DWG NO 938J912

F2

Drawing 6

938J912

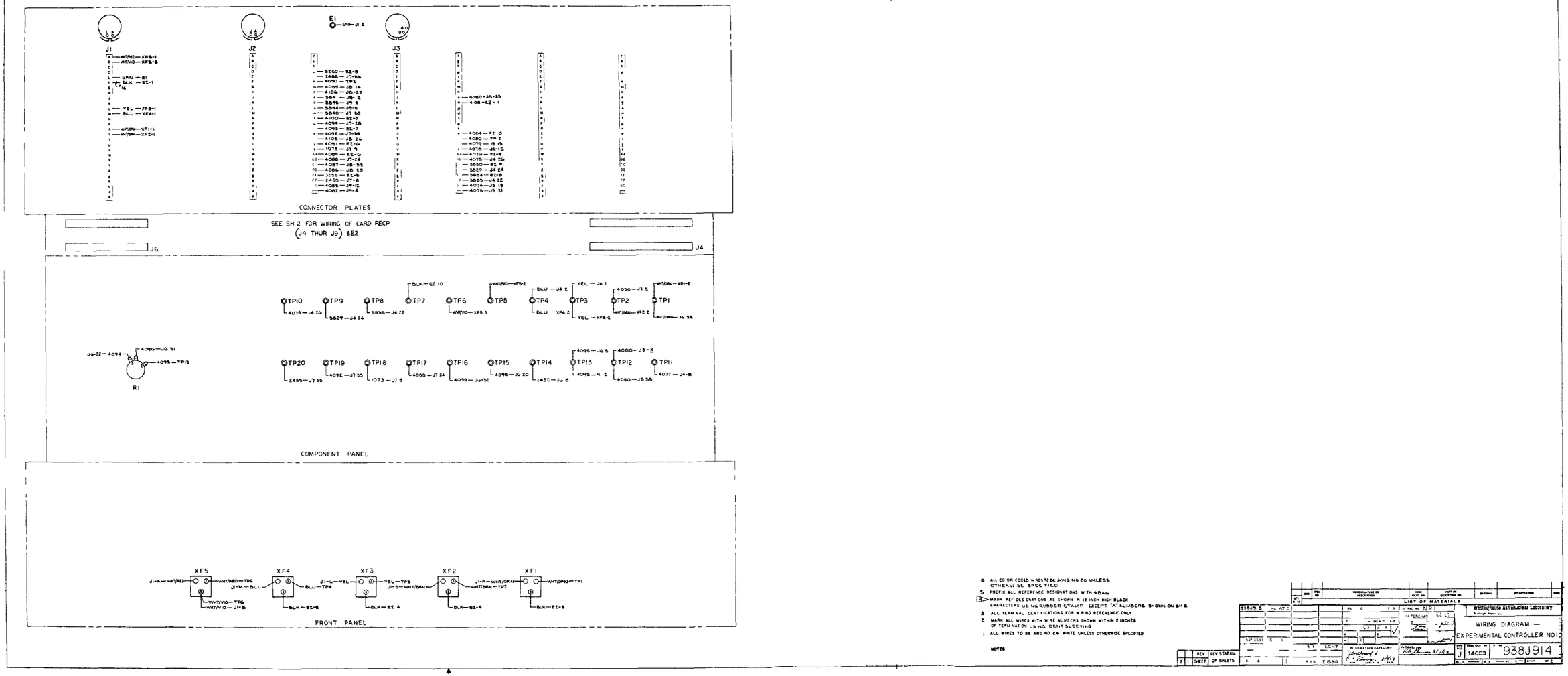
Experimental Controller No. 1



Drawing 7

938J913

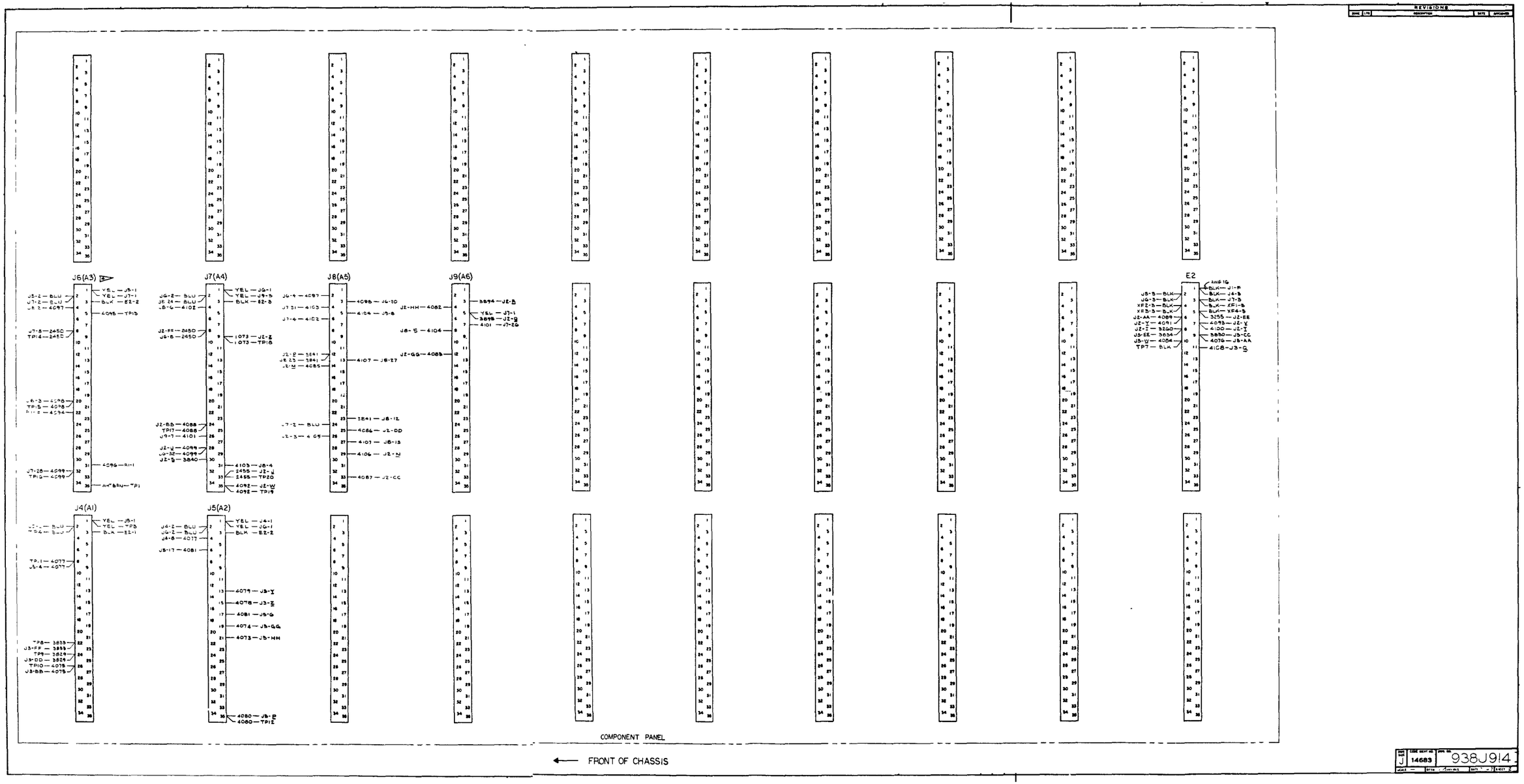
Schematic Diagram - Experimental Controller No. 1



Drawing 8

938J914

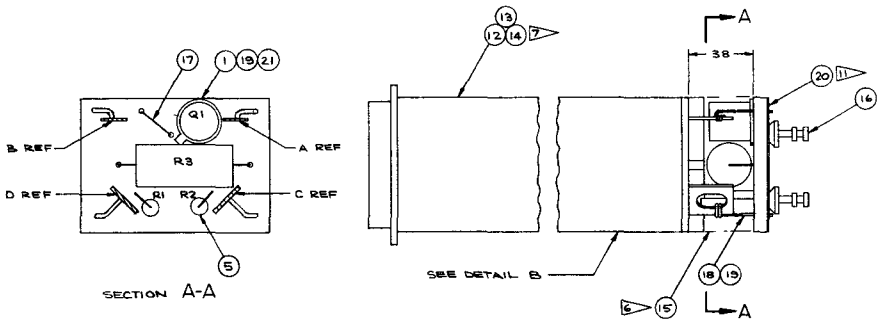
Wiring Diagram - Experimental Controller No. 1
(Sheet 1)

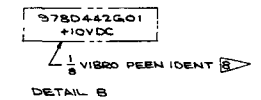


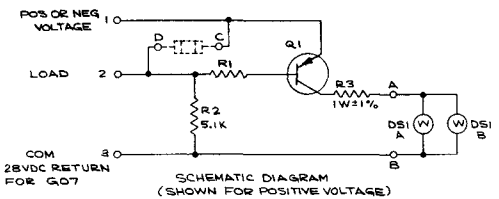
Drawing 8

938J914

Wiring Diagram - Experimental Controller No. 1
(Sheet 2)







SCHEMATIC DIAGRAM (SHOWN FOR POSITIVE VOLTAGE) SEE TABLE A FOR TYPE AND VALUE OF Q1, R1, AND R3

TABLE A

GROUP	ITEM NO. Q1	R1	R3	VOLTAGE
G01	3	4	9	+10VDC
G02	2	4	9	-10VDC
G03E	3	6	10	+15VDC
G04E	2	6	10	-15VDC
G05	3	7	11	+16VDC
G06	2	7	11	-16VDC
G07	3	8	18	+28VDC
G08	2	8	18	-28VDC
G09	3	8	18	+24VDC
G10	2	8	18	-24VDC

13 MFD BY CHICAGO MINIATURE LAMP WORKS, CHICAGO, ILL OR EQUAL

12. MFD BY G.C. ELECTRONICS CO., ROCKFORD, ILL OR EQUAL

11 SPRAY ETCHED SIDE OF ITEM 1 WITH INSULATING MATERIAL (ITEM 20). COATING TO BE APPROXIMATELY .003 THICK.

10 MFD BY MASTER SPECIALTIES CO, GARDENA, CALIF, OR EQUAL

9 MFD BY MOTOROLA INC, PHOENIX, ARIZ, OR EQUAL

8 GROUP 1 (G01) IDENTIFIED AS SHOWN. GROUP 2 (G02) TO GROUP 7 (G07) SEE TABLE A FOR NOMENCLATURE.

7 FUSE IS NOT SUPPLIED WITH THIS UNIT.

6 FILL ENTIRE CAVITY BETWEEN FUSEHOLDER AND PRINTED CIRCUIT BOARD WITH SILICONE RUBBER ITEM 15.

5 MFD BY USECO-LITTON, ENGLEWOOD CLIFFS, N J OR EQUAL.

4 MFD BY GENERAL ELECTRIC CO, WATERFORD, N Y OR EQUAL

3 MFD BY ALPHA WIRE CORP, NEW YORK, N Y OR EQUAL

2 MFD BY WARD-LEONARD ELECTRIC CO, MT VERNON, N Y OR EQUAL

1 UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS, ±5%, AND ALL RESISTORS ARE 1/4W

NOTES:

REVISIONS

ZONE	SYM	DESCRIPTION	DATE	APPROVED
	A	CHANGED PER ECO No. 13078	4-6-66 U F Hauley	A-6 GC B P O Dwng Adm 9-27-66
	B	CHANGED PER ECO 13096	4-26-66 U F Hauley	
	C	CHANGED PER ECO 13559	U F Hauley 8 9 66 PT	9-7-66
	D	CHANGED PER ECO 13676	8 29-66 M E H	9-13-66
	E	CHANGED PER ECO 15583	M E H 9 12 67	9-15-67

LIST OF MATERIALS

G10	G09	G08	G07	G06	G05	G04	G03	G02	G01	SYM	ITEM NO.	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
AR	AR	AR	AR	AR	AR	AR	AR	AR	AR	3	21	SHRINKABLE TUBING	FIT-221-6			
AR	AR	AR	AR	AR	AR	AR	AR	AR	AR	12	20	RESIN, INSULATING	5123			
AR	AR	AR	AR	AR	AR	AR	AR	AR	AR		19	SOLDER	TYPE R	60SN	QQ-S-571	
AR	AR	AR	AR	AR	AR	AR	AR	AR	AR		18	WIRE, AWG NO 20 BARE	TYPE S		QQ-W-341	
AR	AR	AR	AR	AR	AR	AR	AR	AR	AR		17	WIRE, AWG NO 24 BARE	TYPE S		QQ-W-341	
3	3	3	3	3	3	3	3	3	3	5	16	TERMINAL	7030-B			
AR	AR	AR	AR	AR	AR	AR	AR	AR	AR	4	15	SILICONE RUBBER	RTV-11			
2	2	2		2							14	LAMP, 28V, 04A	MS25237-327			
			2		2	2	2	2	2	13	13	LAMP, 6V, 04A	345			
1	1	1	1	1	1	1	1	1	1	10	12	FUSE, IND UNIT	70E-A1-F(W)-J1			
				1	1					2	11	RESISTOR, 130Ω 1W±1%	TYPE 1X			
						1	1			2	10	,82±2W±1%	TYPE 2X			
								1	1	2	9	,43Ω,1W±1%	TYPE 1X			
1	1	1	1								8	,30K,¼W±5%	RC07GF303J		MIL-R-11/8	
				1	1						7	,10K,¼W,±5%	RC07GF103J			
						1	1	1			6	,8.2K,¼W ±5%	RC07GF822J			
1	1	1	1	1	1	1	1	1	1		5	,5.1K,¼W,±5%	RC07GF512J			
								1	1		4	RESISTOR, 2K, ¼W ±5%	RC07GF202J		MIL-R-11/8	
1	1		1		1		1		1	9	3	TRANSISTOR	2N2907			
1	1	1	1	1	1	1	1	1	1	8	2	TRANSISTOR	2N2222			
1	1	1	1	1	1	1	1	1	1		1	PRINTED CIRCUIT BOARD	544C768H01			

QUANTITY REQUIRED — CODE 1

UNLESS OTHERWISE SPECIFIED: INTERPRET DWG PER MIL-D-1000 DIM IN INCHES BASED ON 8F; TOLERANCES — DO NOT SCALE; 2PL DEC ±.02; 3PL DEC ±; ANGLES ±

CONTRACT NO NP-1

DRFTM J C Brown 10-12-65

CHECKER 12-20-65

DESIGN 12-20-65

ANALYSIS

MATL

SPEC SUPV 12-20-65

Westinghouse Astronuclear Laboratory, Pittsburgh, Pennsylvania

FUSEHOLDER, DRIVEN INDICATOR

P294517-1 | IDENT — | SPECIFICATION D-SPEC 751588-AT | TYPE NE2270 | INFORMATION CATEGORY | AUTHORIZED CLASSIFIER | DATE

DWG SIZE D | CODE IDENT NO. 14683 | DWG NO. 979D442

SCALE 4/1 | WT ACT — | WT CALC — | SHEET 1 | OF 1

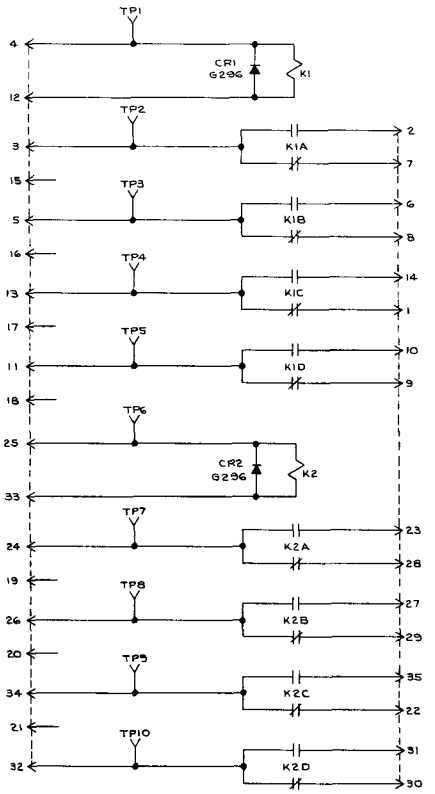
Drawing 9

979D442

Fuseholder, Driven Indicator

Astronuclear Laboratory

WANL-TME-1704



REVISIONS

ZONE	SYM	DESCRIPTION	DATE	APPROVED

LIST OF MATERIALS

QTY REQD	SYM	ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO.	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE

UNLESS OTHERWISE SPECIFIED
INTERPRET DWG PER MIL-D-1000
DIM IN INCHES BASED ON 68°F
TOLERANCES — DO NOT SCALE
FRACTIONAL ± | 2PL. DEC ± | 3PL. DEC ± | ANGLES ±
MATL | DFT SUPV 3 30-66

CONTRACT NO. NP-1
DFTR R WALKUP 3-15-66
CHECKER
ENGR
MFG
ANALYSIS

Westinghouse Astronuclear Laboratory
Pittsburgh, Pennsylvania

SCHEMATIC DIAGRAM—
RELAY MODULE, 4PDT 2 UNIT

979D575 XE-1 (ECS)
NEXT ASSY | USED ON
APPLICATION
DWG. CODE NO | SPECIFICATION | TYPE
751586 BD | NE1500

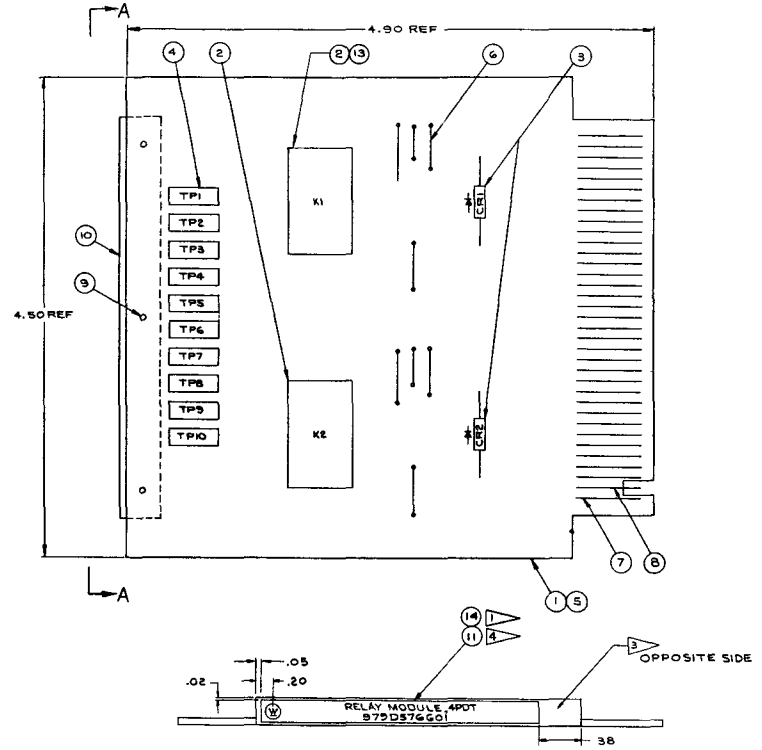
INFORMATION CATEGORY
AUTHORIZED CLASSIFIER | DATE

DWG SIZE D | CODE IDENT NO 14683 | DWG NO 979D575
SCALE — | WT ACT — | WT CALC — | SHEET 1 OF 1

Drawing 10

979D575

Schematic Diagram, Relay Module 4PDT



VIEW A-A
(ROTATED 90° CW)

REVISIONS			
ZONE	STR	DESCRIPTION	DATE	APPROVED
	A	REVISED PER ECO 14078	7-17-67 Roberts	
	B	REVISED PER ECO 14990	8-2-67 M.E.H.	
	C	REVISED PER ECO 15008	6-15-67 M.Crow	
	D	REVISED PER ECO 15020	7-14-67 M.Crow	

QUANTITY REQ'D		STR	ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO.	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
1			14	TAG, CARD IDENT		979D576H14			
1		V	13	RELAY, 4PDT (13-28VDC)	01526	3SAH5005F1			
XX	XX		12	SCHEMATIC DIAGRAM		979D575			
	1	1	11	TAG, CARD IDENT		979D576H11			
1	1		10	HANDLE		947C333HC1			
3	3	N	9	RIVET, .094 DIA X .312 LG		MS20470A3-6			
17	17	N	8	CONTACT, UPPER TIER	91662	7001.0513			
18	18	N	7	CONTACT, LOWER TIER	91662	7001.1513			
AR	AR	L	6	WIRE, AWG NO 20, BARE		TYPE S		QQ-W-343	
AR	AR	L	5	SOLDER		TYPE R	60SN	QQ-S-571	
10	10	V	4	TEST JACK, WHITE	78947	111437-A			
2	2	V	3	DIODE		1N645			
1	2	V	2	RELAY, 4PDT (20-34VDC)	01526	3SAH5005K1			
1	1		1	PRINTED CIRCUIT BOARD		928F423H01			

LIST OF MATERIALS

4 ITEM 11 WORDED AS SHOWN
ITEM 14 - RELAY MODULE, 4-PDT/979D576G02

3 APPLY WANL SERIAL NO WITH INDELIBLE INK OR MARKING ENAMEL

2 INTERPRET SYMBOL IN L/M SYMBOL COLUMN AS FOLLOWS
V = VENDOR ITEM
L = ITEM STOCKED BY CONTROL SYSTEMS LAB
N = ITEM STOCKED BY NERVA STORES

1 MAKE FROM 946C08GH12 LETTERING TO BE WHITE ON BLACK BACKGROUND

NOTES .

938J081G01	XE 1(ECS)		
NEXT ASSY	USED ON		
B APPLICATION		SPECIFICATION	TYPE
DWG. CODE NO.	1	751588-BD	NE1500

UNLESS OTHERWISE SPECIFIED
INTERPRET DWG PER MIL-D-1000 FOR W PCBS BASED ON SET
TOLERANCES — DO NOT SCALE
SPL. DEC. ±.02 | SPL. DEC. ± | ANGLES ±
INFORMATION CATEGORY
AUTHORIZED CLASSIFIER 3/11/66 DATE

CONTRACT NO. NP-1
DRN. R.WALKUP DATE OF DWG. 3-10-66
CHECKER
DESIGN
MATL.
APPD.
DATE

Westinghouse Astronuclear Laboratory
Pittsburgh, Pennsylvania

RELAY MODULE, 4PDT 2 UNIT

SIZE D | CODE IDENT NO. 14683 | DWG. NO. 979D576
SCALE 2/1 | WT ACT — | WT CALC — | SHEET 1 | OF 1

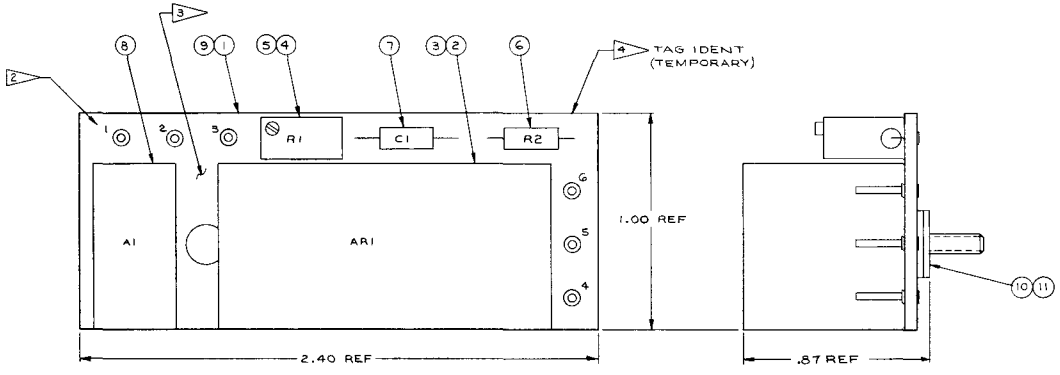
Drawing 11

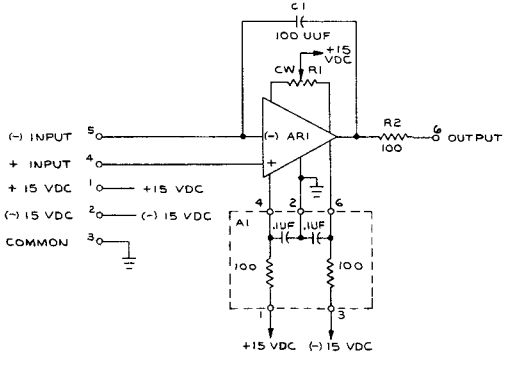
979D576

Relay Module 4PDT

Astronuclear Laboratory

WANL-TME-1704





SCHEMATIC DIAGRAM

4 TEMPORARY TAG IDENT 980D916G01 FOR GROUP 1, 980D916G02 FOR GROUP 2.

3 APPLY WANL SERIAL NO. WITH INDELIBLE INK OR MARKING ENAMEL.

2 TERMINAL NUMBERS ARE FOR REFERENCE ONLY.

I INTERPRET SYMBOL IN L/M SY 480L COLUMN AS FOLLOWS
V = VENDOR ITEM N = ITEM S OCKED BY NERVA STORES
L = ITEM STOCKED BY CONTRC. SYSTEMS LABORATORY

NOTES

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED PER ECO IS004	6/14/67	6-16-67

LIST OF MATERIALS

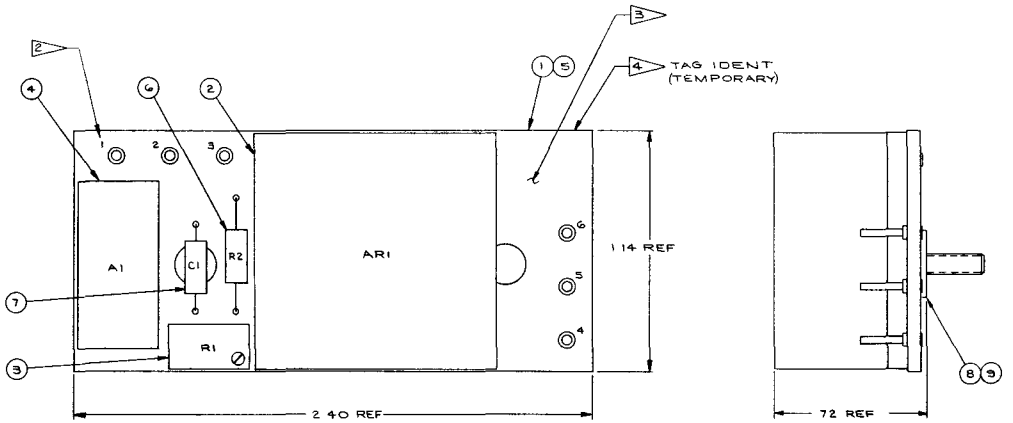
QTY. REQD		STR	ITEM NO	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO.	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
4	4	V	11	WASHER, FLAT, PLASTIC	04868	3IN-030-128			
AR	AR	L	10	ADHESIVE	74364	TYPE 910			
AR	AR	L	9	SOLDER		TYPE R	60 SN	QQ-S-571	
1	1		8	FILTER MODULE, AMPLIFIER		980D917G01			
1	1	V	7	CAPACITOR, 100 UUF, 200V, ±10%	72259	DC-101K			
1	1	V	6	RESISTOR, 100 OHMS, ¼W, ±5%		RC07GF101J		MIL-R-11/8	
1	1	V	5	POTENTIOMETER, 50K, ½W, ±20%	80294	3281W-1-503			
1	1	V	4	POTENTIOMETER, 1 MEG, ½W, ±20%	80294	3281W-1-105			
1	1	V	3	AMPLIFIER, D CASE	17276	CDA-3a			
1	1	V	2	AMPLIFIER	17276	DA-1a			
1	1		1	PRINTED CIRCUIT BOARD		980D915G01			

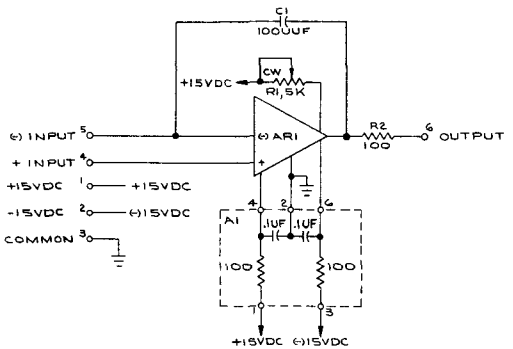
				UNLESS OTHERWISE SPECIFIED	CONTRACT NO.	NP-1	Westinghouse Astronuclear Laboratory		
				INTERPRET DWG PER MIL-D-1000 DIM IN INCHES BASED ON .00?	DRFTR. W. F. Hanley	DATE OF DWG 2-17-67	Pittsburgh, Pennsylvania		
				TOLERANCES — DO NOT SCALE	CHECKER M.J.D.	REVISED, D.O.R. 6/14/67	STANDARD OPERATIONAL AMPLIFIER SERIES 2		
				2PL. DEC ± / 3PL. DEC ± / ANGLES ±	DESIGN E. J. Wyrick	STRESS			
					ANALYSIS	MATL.			
	XE-1 (ECS)	T-711883	TEST						
NEXT ASSY	USED ON	P294517-1	IDENT	INFORMATION CATEGORY	WANL		DWG SIZE D	CODE IDENT NO. 14683	DWG. NO. 980D916
B APPLICATION		SPECIFICATION	TYPE		AUTHORIZED CLASSIFIER	DATE	SCALE 4/1	WT ACT —	WT CALC —
DWG CODE NO	1	0751588-8R	NE 1530		AEC			SHEET 1	OF 1

Drawing 12

980D916

Standard Operational Amplifier





SCHEMATIC DIAGRAM

4 TEMPORARY TAG IDENT 980D922G01.

3 APPLY WANL SERIAL NO WITH INDELIBLE INK OR MARKING ENAMEL.

2 TERMINAL NUMBERS ARE FOR REFERENCE ONLY.

1 INTERPRET SYMBOL IN L/M SYMBOL COLUMN AS FOLLOWS
V = VENDOR ITEM N = ITEM STOCKED BY NERVA STORES
L = ITEM STOCKED BY CONTROL SYSTEMS LABORATORY

NOTES

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED PER ECO 15003	5 31 67	TWB Y&RLV

QTY REQD	SYM	ITEM NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT NO.	PART OR IDENTIFYING NO.	MATERIAL	SPECIFICATION	ZONE
2	V	9	WASHER, FLAT, PLASTIC	04865	3IN-030-128			
AR	L	8	ADHESIVE	74364	TYPE 910			
1	V	7	CAPACITOR, 100UUF, 200V, ±10%	72259	DC-101K			
1	V	6	RESISTOR, 100 OHMS, 1/4W, ±5%		RC07GF101J		MIL-R-11/8	
AR	L	5	SOLDER		TYPE R	60SN	QQ-S-571	
1		4	FILTER MODULE, AMPLIFIER		980D917G01			
1	V	3	POTENTIOMETER, 5K, 1W, ±5%	80294	3280W-1-502			
1	V	2	AMPLIFIER DIFFERENTIAL	95023	PP25A			
1		1	PRINTED CIRCUIT BOARD		980D920G01			

LIST OF MATERIALS

928F957G01	XE-1(ECS)		
910E307G01	XE-1(ECS)	T-711683	TEST
NEXT ASSY	USED ON	P234517-1	IDENT
B	APPLICATION	SPECIFICATION	TYPE
DWG. CODE NO	1	D751588 BR	NE1530

UNLESS OTHERWISE SPECIFIED
INTERPRET DWG PER MIL-D-1000 DIM IN INCHES BOARD OR SKY
TOLERANCES — DO NOT SCALE
2PL. DEC ±, 3PL. DEC ±, ANGLES ±, AA

CONTRACT NO. NP-1
DRFTM P. WALKUP 2-16-67
CHECKED MJD
DESIGN
ANALYSIS
MATL
STRESS
INFORMATION CATEGORY
AUTHORIZED CLASSIFIER DATE
WANL
AGC

Westinghouse Astronuclear Laboratory
Pittsburgh, Pennsylvania

OPERATIONAL AMPLIFIER-
SERIES 2

DWG SIZE D | CODE IDENT NO. 14683 | DWG. NO 980D922
SCALE 4/1 | WT ACT — | WT CALC — | SHEET 1 OF 1

Drawing 13

980D922

Operational Amplifier

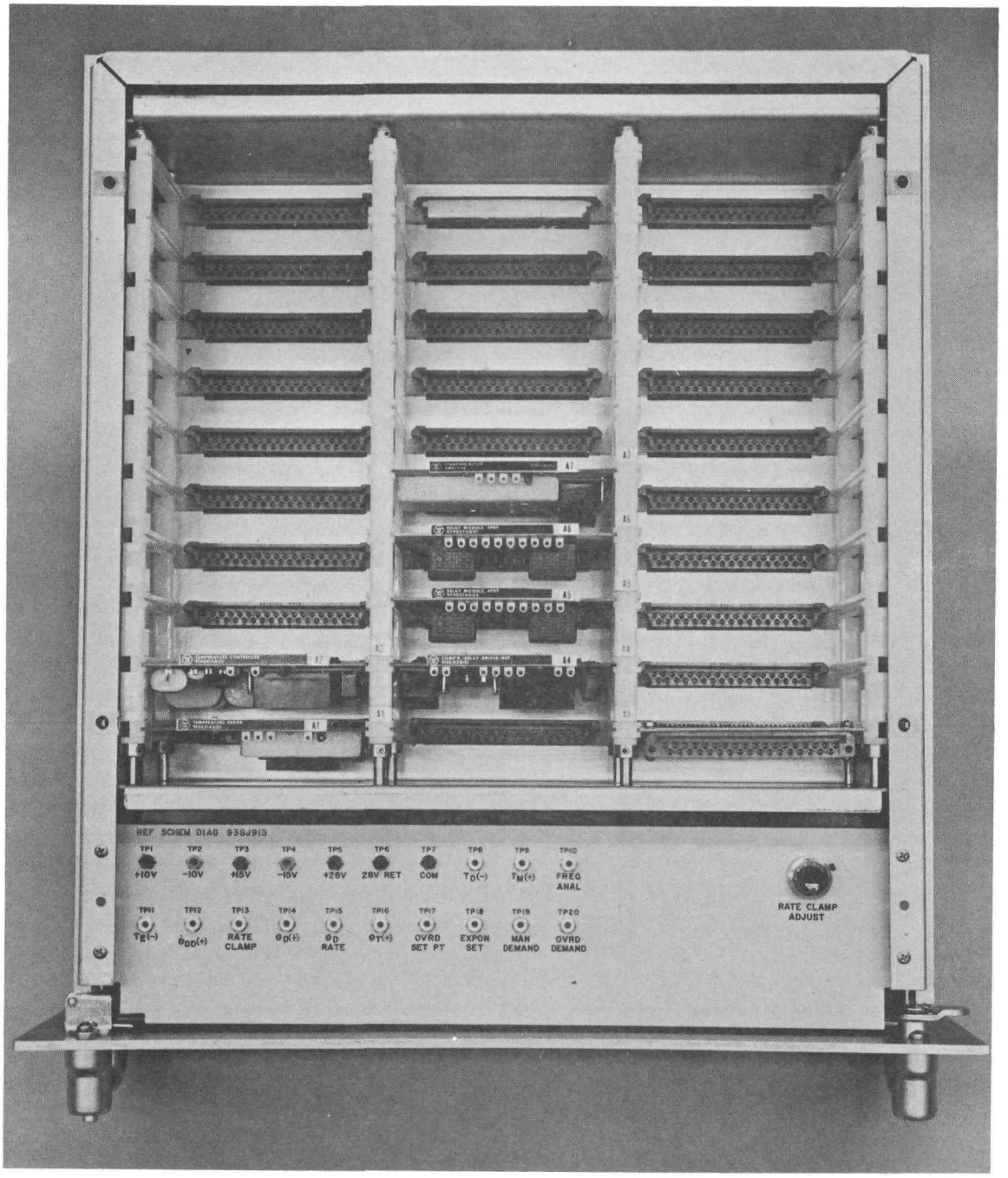


Figure 1

Experimental Controller No. 1

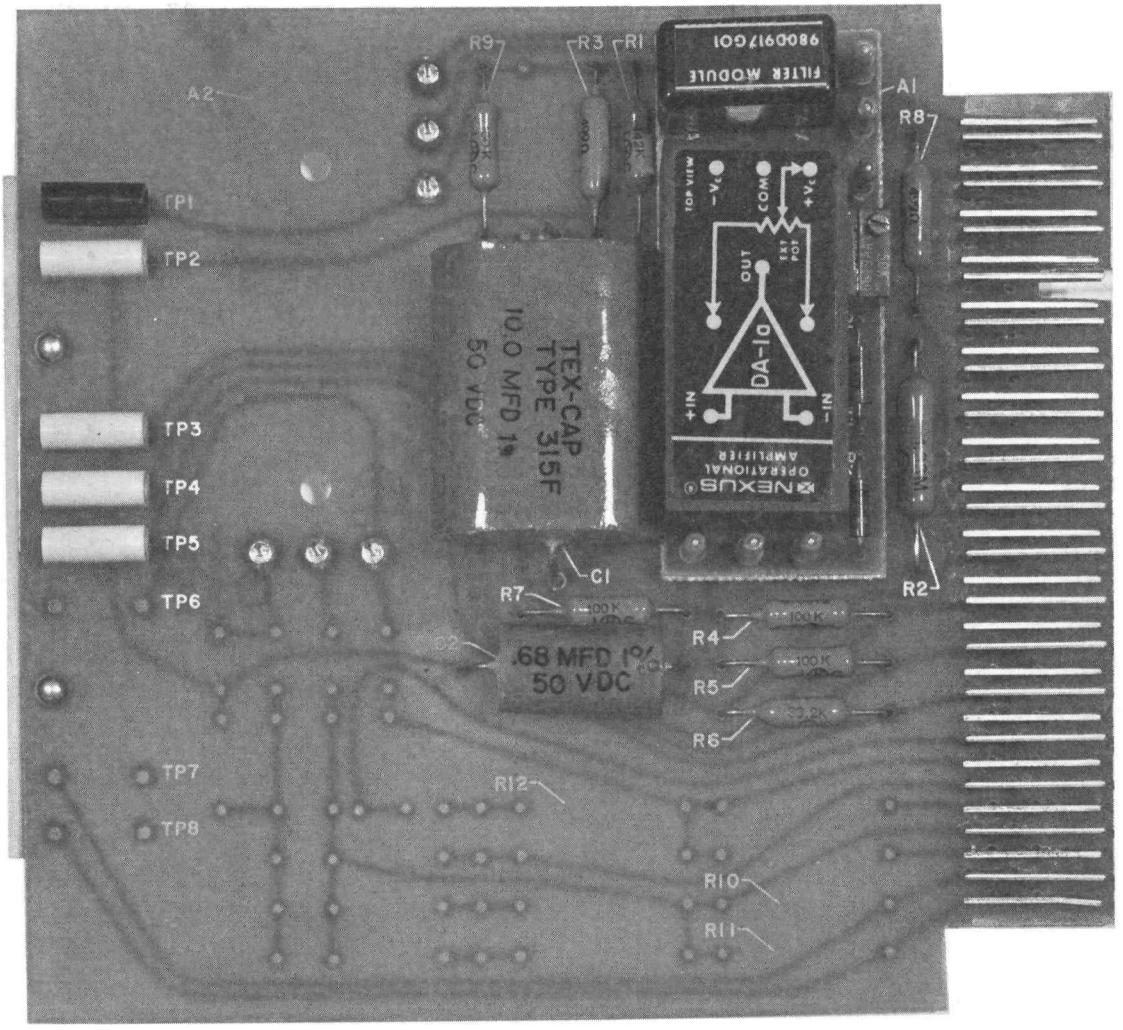


Figure 2

Temperature Error Amplifier

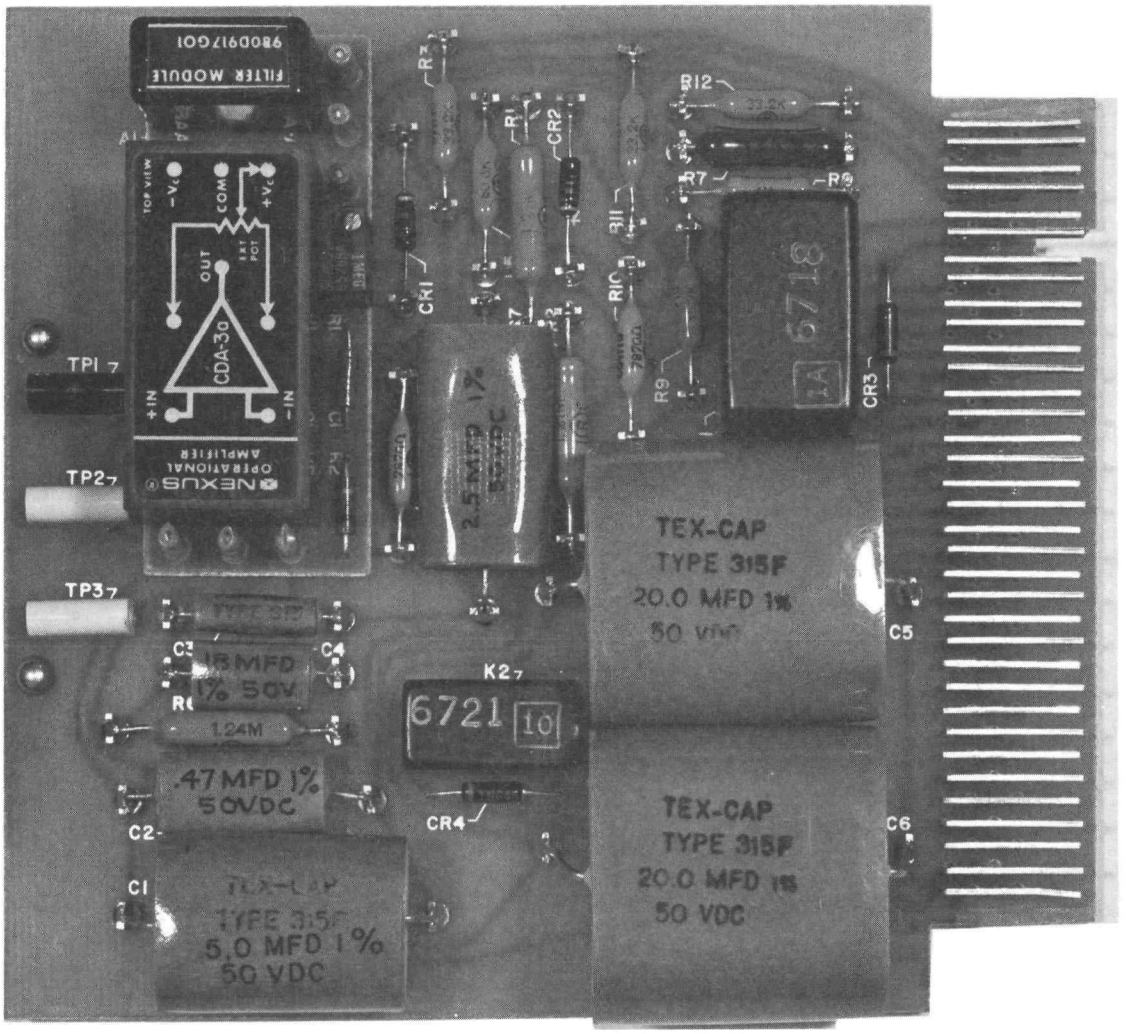


Figure 3

Temperature Controller

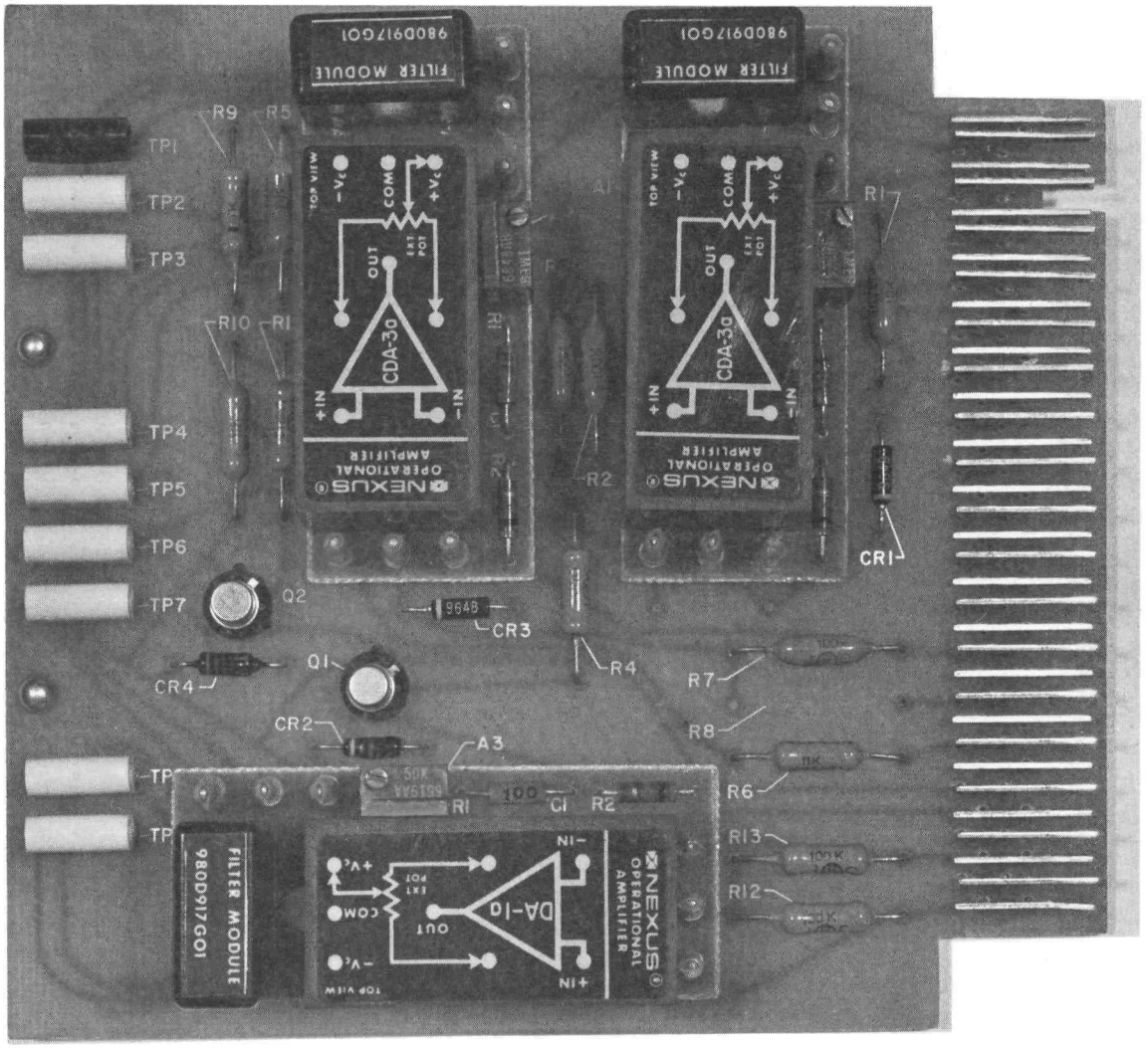


Figure 4

Comparator/Relay Driver/Buffer

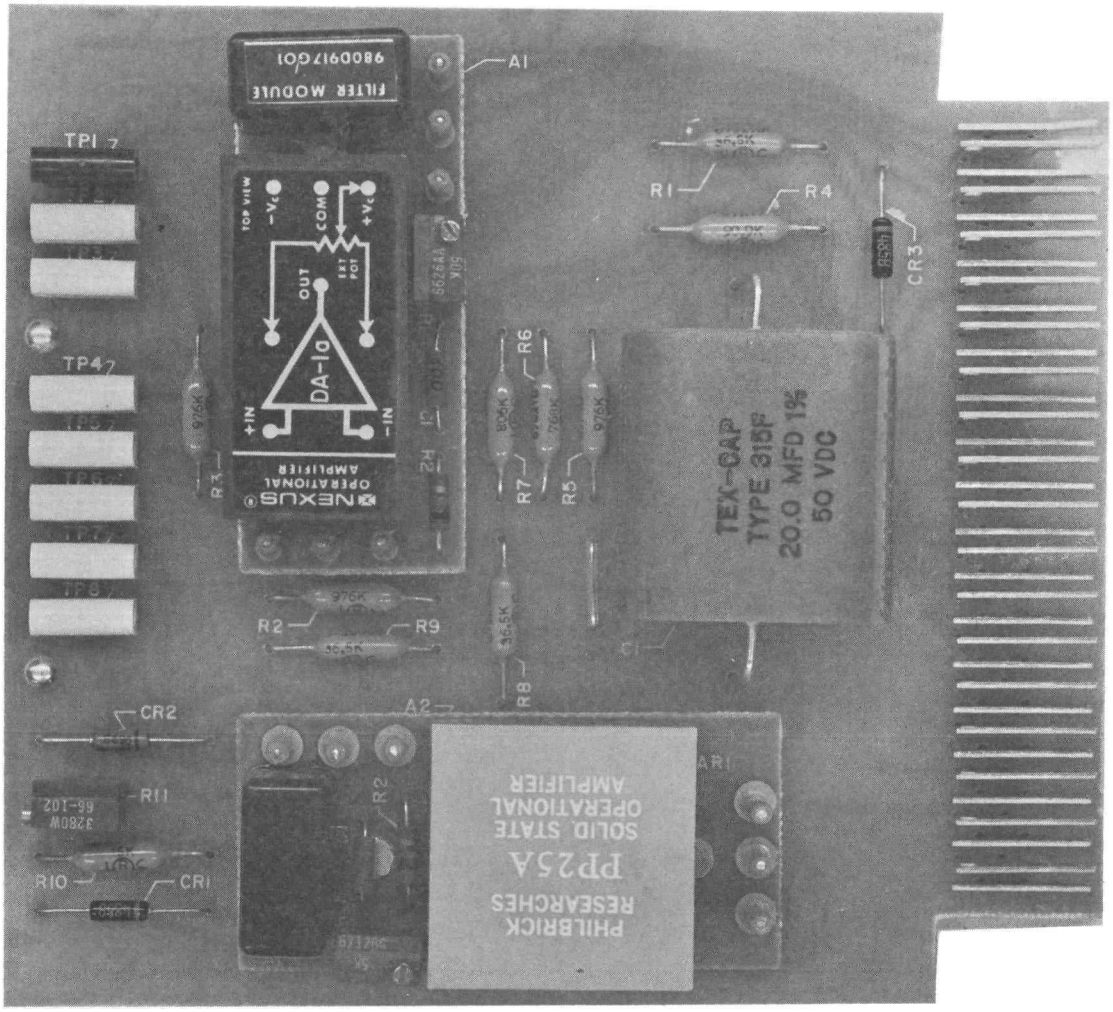


Figure 5

Rate Limited Tracking Amplifier

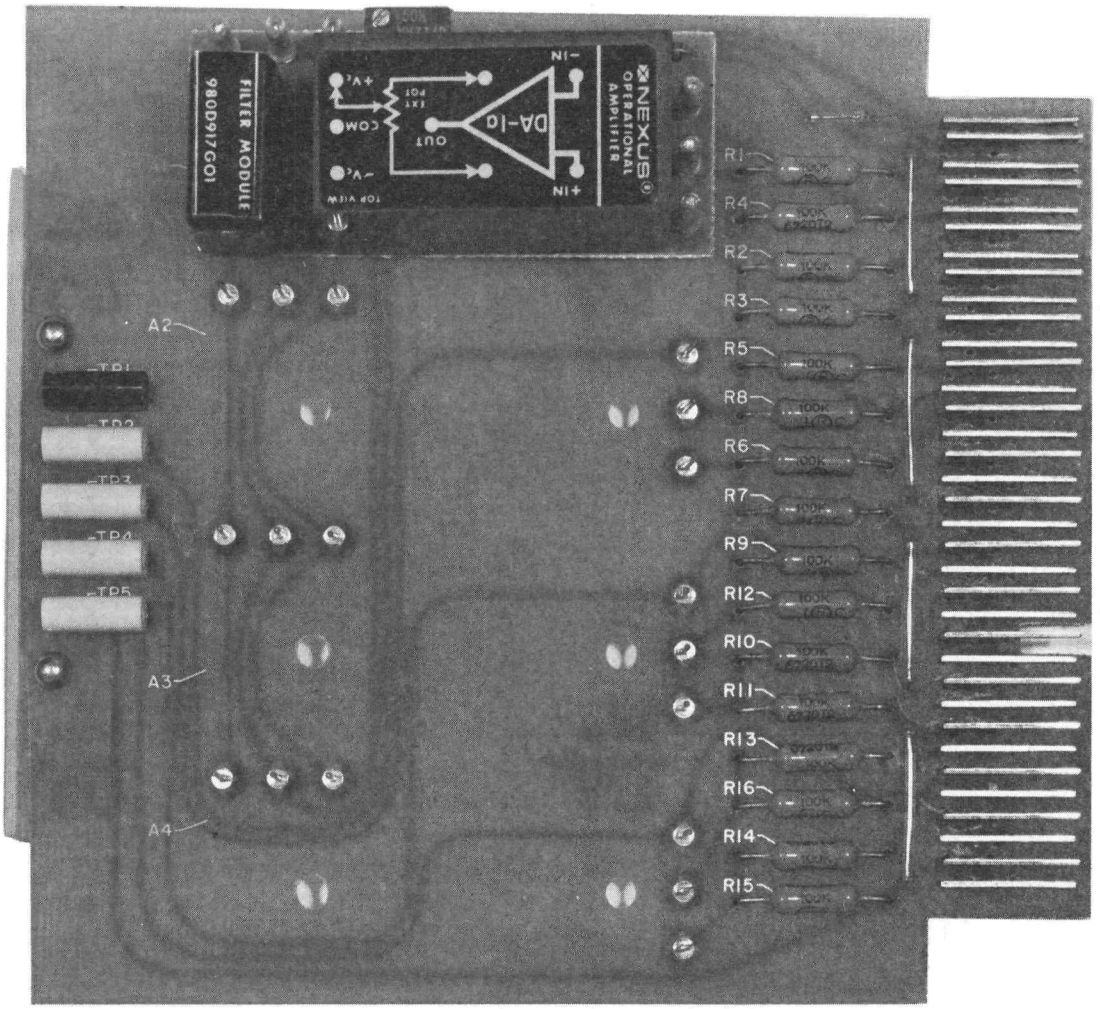


Figure 6
Buffer Amplifier

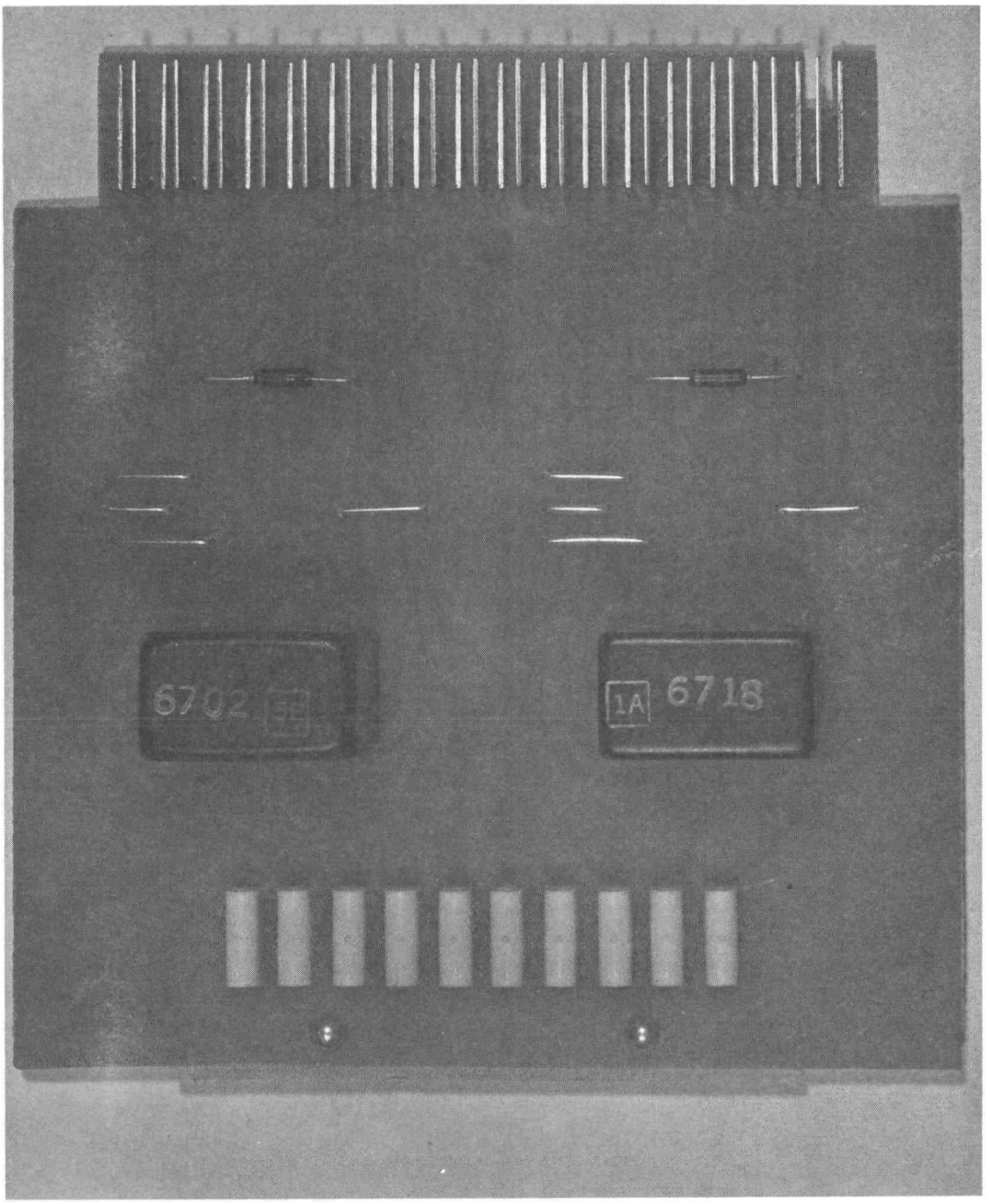


Figure 7
Relay Module