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Engineering
and Equipment

MASTER

AN AUTOMATIC LINEAR VARIABLE DIFFERENTIAL
TRANSFORMER (LVDT) CALIBRATOR (U)

H. H. Cromwell
W. W. Lee

UNION CARBIDE CORPORATION
NUCLEAR DIVISION
OAK RIDGE Y-12 PLANT

operated for the ATOMIC ENERGY COMMISSION under U. S. GOVERNMENT Contract W-7405 eng 26

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ABSTRACT

Calibration of linear variable differential transformers (LVDT) has been automated using a small digital computer. The computer controls external equipment, takes data, and performs calculations. Use of this computer reduces the calibration time from approximately two hours to approximately two minutes.

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SUMMARY

A system for automatically calibrating a linear variable differential transformer (LVDT) employs a small digital computer and an optical interferometer. The interferometer is used to measure displacements. Interfacing circuits enable the computer to control external equipment and track armature displacement. The computer contains an analog-to-digital converter which reads the LVDT output voltage while the armature is moving. Finally, appropriate software performs mathematical operations on the data and types the results on a teletype.

Calibration time is reduced from approximately two hours to approximately two minutes. Tests indicate that total uncertainty in the output is ± 0.08 percent at the 95 percent confidence level.

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INTRODUCTION

Manually certifying the linearity of a linear variable differential transformer (LVDT) is a very time-consuming operation. The null position, or lowest voltage point, must be located, the armature precisely displaced from this reference, and the amplified output voltage recorded at twenty-six preselected points throughout the gaging range. To eliminate nonlinearity in the voltage amplifier, a precision ratio transformer must be substituted for the LVDT. The ratio-transformer switch settings required to obtain the same output voltage as the LVDT at each datum point must be recorded. Finally, mathematical operations must be performed on these data to determine LVDT linearity. This entire process takes approximately two hours.

The system discussed in this report uses a digital computer to automate this operation. The time involved is reduced to approximately two minutes.

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DISCUSSION OF THE CALIBRATOR

DESCRIPTION

The automated calibration system can certify LVDT's having an excitation frequency of five or ten kilocycles, excitation voltages from one through seven volts, rms, and gaging ranges from 0.005 through 0.25 inch. These data are loaded into the computer from a binary coded perforated tape. A front view of the facility is presented in Figure 1 and a block diagram of the system is shown in Appendix A.

The computer^(a) performs seven basic functions: (1) sets the excitation supply; (2) controls the fixture travel; (3) operates the ratio transformer; (4) sets the amplifier gain, polarity, and input; (5) tracks the LVDT armature displacement; (6) measures the voltage; and (7) calculates the linearity. The first four functions are accomplished by device selector circuits which decode the computer's accumulator register, memory buffer register, and input-output pulses to operate relays and solenoids. These operations result in a specific computer command to operate a particular device. For instance, the excitation voltage is set by one of these commands (STFE = 6703) according to the contents of Bits 9, 10, and 11 of the accumulator. These three bits actuate relays in a matrix forming a digital potentiometer which divides the excitation supply output down to precisely the required voltage.

LVDT armature displacement is measured with an optical interferometer. The interferometer signals are decoded and connected to the computer's "interrupt" and "skip" busses. This connection results in a pulse to the interrupt bus at each 1/4 fringe, or 3.125 microinches of displacement, and a logic level on the skip bus to indicate direction. An appropriate subroutine uses this information to increment or decrement an internal storage register in tracking displacement.

The computer contains an analog-to-digital converter (ADC) for measuring voltage. This component makes it possible to convert an analog voltage to a digital number for use in calculations.

Calculations to determine LVDT linearity from the resulting data are performed in double-precision, floating-point arithmetic. These calculations are performed using software supplied with the computer and specially written programs.

To perform these operations, the LVDT is connected to the computer system. The excitation voltage, excitation frequency, and gaging range data are read into the computer from a paper tape. The computer then types out the format on the teletype,

(a) Model PDP-5, manufactured by the Digital Equipment Corporation.

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Figure 1. AUTOMATIC LVDT CALIBRATION FACILITY.

sets up the excitation supply, and starts the fixture moving forward at approximately 1/4 inch per minute. The following is a sample of an output format:

M-2345
DATE: 9-8-66
REQ: A. J. JOHNSON
MFR: SHEFFIELD
FREQ: 5 KC
VOLT: 3V
RANGE: 20 MIL
LINEARITY: 00.76%

The signal from the LVDT is amplified and synchronously rectified. The computer ADC monitors this signal as the fixture displaces the LVDT armature. When the output voltage goes to zero volt, the computer accepts interferometer count pulses through the computer interrupt and skip busses. This null point is used as a displacement reference. When the number of interferometer pulses indicates a displacement of fifty-five percent of the total gaging range, the computer takes an

ADC reading and multiplies the amplifier gain by a factor of two or four if needed to produce between five and ten volts output. If this is not possible, the computer will indicate a high or low gain condition on the teletype, and the gain must be reset manually. The fixture is then moved in the reverse direction while the computer monitors displacement. After the armature has moved to fifty-five percent of the total gaging range on the opposite side of the null point, the fixture is again driven forward; ADC readings are taken at the prescribed displacements and stored in the computer. The prescribed data points in percent of total gaging range and in reference to the null position are as follows: -55, -50, ..., -5, -2.5, -1.25, +1.25, 2.5, 5, ..., 50, and 55. When these data have been taken, the fixture travel is automatically reversed to get into position for the next LVDT.

The amplifier input is automatically transferred to the output of a precision, relay-operated, eighteen-bit ratio transformer.^(b) The ratio transformer has the same excitation as the LVDT and is used to obtain a proportional representation of the LVDT data independent of amplifier linearity. Using the successive approximation method, the computer actuates relays in the ratio transformer, takes an ADC reading of the output voltage, and compares it with the ADC reading obtained from the LVDT. In this manner, each LVDT voltage reading is replaced by a ratio-transformer word.

Next, the computer converts these ratio-transformer words to normalized floating-point numbers and from these calculates a least-squares line passing through zero. The deviation of each datum point from this line is then calculated and stored as a percentage of the first datum point. Maximum deviation is typed on the teletype^(c) as the LVDT linearity; the deviation at each point may be listed if desired.

MAJOR SUBSYSTEMS

A detailed description of each major subsystem is presented in the sections that follow. Schematics and modules appropriate to these subsystems are included in Appendix B.

Computer System

The computer system consists of the Model PDP-5 computer, interface, teletype, and associated software. The PDP-5 is a small digital computer using twelve-bit, two's-complement arithmetic. It has a 4096-word random address magnetic core memory with a six-microsecond cycle time.

(b) Model BRT-383A, manufactured by Gertsch Products, Inc.

(c) Model 33-ASR, manufactured by the Teletype Corporation.

Accumulator input (AC) and output (BAC), memory buffer (MB), skip bus (IOS), program interrupt bus, input-output pulses (IOP), and data-break signal lines are brought out to an interface connector. External circuits wired into this interface and appropriate programming enable the computer to control the external equipment.

The teletype is used to transfer information to the computer from the keyboard or perforated tape and to output information from the computer in the form of typed copy or perforated tape. It is used in this system to read in the main program and LVDT data and to type the format and linearity.

The eleven-bit ADC in the computer is used to measure the amplifier output voltage. Range of the ADC is + 10 to 0 to - 10 volts with corresponding octal representations of 0000-4000-7777. A sample-and-hold circuit incorporated in the ADC enables accurate conversion of a time-varying voltage. This feature is used to measure LVDT output while the armature is moving. The PDP-5 Handbook⁽¹⁾ should be consulted for a more detailed description of the computer, teletype, ADC, and interface.

Software for the system consists of programs supplied by the computer manufacturer and those written specifically for this system. The Floating Point Interpretive and I/O package (DEC-5-S-BIN) supplied by the computer manufacturer is used in the calculation process. The binary loader (DEC-5-2-U-RIM) is used to read in programs from perforated tapes. The PDP-5 Programs⁽²⁾ manual contains a detailed description of these programs. Programs written specifically for this system are the operating program (LVDT-OPR) and maintenance program (LVDT-MTN). In addition to the actual programs, two modification tapes and four data tapes were made for the operating program. The modification tapes (LVDT-MAX and LVDT-ALL) change the output mode between maximum deviation only and all-points deviation. The four data tapes (LVDT-D-2-10-10, -2-10-20, -3-10-10, and -3-10-20) contain codes of the four combinations of voltage frequency and gaging range presently in use. Appendix C contains a flow diagram, discussion, and complete listing of each program.

Device Selector

The device selector circuit uses the computer interface to select and operate such components as the relays and solenoids. The circuits are made up of digital plug-in modules located in the DEC^(d) and Delco^(e) card racks. Since interconnections are made by connector pins on the racks, which are located near the top of the cabinet, a faulty module can be easily replaced. Power for the DEC card rack is supplied from a power unit mounted in the rack; power for the Delco rack is supplied from a Delco power unit mounted in the bottom of the cabinet. Connection to the computer

(d) Card rack manufactured by the Digital Equipment Corporation.

(e) Card rack manufactured by the Delco Radio Division, General Motors Corporation.

is by means of a 50-conductor cable which connects into the top right side of the equipment cabinet. (Refer to the manufacturer's data sheets for circuit diagrams and other data concerning individual modules.) The device selector commands along with their octal representations and functions are listed in Appendix D.

The 4605-pulse amplifier and gate cards decode the MB and IOP to generate input-output-transfer (IOT) signals. One of these signals (6711) is used as a strobe in the interferometer count direction circuit. Three others (6721, 6722, and 6724) are used to set and clear two flip-flops which operate two CD301 high-current drivers. These drivers then operate relays in the amplifier gain circuit (discussed later). Four of the remaining five IOT signals (6701, 6702, 6704, and 6714) are used to set four flip-flops while the remaining signal (6712) is a common clear command. The flip-flop outputs are inverted to provide better driving capability. These outputs are fed to the AND gate inputs of thirteen high-current drivers, which generate thirteen distinctive control commands. Three of these commands are not used in the system but were decoded as spares. Nine of the remaining drivers operate relays directly which are used in other circuits. The AND gate output of the remaining driver is double inverted for isolation and used to drive a complementing flip-flop (4214-2). This flip-flop is independently reset by the AND gate output of the RESET driver. The O output of this flip-flop is fed into another high-current driver which operates the RFRV relay, which is also used in the amplifier circuit.

Interferometer Decoder

The purpose of this circuit is to decode the interferometer amplifier signals such that the computer can measure LVDT armature displacement. The two signals, Channels A and B, from the interferometer amplifier are quadrature sine waves. A particular channel lags or leads the other one depending upon the direction of travel. One complete cycle corresponds to one fringe or approximately 12.5 microinches.

These buffered signals are fed into Schmitt triggers for conversion to square waves. The switching-point offset of the triggers offers protection from noise. The outputs, normal and inverted, of each trigger are fed into one shots whose outputs are connected to an OR gate. The output of this gate is inverted and connected to the computer interrupt bus; thus, a pulse appears at the interrupt bus for each level change of each channel. This level change gives one pulse for each one-quarter fringe. The one shots are set for a pulse width of approximately fifty microseconds enabling the computer to acknowledge the interrupt. This pulse takes care of indicating displacement intervals, but it gives no indication of direction. The logic circuit near the bottom of the schematic (Appendix B, Figure B-16) is used to indicate direction. Corresponding outputs of the Schmitt triggers are used as inputs to the two NAND gates. Outputs of the NAND gates are connected to an OR gate to indicate whether the interferometer signals are at the same or different logic levels. This output and its complement are used as one input to two more NAND gates. The other input of each gate comes from the output of two gates connected to form a

set-reset flip-flop. Inputs to the flip-flop are the one-shot pair output of each channel. Finally, outputs of the two NAND gates are connected to an OR gate to produce the direction logic level. Table 1 shows the input and output states of this circuit.

Table 1
INPUT AND OUTPUT STATES OF THE
INTERFEROMETER CIRCUIT

Transition	Input Levels	Output	
		Direction Signal	Displacement Direction
A	Same	Positive	FWD
B	Opposite	Positive	FWD
A	Opposite	Negative	REV
B	Same	Negative	REV

The direction signal is fed to the computer IOS bus by means of another NAND gate and a strobe signal (6711) from the device selector circuit. Thus, the computer tracks displacement by receiving an interrupt signal at each 3.125-microinch interval and producing a programmed strobe to determine the direction of travel. These displacement intervals are counted by appropriately incrementing or decrementing an internal storage register.

Signal Amplifier and Control

The LVDT amplifier system consists of four basic parts: (1) a wide-band preamplifier, (2) a push-pull phase-reference system, (3) a synchronous-chopper demodulator circuit, and (4) an output filter and DC amplifier.

The preamplifier system incorporates three feedback-stabilized differential amplifiers (DOA) which are capacitor coupled. The coupling condensers are chosen so that they pass five and ten-kc signals but attenuate 60 cycles. These plug-in amplifiers are contained in the right-hand chassis. A relay gain-set matrix for X1, X2, or X4 automatic gain adjustment from the computer and a front panel switch for manual gain adjustment are also enclosed in the chassis. Normal output level is about two volts, rms, full scale.

The synchronous rectifier consists of two transistor choppers in parallel with a DC differential amplifier wired so that the alternate inputs produce an average DC output proportional to the phase X magnitude products of the AC signal from the preamplifier.

Reversal of the reference phase will provide polarity reversal at the DC-ampere output; hence, balance of the circuit may be accomplished by reversing the reference phase and comparing the absolute magnitude of the DC output.

The phase-reference system takes a reference voltage from the power source and converts this to a ten-volt, rms, push-pull chopper-drive signal. Provisions are made to flip the reference-voltage phase 180 degrees by either a front panel switch or through relay actuation (RFRV) from the computer. This unit uses a solid-state amplifier^(f) to generate balanced opposite-phase outputs to drive the synchronous rectifier.

The output filter system consists of a constant K, 1.2-kc filter which removes all AC components above 1.2 kc to reduce ripple and allow instantaneous readings. Settling time of this filter for transients is particularly important when using the circuit to compare LVDT output with the ratio transformer. Hence, the circuit was selected, not for maximum attenuation of a five and ten-kilocycle ripple, but for the best combination of ripple filtering and transient response. The output transient for a step change in the AC voltage level lasts about 3 1/2 to 8 milliseconds. The output amplifier^(f) (needed to supply ± 10 volts to the computer) is set for a voltage gain of about 2 1/2.

Fixture and Control

Figure 2 shows the fixture mechanism used to hold the LVDT in place and to move its armature. The laser^(g) and interferometer are also mounted on the fixture base plate. The base plate is used to provide a solid base for the driver-interferometer-laser combination.

The driving mechanism is an air cylinder which drives a hydraulic resistance device^(h) that incorporates precision micrometer-type check valves for speed control. Air at 60 psi provides the power to operate the driver and valves. The air is switched on and off by solenoid-actuated valves in the fixture control unit. This unit is mounted in the rear of the cabinet, as shown in Figure 3. A shaft mounted in a bearing seat is used to couple the driver movement to the LVDT armature.

The fixture control circuit consists of three latching relays and four solenoid-actuated valves. Three of the valves are controlled by the latching relays. These relays are actuated individually by corresponding relays in the device selector circuit, and all

(f) Model P65A, manufactured by the George A. Philbrick Researches, Inc.

(g) Laser, Model 119, and the Laser Power Supply, Model 259B, manufactured by Spectra-Physics.

(h) Hydro-Check, SBDA-PSTS-50-20, manufactured by Bellows-Valvoir.

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Figure 2. FIXTURE USED TO HOLD THE LVDT IN PLACE AND TO MOVE ITS ARMATURE.

three are wired such that actuation of any one resets the other two. The FXI device-selector relay drives the corresponding solenoid valve directly. The indexing mechanism is not presently used.

Oscillator and Power Amplifier

The oscillator and power amplifier⁽ⁱ⁾ are used as the excitation source for the LVDT and ratio transformer. Good stability, low harmonic distortion, and pushbutton frequency selection are provided. Frequency is selected by a 3 by 10 pushbutton-switch array which is easily actuated by air-driven plungers.

(i) Oscillator, Model LDS-446R, and Power Amplifier, Model LDS-103R, manufactured by the Krohn-Hite Corporation.

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Figure 3. EQUIPMENT RACK. (Rear View)

AC Decoder and Buffer

The circuit used to decode and buffer the accumulator output (BAC) signals consists mainly of three groups of high-current drivers with NAND gate inputs. The two groups of nine drivers have accumulator (AC) bits, 0 through 8, as one input to each gate. The other inputs in each group are connected together to form an inhibit line, which permits one group to be selected at a time. A negative voltage on an

inhibit line prevents that group of drivers from being actuated. Thus, both groups are normally inhibited. Group A is used by the most significant bits of the ratio transformer (described later), and is enabled by the STRT command. The SLRT command drives a latching relay which disables this group and allows STRT to enable Group B, which is used by the least significant bits of the ratio transformer. The SLAVE relay is operated momentarily by SLRT to allow unwanted ratio-transformer relays to drop out before latching.

This circuit is also used as a decoder and buffer for the excitation voltage and frequency select circuit. Group B drivers are also enabled by the STFE command. The first four drivers in this group are used to select the excitation frequency. Excitation voltage is selected by the three drivers in Group C. These drivers are not gated, and their outputs simply follow AC Bits 9, 10, and 11.

Excitation Voltage and Frequency Select System

This circuit is used to automatically select the appropriate excitation for an LVDT. The unit containing this circuit is mounted in the front of the cabinet near the bottom. Solenoid valves, actuated by Bits 0 through 3 of the AC decoder and buffer circuit, set the frequency. These valves switch air at 60 psi to drive plungers which operate pushbuttons on the Krohn-Hite oscillator. For instance, the octal number 4000 in the AC, when the STFE command is given, sets the frequency to ten kilocycles.

Excitation voltage is selected in a similar manner except relays are used. Precision resistors are connected to three latching relays to form a "digital potentiometer". The Krohn-Hite power amplifier, set for a seven-volt output, is used as the input to this voltage divider. An output voltage of one through seven volts in steps of one volt each is selected according to the contents of Bits 9, 10, and 11 of the AC at the time STFE is given. This selection is accomplished by driving the relays with the AC decoder and buffer circuit. The octal number 0003 in the AC, when STFE is given, selects a three-volt output. The latching relays are set for a zero-volt output by the RESET command. Diodes are connected across all coils for noise suppression and in series with all coils for isolation.

Ratio Transformer and Control System

The ratio transformer, located behind the relay panel, is used to develop an AC voltage which gives the same amplifier output as the LVDT. The ratio-transformer input is connected in parallel with the LVDT primary and, thus, receives the same excitation voltage. Relays inside the transformer are connected to form an eighteen-bit switch which is used to divide the input voltage down to an amplitude corresponding to the LVDT output. The relay string is divided into two groups of nine each to facilitate operation with a twelve-bit computer. Each relay coil is connected to a driver in the AC decoder and buffer circuit and is actuated by the STRT

command from the device selector circuit. When this command is given, ratio-transformer relays in the most significant half are actuated according to the contents of Bits 0 through 8 of the AC. This group of relays can be latched in by the SLRT command by grounding one side of the relay coils through their normally open contacts. After latching, the next STRT command causes the least significant group of relays to be actuated according to the contents of Bits 0 through 8 of the AC. Latched relays are released by the ULRT command or the more general RESET command.

PERFORMANCE

The performance of any system is determined by three types of error: gross, systematic, and random. Gross errors in this system include such mishaps as computer malfunction and marginal interferometer balance. While these errors have drastic effects on system performance, they are easily detected. The interferometer balance is displayed on a meter during normal operation, and any unbalance is obvious. Computer malfunction and other gross errors produce a suspiciously high nonlinearity output. Thus, when an error of this type occurs, the output can be disregarded and the equipment repaired or adjusted.

Systematic and random errors determine the accuracy of the system. In this system, the displacement measurements are used as ratios. Hence, the absolute accuracy of a fringe produced by the interferometer does not affect the accuracy of the system. Similarly, use of the ratio transformer prevents the amplifier and ADC linearity from affecting the accuracy of the system.

The ADC incorporates a sample-and-hold circuit which eliminates systematic error due to conversion time in converting a time-varying voltage. These features leave the ratio transformer, which has a maximum nonlinearity of ± 0.011 percent and traceable to the National Bureau of Standards, as the single source of systematic error.

Repeatability of the system is determined by the random errors. Sources of random error and their magnitudes are listed in Table 2.

The percent full-scale values are calculated at the worst case of a five-volt output, five-mil gaging range, and a three-volt excitation. Actual measurements were made on the amplifier output to determine noise and drift characteristics. The ratio transformer has an eighteen-bit switching arrangement with the output divided by six in the amplifier. The resolution in percent full scale is calculated assuming an LVDT full-scale output of ten millivolts.

Two tests were made to determine the overall repeatability. The first test consisted of storing constant data in place of the LVDT data, which has the effect of removing LVDT and interferometer repeatability from the system. Twenty of these constant

Table 2
SOURCES OF RANDOM ERROR

Source	Magnitude	Percent of Full Scale
Stability of Excitation Supply	0.1%	± 0.05 (estimate)
Resolution of Interferometer	$\pm 1/4$ fringe	± 0.03
Resolution of ADC	$\pm 1/2$ LSB	± 0.10
Resolution of Ratio Transformer	$\pm 1/2$ LSB	± 1.01
Amplifier Drift	± 4 mv	± 0.08
Amplifier Noise	± 4 mv	± 0.08

data runs were made, and the standard deviation was calculated as 0.029 percent. The resulting 95 percent confidence interval was 0.023 to 0.043 percent. The 95 percent confidence interval for the mean was $\bar{X} \pm 0.07$ percent.

The second test consisted of checking five LVDT's twenty times each and calculating the standard deviations. During this test, the interferometer balance was kept to within $\pm 1/16$ fringe to reduce the error to less than ± 0.01 percent. The 95 percent confidence intervals for the standard deviations are presented in Table 3.

Table 3
STANDARD DEVIATIONS OBTAINED FROM
REPEATABILITY TESTS

LVDT Identification	Standard Deviation (%)
M-3160	0.059 - 0.113
M-8231	0.045 - 0.085
M-3567	0.058 - 0.110
M-3399	0.043 - 0.082
M-2588	0.060 - 0.114

These data indicate that the repeatability of the equipment is reasonably good compared to the repeatability of the LVDT's checked. It also indicates that the random errors, excluding the interferometer resolution, produced an uncertainty in the output of ± 0.07 percent at a 95 percent confidence level. The uncertainty due to interferometer resolution is ± 0.03 percent maximum. The quadrature addition of these two quantities gives an uncertainty of ± 0.076 percent or approximately 0.08 percent due to random errors.

A good estimate of total uncertainty in the output is obtained by the quadrature addition of the random and systematic errors. As stated previously, the systematic error is ± 0.011 percent maximum. Thus, the total uncertainty in the output is ± 0.08 percent at a 95 percent confidence level.

OPERATION

Prior to operation, the entire system, except the teletype, should be allowed to warm up for at least one-half hour. If the laser power supply has been on standby, this period may be extended to one hour to eliminate frequent adjustment of interferometer balance. In the normal shutdown condition (overnight and weekends), the oscillator-power amplifier combination and the laser power supply should be in standby condition, and the signal amplifier and logic power supplies should be on full. The computer, teletype, and twenty-four VDC power⁽ⁱ⁾ supply should be off. For information concerning the operation of individual units, the appropriate manufacturer's literature should be consulted.

Normally, the operating program will be in the computer. However, if it has been displaced, it must be reloaded from a perforated tape (LVDT-OPR). This tape is in binary (BIN) format and should be loaded according to the procedure described in the PDP-5 Handbook.⁽¹⁾ This program outputs maximum nonlinearity only. However, if the deviation at each checkpoint is desired, a short modification tape (LVDT-MI) can be loaded into the computer; to change back to maximum-point-only output without reloading the entire program, another short modification tape (LVDT-WI) must be loaded. Finally, one of the data tapes for the appropriate voltage, frequency, and gaging range must be loaded.

Next, the LVDT should be connected to the system. The LVDT should be loaded in its holder, as shown in Figure 4, and its cable connected to the appropriate receptacle on the junction box. The LVDT armature should be close to the drive shaft but not touching it.

With appropriate programs in the computer and the LVDT connected, the next step is to perform preliminary checks on the signal amplifier and laser and to adjust for phase shift in the LVDT. Equipment controls are shown in Figure 5.

The procedures for these checks are as follows:

Amplifier Zero

1. Set 1000 in the computer's Switch Register.

(i) SPS-2022-R-VM-AM-RC, Plug-In Instruments, Inc.

120647

Figure 4. LVDT CONNECTION.

2. Press the Load-Address button.
3. Press the Start button.
4. Actuate the amplifier RFRV switch and observe the AC.
5. Adjust the amplifier Zero control until the AC switches between 3776_g and 4002_g when the RFRV switch is actuated.

Amplifier Balance

1. Place the amplifier Gain switch in the Low position.
2. Set 1000 in the computer's Switch Register.
3. Press the Load-Address button.

120645

Figure 5. EQUIPMENT CONTROL PANEL.

4. Set 5000 in the Switch Register.
5. Press the Start button. (The AC should indicate a voltage near nine volts.)

6. Actuate the RFRV switch and observe the AC.
7. Adjust the amplifier balance control until the AC remains constant within 0002 when the RFRV switch is actuated.
8. Press the Stop button.

Laser Balance

1. Set 4300 in the Switch Register.
2. Press the Load-Address button.
3. Press the Start button. (The fixture should drive forward.)
4. Observe the balance meter on the interferometer amplifier and make adjustments if necessary.
5. Press the Continue switch to drive the fixture back to its starting position. (It may be necessary to recycle the fixture. Each time the Continue switch is actuated, direction of travel is reversed.)
6. Press the Stop button.

Phase Shift

1. Place amplifier Gain switch in the Low position.
2. Set 1000 in the computer Switch Register.
3. Press the Load-Address button.
4. Set 0000 in the Switch Register.
5. Press the Start button.
6. Adjust the amplifier Phase control for maximum indication in AC.
7. Press the Stop button.

The equipment is now ready to check the LVDT. Insure that the teletype is on "line" and the tape reader is on "free", set 4000 in the Switch Register, press the Load Address button, and press the Start button. The computer will type the format, check the LVDT, type the results, and stop. To check the same LVDT again without retyping the format, press the Continue switch.

In checking subsequent LVDT's, interferometer balance can be observed on the meter and adjustments made as needed. Amplifier zero and balance should be checked approximately every hour or after changing the excitation frequency. The phase shift should be rechecked when changing LVDT tapes.

A simplified outline of the operating procedure consists of the following steps:

1. Turn equipment on and allow to warm up, if necessary.
2. Load computer tape(s), if necessary.
3. Connect the LVDT.
4. Check and adjust amplifier zero, amplifier balance, interferometer balance, and phase shift, if necessary.
5. Start the computer at Location 4000.

MAINTENANCE

System performance and reliability depend greatly upon periodic checkout and adjustment of the individual units. Thus, the manufacturer's maintenance schedule for these units should be followed closely. Of special importance is the periodic maintenance procedures for the computer-teletype combination described in the PDP-5 Maintenance Manual.⁽³⁾ This equipment, which is the most complex in the system, is used to check out and troubleshoot other units. Detailed maintenance and troubleshooting of standard equipment is left to the manufacturer's literature. System maintenance, troubleshooting, and problem isolation to a subsystem are discussed later along with detailed maintenance of nonstandard units. Refer to the schematics in Appendix B when troubleshooting nonstandard units.

System Troubleshooting

If the system seems to be working improperly, insure that the trouble is actually in the equipment by using an LVDT of known linearity and rechecking switch settings and the operating procedure. If the trouble still persists, it should be isolated to a particular unit and the troubleshooting procedure for that unit performed.

The failure can usually be isolated in a particular subsystem or unit by observing the equipment while attempting to check an LVDT. Isolation in this manner is greatly facilitated by a thorough knowledge of how the system operates and the chronological order the operations follow. Table 4 lists the trouble indications and their probable causes. If isolation in this manner is impossible, each unit must be checked separately until the trouble is located. These units should be checked in the order listed in Table 4.

Table 4
TROUBLESHOOTING GUIDE

Symptom	Probable Cause
1. Computer does not run.	Computer started at wrong location. (1) Computer inoperative.
2. Computer runs but relays do not actuate.	Computer started at wrong location. (1) DC power supply inoperative.
3. Relays operate but fixture does not move.	Fixture already fully forward. (1) Loss of air pressure. Fixture or control system inoperative.
4. Fixture drives forward but does not reverse.	Excitation supply inoperative. Interferometer inoperative.
5. Computer never exits from ratio-transformer sequence.	Part of program lost from memory. (2)
6. Computer does not type linearity.	Teletype inoperative.
7. Output indicates high linearity.	Amplifier not operating properly. Interferometer not operating properly. Computer not operating properly.

(1) Improper operating procedure.

(2) Partial loss of program from memory may give any of the symptoms listed in the table.

Subsystem Troubleshooting

Part of the subsystem troubleshooting is performed with the aid of the computer. Thus, to check these, the maintenance program must be loaded into the computer from a perforated tape (LVDT-MTN). This tape is in a binary format and is loaded according to the procedure described in the PDP-5 Handbook.

DC Power Supplies - These are the -24 VDC supply, Delco rack-power supply, and the DEC rack-power supply. Check out and troubleshoot in accordance with the manufacturer's literature.

Excitation Supply - Check out and troubleshoot the Krohn-Hite oscillator and power amplifier in accordance with the manufacturer's literature.

Computer-Teletype Combination - Check out and troubleshoot this combination in accordance with the manufacturer's literature.

Device Selector System - The computer is used to check out this system. Load the maintenance program (LVDT-MTN), and start the computer at Location 0200. The FXFD relay on the relay panel should actuate, and the computer should halt after typing FXFD. By successively pressing the Continue switch, the other relays should

be actuated. When all the relay panel commands have been generated, END will be typed. This program checks the most complicated part of the device selector circuits.

An oscilloscope or DC voltmeter is needed to check the amplifier gain commands (6721, 6723, 6727). Start the computer at Location 0260. Both the GX2 and GX4 drivers should be off. Pressing the Continue switch should turn the GX2 driver on. Press the Continue switch again to turn both drivers on. The program can be recycled by successively pressing the Continue switch.

To check the interferometer strobe command (6711) or to localize an indicated failure in this circuit, an oscilloscope must be used. Start the computer at Location 0270 with the appropriate octal number in the Switch Register. The computer will generate the command repeatedly and the IOP signal can be traced through the circuit with the scope. A module location decal is attached to the DEC power supply to facilitate module identification. When a module is suspected of being at fault, it should be exchanged with a spare or a like module in another location for confirmation. It should then be repaired or replaced, as necessary.

AC Decoder and Buffer - Load the maintenance program (LVDT-MTN) if it is not already in the computer. To keep from overdriving the amplifier during this test, turn the Amplitude control on the Krohn-Hite power amplifier to zero. Start the computer at Location 0300. All Group A driver outputs should be near zero volt. These outputs are accessible at the Delco terminal strip. Pressing the Continue switch should cause the outputs to switch to -24 VDC. The outputs should reverse at each successive actuation of this switch. Test Group B in the same manner by starting the computer at Location 0320. This operation checks that part of the circuit associated with the ratio transformer.

Before performing the next check, disconnect the air line to the voltage and frequency select chassis to prevent jamming the frequency select switches on the Krohn-Hite oscillator. Start the computer at Location 0340. The outputs of Groups B and C drivers should be near zero volt. Pressing the Continue switch should cause these outputs to switch, as described in the preceding paragraph. This operation checks that part of the circuit associated with voltage and frequency selection. Connect the air line.

Each driver card (CD301) contains four drivers. If any driver does not operate, the associated card should be exchanged with another card to determine whether the trouble is in the driver. If an entire group of drivers is inoperative, the inhibit circuit for that group should be checked.

Fixture and Fixture Control System - Load the maintenance program (LVDT-MTN) and start the computer at Location 0400. The fixture should drive forward. Successive actuation of the Continue switch should cause the fixture to stop or reverse

travel. If the fixture does not operate in this manner, the relays and solenoid valves in the circuit should be checked. Next, the air lines should be checked for air pressure at the appropriate control command. Finally, the air-driven cylinder and hydraulic resistance unit should be checked according to the manufacturer's literature. Mechanical stops on the hydraulic resistance unit should be checked for 1/4-inch full travel and to insure that the drive shaft cannot contact the interferometer mounting bracket.

Interferometer and Amplifier - Load the maintenance program (LVDT-MTN) and start the computer at Location 0500. The fixture will move forward. Successive actuation of the Continue switch will reverse the direction of travel. The fixture must be kept moving during these checks. Check the interferometer and interferometer amplifier system according to the manufacturer's literature. Frequency of the interferometer signals should be between 500 and 1000 cycles per second. The frequency is controlled by check valves on the hydraulic resistance unit and should be approximately the same for both directions of travel.

Interferometer Decoder - Load the maintenance program (LVDT-MTN). Use the computer to move the fixture and observe the Schmitt trigger outputs at the front panel connectors. These outputs should be symmetrical square waves with a 90-degree phase difference. Next, check the count and direction outputs of the circuit. The count output should be 50-millisecond pulses (-3 v to gnd) at four times the frequency of the trigger outputs. The direction output should be a square wave at four times the trigger frequency. When the fixture is moving forward, the direction signal should be at -3 volts for 1/2 cycle after the count pulse appears. When moving in the opposite direction, this signal should be at zero volt for the same period. If the count direction strobe (6711) was not previously checked as described for the device selector, it should be checked now.

Voltage and Frequency Selection System - Load the maintenance program (LVDT-MTN). Connect an AC voltmeter to the LVDT junction box test points, and start the computer at Location 0600. The voltmeters should indicate zero volt. Successive actuations of the Continue switch should set the voltage to 1, 2, ..., 7 volts. The computer will type END when all eight states have been tried. To check frequency selection, start the computer at Location 0640, which should set the frequency to five kilocycles. Pressing the Continue switch successively should change the frequency to between five and ten kilocycles. If improper operation is indicated, the solenoid valves, air system, latching relays, and resistors should be inspected to locate the trouble. If the relay and valve coils are not being energized, the -24 VDC supply and the AC decoder and buffer circuit should be checked.

Ratio Transformer and Control System - Load the maintenance program (LVDT-MTN). Connect an AC voltmeter to the ratio-transformer output and start the computer at Location 0700. The voltmeter should indicate approximately 1.5 volts. Pressing the Continue switch successively should reduce the voltage to 1/2 its previous value

until all eighteen relays have been operated. After all relays have been tried, END will be typed. If improper operation is indicated, the relays and wiring should be inspected. If the relay coils are not being energized, the -24 VDC supply and the AC decoder and buffer circuit should be checked.

Signal Amplifier - Load the maintenance program (LVDT-MTN). An RIDL extender cable is needed to check out and troubleshoot this unit. Input signal for the amplifier is taken from the ratio transformer which is controlled by the computer. Zero and balance are checked as described in the preliminary check-out procedure. If the output will not adjust to zero, check the preamp transfer relay in Unit 1. It should be energized to connect the amplifier input to the ratio transformer. Otherwise, the input is taken from the LVDT which is not necessarily zero volt.

If more than seven millivolts of noise are observed at the output or if the balance program does not set the output to approximately nine volts, excessive unbalance or component failure exists. In this case, an LVDT should be used to generate the input signal. Start the computer at Location 1000 with 0000 in the switch register to transfer the amplifier input to the LVDT. The LVDT armature can be manually displaced to adjust the signal amplitude. The signal should be traced through the amplifier starting with the preamp stages in Unit 3. Gain of each stage is noted on the schematic. The output of Unit 2 should be a full-wave rectified sine wave which changes polarity when the RFRV switch is actuated. If excessive unbalance exists, the amplitudes of the two half cycles will be greatly different. If balance cannot be obtained with the balance control, the two synchronous rectifier transistors must be replaced with a matched pair. All amplifier stages are the modular plug-in type and should be replaced at the slightest provocation to minimize down time.

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REFERENCES

- (1) PDP-5 Handbook, F-55; Digital Equipment Corporation, Maynard, Massachusetts (1964).
- (2) PDP-5 Programs; Digital Equipment Corporation, Maynard, Massachusetts (1964).
- (3) PDP-5 Maintenance Manual, F-57; Digital Equipment Corporation, Maynard, Massachusetts (1964).

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AUTOMATIC LVDT CALIBRATOR

Figure A-1. AUTOMATIC LVDT CALIBRATOR. (Signal Flow Diagram)

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APPENDIX B

SUBSYSTEM DIAGRAMS AND MODULES

Standard logic levels for the digital circuits are 0 and -3 volts for DEC modules and 0 and -6 volts for Delco modules. Delco modules which have inputs from DEC modules are modified for the 0 and -3 volt levels. Logic signal symbols used in these circuits are:

The logic modules are as follows:

<u>Type</u>	<u>Function</u>
151	Diode Gate (Delco)
202	Delay, One Shot (Delco)
205	Schmitt Trigger (Delco)
301	High-Current Driver (Delco)
4106	Inverter (DEC)
4113	Diode Gate (DEC)
4214	Set-Reset Flip-Flop (DEC)
4605	Pulse Amplifier (DEC)

An instrument drawing list is given in Table B-1 and circuit diagrams for the automatic LVDT calibrator are presented in Figures B-1 through B-16.

Figure B-1. AMPLIFIER BLOCK DIAGRAM.

Figure B-2. PDA SCHEMATIC DIAGRAM.

Figure B-3. PHASE DEMODULATOR SCHEMATIC DIAGRAM.

Figure B-4. PHASE DEMODULATOR BLOCK DIAGRAM.

Table B-1
DRAWING LIST FOR THE AUTOMATIC LVDT CALIBRATOR

Figure Number	Title
B-1	Amplifier Block Diagram
B-2	PDA Schematic Diagram
B-3	Phase Demodulator Schematic Diagram
B-4	Phase Demodulator Block Diagram
B-5	Cable Junction Box Schematic Diagram
B-6	Ratio Tran Cable Diagram
B-7	RDPA Schematic Diagram
(1)	Signal Flow Diagram
B-8	Device Selector Logic Diagram
B-9	Interconnection Diagram
B-10	Control and Output Chassis Schematic Diagram
B-11	Schematic Diagram, Model BRT-383AR(2)
B-12	Preamplifier Schematic Diagram
B-13	AC Decoder Logic Diagram
B-14	Exciter and Frequency Selector Schematic Diagram
B-15	Fixture Control Schematic Diagram
B-16	Interferometer Decoder

(1) Appendix A.

(2) Manufacturer's drawing, Gertsch Products Inc. This drawing was revised to show modifications for the automatic LVDT calibrator.

Figure B-5. CABLE JUNCTION BOX SCHEMATIC DIAGRAM.

Figure B-6. RATIO TRAN CABLE DIAGRAM.

Note: All resistors are 1/4W, 5% unless otherwise noted

Figure B-7. RDPA SCHEMATIC DIAGRAM.

Figure B-8. DEVICE SELECTOR LOGIC DIAGRAM.

Figure B-9. INTERCONNECTION DIAGRAM.

Figure B-10. CONTROL AND OUTPUT CHASSIS SCHEMATIC DIAGRAM.

Figure B-11. SCHEMATIC DIAGRAM OF MODEL BRT-383AR.

Note: P1 is module rack and panel connector

Figure B-12. PREAMPLIFIER SCHEMATIC DIAGRAM.

Figure B-13. AC DECODER LOGIC DIAGRAM.

Figure B-14. EXCITER AND FREQUENCY SELECTOR SCHEMATIC DIAGRAM.

Figure B-15. FIXTURE CONTROL SCHEMATIC DIAGRAM.

Figure B-16. INTERFEROMETER DECODER.

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APPENDIX C

COMPUTER PROGRAMS

Introduction

This section contains a discussion, listing, and flow diagram for each computer program. A memory usage chart for the computer is presented in Figure C-1. The maintenance program (LVDT-MTN) and data tapes are treated as single units. However, the operating program (LVDT-OPR), shown in Figure C-2, is divided into subprograms as follows:

<u>Subprogram</u>	<u>Description</u>
CDS	Constant Data Storage Routine
CNVT	Conversion Routine
COMM	Delay Subroutine and Negative Number Array
EXEC	Executive Program
LS	Least-Squares Routine
LST	Least-Squares Control
PCHK	Preliminary Checkout Routine
RATR	Ratio Transformer Routine
TYPOUT	Format and Gain Status Typeout
XINC	Displacement Increment Routine
*	Teletype Output Package
*	Decimal to Binary Conversion

*These routines are standard programs supplied with the computer by the manufacturer.

Constant Data Storage (CDS)

Introduction - This program, diagrammed in Figure C-3 and listed in Figure C-4, stores an array of data with a linearity of approximately 1.25 percent in place of the LVDT data. It is used to check and evaluate the operation of the system.

Requirements - The CDS program occupies Locations 1500 through 1573 in the computer. It also uses the excitation voltage and frequency data and delay subroutine stored in Page zero of the computer memory.

Description - The program is entered manually from the computer console at Location 1500. All latching relays are reset, the amplifier gain is set to the maximum, and the excitation voltage and frequency are selected. The twenty-six constant data

0000 COMM	0200 LS	0400 CNVT	0600
1000 PCHK	1200 RATR	1400 XINC and CDS	1600
2000 DEC-BIN CONVERSION	2200	2400 LINEAR NUMBER ARRAY	2600 DATA STORAGE
3000 TELETYPE OUT- PUT PACKAGE	3200	3400 LST	3600
4000 EXEC	4200 TYPOUT	4400	4600
5000	5200	5400 FLOATING POINT PACKAGE	5600 FP CONT'D
6000 FP CONT'D	6200 FP CONT'D	6400 FP CONT'D	6600 FP CONT'D
7000 FP CONT'D	7200 FP CONT'D	7400 FP CONT'D	7600 RIM-BIN LOADERS

Figure C-1. COMPUTER MEMORY USAGE CHART.

Figure C-2. SUBPROGRAMS OF THE LVDT OPERATING PROGRAM.

Figure C-3. CDS PROGRAM DIAGRAM.

words are stored in the LVDT data locations in Page 15 of the computer memory. Exit from the program is made by a jump to the ratio-transformer program, RATR.

Conversion Routine (CNVT)

Introduction - This routine, diagrammed in Figure C-5 and listed in Figure C-6, converts an octal floating-point number to a four-digit decimal integer in chopped teletype code, which is stored in a three-word location supplied by the calling routine.

Requirements - CNVT and its internal subroutines, SBNC and PRNT, occupy Locations 400 through 546 and the location of the error stop, ERST. It uses Locations 0032 and 0034 for permanent counters.

Description - CNVT expects a positive, normalized floating-point number occupying three words to be stored with the exponent in the address supplied for it. The output of CNVT will be stored in the location supplied for its output and in the two words following that location. Operational characteristics of this program include the following steps:

```

*1500
RSFF=6712
DELAY=4160
GX4=6727
STFE=6743
CDS.      CLA          / INITIALIZE
          TAD ADDR
          DCA YLOC
          TAD NO
          DCA ENUF
          TAD STOR
          DCA DATA
          RSFF
          6702          / RE
          6714          / SET
          DELAY
          GX4
          DELAY
          TAD Z 114      / FREQ CODE
          TAD Z 113      / VOLT CODE
          STFE
          DELAY
AGN.      TAD I DATA    / LOAD
          DCA I YLOC     / DATA WORD
          ISZ DATA      / SET DATA FOR NEXT WORD
          ISZ YLOC       / SET YLOC
          ISZ YLOC       / FOR NEXT
          ISZ YLOC       / LOCATION
          ISZ ENUF       / THRU?
          JMP AGN        / NO, GET NEXT WORD
          JMP I RT       / YES, GO TO RATIO TRAN ROUTINE

ADDR.     2600          / FIRST DATA STOR
YLOC.     0000
NO.        7746          / 0-26
ENUF.     0000
STOR.     1542          / LOC OF FIRST DATA WORD
DATA.     0000
RT.        1200          / START ADD FOR RATIO TRAN ROUTINE

*1542
          6620          / ERROR
          6400
          6200
          6000
          5600
          5400
          5200
          5000
          4600
          4400
          4200
          4100
          4040
          3740
          3700
          3600
          3400
          3200
          3000
          2600
          2400
          2200
          2040
          1600
          1400
          1220          / ERROR
          $

```

Figure C-4. CDS PROGRAM LISTING.

Figure C-5. CNVT PROGRAM DIAGRAM.


```

/CONVERT A FLOATING POINT NUMBER TO AN INTEGER
/CALLING SEQUENCE: TAD (ADDRESS OF FP NUMBER)
/ ADDRESS OF OUTPUT STORAGE LOCATION.
/ RETURN
*400

CNVT, 0000
DCA ADF
TAD I CNVT
ISZ CNVT
DCA APUT /STORE OUTPUT STORAGE LOCATION
TAD I ADF /DETERMINE ROTATION DIRECTION
SNA
JMP SBNC /NO ROTATION
SMA
JMP ERR / GREATER THAN 20.47 PERCENT ERROR
LUP, DCA ROT /LOAD ROTATION COUNTER
ISZ ADF
TAD I ADF
CLL RAR
ISZ ROT
JMP --2

/ CONVERSION TO DECIMAL
/ CALLING SEQUENCE: TAD INTEGER
/ RETURN (XX XX)
SBNC, CLL
DCA VAL / INTEGRAL NUMBER OF TEN-THOUSANTS
DCA BOX
DCA DIGT
TAD Z 40-4
DCA ROT
TAD ADDR
DCA XYZ+2
TAD VAL
SPA
JMS I Z 71 / LINEARITY NOT POSITIVE
XYZ, DCA VAL
TAD VAL
TAD CON.
SMA
ISZ BOX /INCREMENT TO DEVELOP DECIMAL DIGIT
SMA
JMP XYZ /LOOP RETURN
ISZ DIGT / SWITCH PARITY
CLA
TAD BOX
JMS PRNT /STORE DECIMAL DIGIT
NEXT, DCA BOX /CLEAR BOX FOR NEXT DIGIT
ISZ XYZ+2
ISZ ROT
JMP XYZ+1 /RETURN FOR NEXT DIGIT
JMP I CNVT

ADF, 0000
APUT, 0000
ROT, 0000
0000
BR, 0000
DIGT, 0000

ADDR, TAD CON
BOX, 0000
VAL, 0000
CON, 6030
7634
7766
7777
/ TRANSFER DECIMAL DIGITS TO OUTPUT ARRAY
/ CALLING SEQUENCE: TAD (DECIMAL DIGIT)
/ RETURN
PRNT, 0000
TAD PNT+1
DCA SI
TAD DIGT
RAR
SNL /DETERMINE DIGIT PARITY
JMP EVEN
CLA CLL
TAD Z 40-6 /SET LOOP COUNTER
DCA ROT+1
TAD SI /ROTATE ODD DIGITS TO THE LEFT
RAL CLL
ISZ ROT+1
JMP --2
DCA SI+1
CLA CLL
JMP I PRNT
EVEN, DCA BR /TRACK DIGIT FOR FINISH
TAD SI
TAD SI+1
DCA I APUT / STORE PACKED PAIR OF DIGITS
ISZ APUT
CLL
TAD BR
RAR
SNL
JMP EVEN-2 / READY FOR NEXT DIGIT
DCA BR
TAD PNT / PACK DECIMAL POINT
JMP EVEN+3
SI, 0000
0000
PNT, 4056
0060
/ERROR TOO LARGE
ERR, CLA
TAD GTR
DCA I APUT
ISZ APUT
TAD GTR+1
DCA I APUT
ISZ APUT
TAD GTR+2
DCA I APUT
JMP I CNVT
GTR, 4040
4076
6260

```

Figure C-6. CNVT PROGRAM LISTING.

1. The program first stores the input number (FP) address in the accumulator, acquires the output address APUT, and increments the contents of the CNVT register to prepare it for the return. The exponent of FP is tested for sign and, if it is positive, the internal subroutine ERR loads > 20 in output storage and returns to the calling program. If the exponent is zero, the control skips to Step 3.
2. If the exponent is negative, the high-order mantissa is rotated to a position equivalent to an unnormalized floating-point number with a zero exponent. The resulting number (VAL) is assumed to be an octal number representing a decimal integer.
3. The routine beginning at SBNC determines the number of thousands contained in VAL by counting the number of times the octal equivalent of the decimal number -1000 may be added to VAL before the result becomes negative. The count is stored in BOX, which becomes the split-off decimal digit. After the count is stored by the internal subroutine PRNT, SBNC then splits off the hundreds, tens, and ones by subtracting 100, 10, and 1, respectively.

SBNC clears BOX and DIGT, a location which contains the number of the digit (1st, 2nd, etc) with which PRNT is entered. It loads a counter and initializes an instruction altered during execution. VAL is checked to see if it is positive, since a negative value indicates a malfunction in the least-squares routine. A negative value will cause entry into ERST from Location 442.

4. The appropriate constant is added to VAL, BOX is incremented, and when the digit is split off, DIGT is incremented and control transfers to internal subroutine PRNT, Step 6, with BOX in the accumulator.
5. After returning from PRNT, an instruction is incremented to begin subtracting the next constant. If all four digits have been determined, exit is made from subroutine CNVT; otherwise, control returns to Step 4.
6. PRNT adds 60 to BOX, rotates it five bits to the left if the parity is odd, and stores it. Odd parity returns control to Step 5.
7. An even-parity digit is packed with the previous odd digit and put in the permanent storage supplied to CNVT. The storage location is incremented, and if this is the first even digit, the decimal point code is put into storage, and the storage location incremented again. Control returns to Step 5.

Common, Page Zero (COMM)

Introduction - This program consists of the delay subroutine, negative number array, and subroutine starting addresses used by the other programs. Usefulness of this pro-

gram is that Page zero can be referenced from any page in the computer memory. A block diagram and a computer listing of the program are presented in Figures C-7 and C-8, respectively.

Figure C-7. COMM PROGRAM DIAGRAM.

Requirements - The COMM program utilizes computer memory locations on Page zero, as shown in the listing.

Description - The negative-number array consists of a series of negative constants (decimal) from -1 to -10 and -25. Similarly, the addresses are constants which specify the starting address of other programs as shown in the listing.

The Delay subroutine is used to allow time for relays and valves to actuate. The contents of the accumulator is maintained during the delay interval since this determines which devices are actuated in some operations. At the end of the delay, interface flip-flops are cleared, and program control is automatically returned to the subroutine calling instruction +1.

Executive Program (EXEC)

Introduction - This program controls the actual LVDT data acquisition process and coordinates the other programs in checking LVDT linearity. A block diagram of this program is shown in Figure C-9; a computer listing is presented in Figure C-10.

Requirements - The EXEC program occupies Locations 4000 through 4141, 0001 through 0007, and 0140 through 0154 in the computer and uses the excitation voltage and frequency code, negative number array, and delay subroutine stored in Page zero. It also uses the following separate programs: TYP0UT, XINC, and RATR.

Description - The program is entered manually from the computer console at Location 4000. The output format is typed using the separate type-out program (TYP0UT). All flags and relays in the system are cleared, and the excitation supply is set ac-

```

/COMM
/COMMON PAGE ZERO
/CONSTANTS, ADDRESSES, DELAY SUBROUTINE
/
/NEGATIVE NUMBER ARRAY
*0026
      7766          / -10 DECIMAL
      7767
      7770
      7771
      7772
      7773
      7774
      7775
      7776
      7777          / -1
      7747          / -25
*0115
      7746          / -26
/
/ADDRESSES
*0066
      3060          /TSC - PART OF TTY PACKAGE
      0200          /LS
*0073
      4174          /STP - PART OF EXEC
*0100
      2400          /LINEAR NUMBER ARRAY
*0101
      2600          /DATA ARRAY (STORAGE)
*0111
      0400          /CNVT
/
/DELAY SUBROUTINE
*0160
DLY,      0          /ENTRY
          DCA TEMP    /STORE AC
          TAD Z CSK
          DCA CNT      /SET BIAS
          TAD TEMP     /RESTORE AC
          ISZ CNT       /FINISHED DELAY?
          JMP .-1       / NO, DO ANOTHER
          6712         /RSFF
          JMP I DLY     /RETURN TO CALLING PGM
CSK,      5000        /BIAS CONSTANT
CNT,      0          /COUNT REGISTER
TEMP,     0          /TEMPORARY STORE
          $

```

Figure C-8. COMM PROGRAM LISTING.

ording to the voltage and frequency code. Next, the displacement increments separating LVDT data points are generated and stored using the displacement increment subroutine (XINC). The output voltage is checked for negative polarity and reversed if necessary. This step completes the static hardware initialization.

The fixture is driven forward, displacing the LVDT armature toward the null position. As the armature moves, the program finds the null by monitoring the signal amplifier output and detecting the negative-to-positive transition. After the null is located, the program finds the positive gaging range limit by counting eleven 5 percent increments using the one-increment (ONEINC) subroutine. At this point, the amplifier output is read and compared with an appropriate constant to determine in which voltage range it lies. These voltage ranges are: < 1.25, 1.25 to 2.5, 2.5 to 5, 5 to 10, and greater than 10. If the voltage is below 1.25 or greater than 10.0, the appropriate gain status message is typed using the type-out program (TYP OUT).

If the voltage is in the range of five to ten volts, the amplifier gain is not changed. However, if the voltage lies in one of the other two ranges, the amplifier gain is multiplied by two or four to get the output voltage in the five to ten-volt range.

After two delay intervals for fixture overtravel, the fixture is driven back, and the program again finds the positive gaging range limit using the interrupt program (INTRPT).

Next, the negative gaging-range limit is found by counting the twenty-five displacement increments using the one-increment (ONEINC) program. When this point is reached, the fixture is driven forward again after two delay intervals for overtravel. The program again finds the negative gaging-range limit by using the interrupt program (INTRPT). The signal amplifier output is read and stored in the data array. The other twenty-five data words are taken at the prescribed points by using the displacement increment array and the one-increment program to locate the points. When all data have been taken, the fixture is driven back in preparation for the next LVDT; program control goes to the ratio-transformer routine (RATR).

The ONEINC subroutine is entered by a jump-to-subroutine (JMS) instruction with the increment length (in $1/4$ fringes) in the AC. The contents of the AC are stored in the interferometer count register (INFCNT) of the interrupt program (INTRPT). The program then uses INTRPT to determine when the required number of interrupts have occurred. This work is accomplished by a jump-to-self instruction (JMP). When the increment is complete, control is returned to the calling instruction +1.

The INTRPT subroutine is entered when an interrupt (representing $1/4$ -fringe displacement) occurs. The contents of the AC are stored in the temporary storage location (TEMP) and the interferometer direction flag is started to determine whether the displacement is positive or negative. The program then modifies the interferometer count register (INFCNT) by one count, restores the AC, and enables the interrupt. Exit is to the instruction being performed when the interrupt occurred if the interferometer count register is not zero. If this register is zero, exit is to the next instruction.

Least-Squares Routine (LS)

Introduction - This program determines the best-fit line (in the least-squares sense) for LVDT output versus distance and finds the maximum deviation of the data from this line. A block diagram and a computer listing of this program are presented in Figures C-11 and C-12, respectively.

Requirements - The LS program occupies Locations 200 through 367 and utilizes information stored in Page zero.

Figure C-9. EXEC PROGRAM DIAGRAM.

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Figure C-11. LS PROGRAM DIAGRAM.

Description - The program is entered from LST. It expects Location 0115 to contain $0 - N$, where N is the number of floating-point numbers to be fitted with a line. It acquires the addresses of the first ordinate and mantissa from 0100 and 0101, respectively. The slope of the line, S , is determined by the algorithm $S = (\sum X^2 - \sum X) / (\sum XY - \sum Y)$. The maximum deviation from the line with this slope, passing through the origin, is stored in MAXE, Location 0020. Control is returned to LST.

Least-Squares Control (LST)

Introduction - This program, diagrammed in Figure C-13 and computer listed in Figure C-14, initializes Page zero for LS, calls it, and normalizes the resulting maximum error to ten thousandths.

Requirements - This routine occupies Locations 3400 through 3476 and utilizes Page zero.

Description - LST loads zero in 0023, calls LS, normalizes MAXE to a percentage, multiplies it by 10,000 decimal, and calls CNVT. It then returns to EXEC.

Preliminary Check Out (PCHK)

Introduction - This program operates the equipment to facilitate check out and adjustment of the amplifier zero and balance, LVDT phase shift, and interferometer balance. The program is diagrammed in Figure C-15 and a computer listing is presented in Figure C-16.

Requirements - The PCHK program occupies Locations 1000 through 1123 in the computer. It also uses the negative number array, excitation voltage and frequency data, and delay subroutine stored in Page zero.

Description - The program is entered manually from the computer console. Entry for amplifier zero, amplifier balance, and LVDT phase shift is at Location 1000 with the switch register set to 1000, 5000, or 0000. The program resets all latching relays and transfers the amplifier input to the LVDT. Next, the amplifier gain is set to maximum and the excitation voltage and frequency are selected. The switch register is read to determine which check is to be performed. If it is phase shift, a jump to the display (DSPLY) subprogram is made. This subprogram periodically reads the ADC input voltage, disregards the insignificant bit, and displays the remainder in the AC as a negative number regardless of polarity. Three delay instructions are used between the ADC readings to eliminate AC light flicker.

If the amplifier zero or balance is to be checked, the amplifier input is transferred to the ratio transformer which is set for zero volt output. The switch register is again

```

/ FIND LEAST-SQUARES LINE /
*200
LS, 0000
CLA
TAD Z 115
DCA MCTR / STORE LOOP COUNTER /
TAD Z 100
DCA ADX
TAD Z 101
DCA ADY
JMS I Z 7 / INITIALIZE SUMS
FGET Z 23
FPUT SMX2
FPUT I SUMX
FPUT I SUMY
FPUT SMXY
FPUT I MAXE
FEXT
D1, JMS I Z 7 / CALCULATE SUMS /-
FGET I ADX
FADD I SUMX
FPUT I SUMX / SUM XI /
FGET I ADX
FMPY I ADX
FADD SMX2
FPUT SMX2 / SUM XI**2 /
FGET I ADY
FADD I SUMY
FPUT I SUMY / SUM YI /
FGET I ADY
FMPY I ADX
FADD SMXY
FPUT SMXY / SUM XI*YI /
FEXT
CLA / RESET ADDRESSES XI, YI /
TAD ADX
TAD THRE
DCA ADX
TAD ADY
TAD THRE
DCA ADY
ISZ MCTR / TEST FOR FINISH OF SUMS LOOP /
JMP D1
JMS I Z 7
FGET SMX2
FSUB I SUMX
FPUT I DELT
FGET SMXY
FSUB I SUMY
FDIV I DELT
FPUT SLPE / STORE LINE SLOPE /
FEXT
CLA
TAD Z 115 / RESET COUNTER AND ADDRESSES FOR ERROR LOOP /
DCA MCTR
TAD Z 100
DCA ADX
TAD Z 101
DCA ADY
D2, JMS I Z 7 / START OF ERROR LOOP /
FGET SLPE
FMPY I ADX
FSUB I ADY
FPUT TEM
FEXT
CLA / TEST LOW ORDER MANTISSA FOR CARRY
TAD TEM+2
CLL CMA IAC
DCA TEM+2
TAD TEM+1
SMA
JMP .+4 / POSITIVE ERROR
SZL
TAD Z 37 / CARRY FROM LOW ORDER MANTISSA
CMA / FORM ABSOLUTE VALUE OF ERROR
DCA TEM+1
JMS I Z 7 / TEST AMBIENT ERROR FOR MAXIMUM
FGET I MAXE
FSUB TEM
FPUT ETEM
FEXT
CLA
TAD ETEM+1
SMA
JMP .+5 / AMBIENT ERROR IS NOT MAXIMUM /
JMS I Z 7 / IF IT IS, IT BECOMES MAXE
FGET TEM
FPUT I MAXE
FEXT
CLA
TAD ADX / RESET COUNTERS FOR ERROR LOOP /
TAD THRE
DCA ADX
TAD ADY
TAD THRE
DCA ADY
ISZ MCTR / TEST FOR FINISH OF ERROR LOOP /
JMP D2
JMP I LS / READY FOR PRINT-OUT /

ADX, 0000
ADY, 0000
THRE, 0003
MCTR, 0-33
MAXE, 0020 / ADDRESS OF LINIARITY STORAGE LOCATION
SUMX, 2573
SUMY, 2773
SMXY, 0000
0000
0000
SMX2, 0000
0000
0000
TEM, 0000
0000
0000
SLPE, 0000
0000
0000
ETEM, 0000
0000
0000
DEI T, 2570

```

Figure C-12. LS PROGRAM LISTING.

Figure C-13. LST PROGRAM DIAGRAM.

read to determine which amplifier check is to be performed. If it is balance, the amplifier gain is set for minimum and the nine most significant bits of the ratio transformer are operated in a successive approximation manner to set the amplifier output near nine volts. When the proper combination of bits is determined, the ratio-transformer relays are latched in and the DSPLY subprogram entered again.

If the amplifier zero is to be checked, the ratio transformer is unlatched to give zero volt output and the READ subprogram is entered. This subprogram is similar to the DSPLY subprogram except the polarity as well as magnitude of the voltage is displayed.

The subprogram for interferometer balance (INF) is entered by starting in Location 1114. The command flip-flops are cleared, and the FXFD command is generated. After a delay to allow the relays to operate, the computer halts. The other half of the subprogram, which generates the FXBK command, is entered by operating the Continue switch. The program recycles with the next Continue operation.

Ratio-Transformer Routine (RATR)

Introduction - This program, diagrammed in Figure C-17 and listed in Figure C-18, converts each LVDT data word into a ratio-transformer word and stores the results as a normalized floating-point number.

```

*3400
LST,  CLA
      JMS  I Z 7
      FGET  LINZ
      FPUT  Z 23      / RELOAD FLOATING ZERO
      FEXT
      CLA
      TAD      SET
      NOP
      JMS  I Z 67      / DETERMINE LINEARITY
      CLA
      JMS  I Z 7      / NORMALIZE LINEARITY WITH FIRST
      FGET  Z 20      / MEMBER OF Y-ARRAY,
      FDIV I Z 101
      FMPY  TENT      / AND MULTIPLY BY TEN THOUSAND
      FPUT  Z 20
      FEXT
      CLA CLL      / ADJUST DECIMAL POINT WITH EXPONENT
      TAD  Z 20
      TAD  ELVN
      DCA  Z 20
      TAD  ALIN      / CONVERT FP NUMBER TO OUTPUT FORMAT
      JMS  I Z 111
OUT,  STOR
      CLA      / TYPE LINEARITY
      TAD  OUT
      JMS  I Z 66
      JMP  I Z 73      / RETURN FOR NEXT GAGE
STOR, 0000      / OUTPUT STORAGE
      0000
      0000
      0045
      0015
      0012
      0012
      0001
ALIN, 0020
      0015      / CR, LF, THE LINEARITY OF THIS GAGE IS
      0012
      2410
      0540
      1411
      1605
      0122
      1124
      3140
      1706
      4024
      1011
      2340
      0701
      0705
      4011
      2340
      4040
      0001
SET,  ALIN+1
ELVN, 7765
TENT, 0016      / 10,000 DECIMAL
      2342
      0000
LINZ, 0000
      0000
      0000

```

Figure C-14. LST PROGRAM LISTING.

Requirements - The RATR program occupies Locations 1200 through 1366 in the computer and uses the negative-number array and delay subroutine located in Page zero. It also uses the manufacturer-supplied floating-point package (DEC).

Description - The program is entered at Location 1200 from either the constant-data storage (CDS) or executive (EXEC) programs by a JMP instruction. The data-address register (Y) and data-points counter (MORE) are initialized.

RTA - To start conversion of each data word, the ratio-transformer relays are unlatched; the delay subroutine is entered to allow time for the relays to release. The data address register is indexed to contain the address of the current data word, and the half-word counter (THAF) is initialized.

RTH - To start conversion in each half of the ratio-transformer word, the binary word register (BINO) is cleared, the rotating bit register (RY) is set to 4000, and the number of bits counter (NOBT) is initialized.

RTB - To check each ratio-transformer bit, contents of the rotating-bit register is shifted right one bit, and the conversion subroutine (CONV) is entered to test the new bit. The binary word register is changed to include this bit if the conversion indicates it should be included.

CONV - The status of each successive bit in the ratio-transformer word is determined by assuming it should be a "1" and checking the result. Thus, a trial word is formed by adding the new bit from the rotating bit register (RY) to that part of the word already assembled in the binary word register (BINO). The result, set into the ratio transformer, is taken on ADC reading and stored in the temporary storage register (TEMP). This ratio-transformer reading and LVDT reading are added, and Bit 0 of the AC is tested to determine whether the readings have the same polarity. If not, the phase of the amplifier reference voltage is reversed to change polarity of the ratio-transformer reading, and the operations are repeated.

When both readings have the same polarity, their magnitudes are compared. First, the link is tested to determine which polarity. If negative, the ratio-transformer reading is complemented and added to the LVDT reading. If positive, the LVDT reading is complemented and added to the ratio-transformer reading. Finally, Bit 0 of the AC is tested to determine which reading has the greatest magnitude. If the ratio-transformer reading is greatest, control is returned to the subroutine calling instruction +2; the bit tested is stored as a "0". Otherwise, control is returned to the subroutine calling instruction +1, and the bit is stored as a "1".

TEST - After each bit conversion, the number of bits counter (NOBT) is tested to determine whether one-half the ratio-transformer word has been formed. If not, RTB is reentered to form the next bit. If so, the half-word counter is tested to determine whether the first half or the entire word has been formed. If only the first half is complete, it is stored in the high-order word register (HOW) and latched into the most significant half of the ratio transformer. The RTH program is then reentered to form the last half.

ADJ - When the last half word is formed, it is stored in the low-order word register (LOW). Thus, the complete word is contained in Bits 0 through 8 of


```

*1000
DELAY=4160
FXFD=6701
STFE=6703
FXBK=6704
STRT=6705
SLRT=6706
RFRV=6707
RSFF=6712
GX1=6721
GX4=6727

CLA / ENTRY FOR ZERO, BAL, & PHASE.
6702 / RE
6714 / SET
DELAY
GX4
DELAY
TAD Z 110
TAD Z 113
STFE
DELAY
DELAY
LAS
SNA CLA / PHASE?
JMP DSPLY / YES, DISPLAY FOR PHASE ADJ.
STRT
DELAY
LAS
SPA CLA / ZERO OR BAL?
JMP BAL / BALANCE
ZERO, 6703 / UL
6714 / RT
DELAY
READ, ADC
AND C7776 / DROP BIT 11
DELAY
DELAY
JMP READ / RECYCLE.
BAL, CLA
GX1
DELAY
DCA BINO
TAD Z 27
DCA ENUF
TAD C4K
DCA RY
AGN, CLA
TAD BINO
TAD RY
STRT
DELAY
ADC
DELAY
SMA / POSITIVE VOLTAGE?
JMP .+4 / YES, CARRY ON.
RFRV / NO, MAKE IT POSITIVE.
DELAY
JMP AGN / RECHECK POLARITY.
TAD REF / 9.37V
SMA CLA / V>REF?
TAD RY / NO, KEEP THIS BIT.
TAD BINO / YES, DROP IT.
DCA BINO
TAD RY
CLL RAR / SET RY FOR NEXT BIT.
DCA RY
ISZ ENUF / FINISHED?
JMP AGN / NO, TRY ANOTHER.
TAD BINO
SLRT
DELAY
DSPLY, DELAY
ADC
AND C7776 / DROP BIT 11
SMA / IF POSITIVE VOLTAGE,
CIA / DISPLAY AS NEGATIVE.
DELAY
DELAY
JMP DSPLY / RECYCLE.
C7776, 7776
RY, 0000
BINO, 0000
ENUF, 0000
C4K, 4000
REF, 7600
INF, RSFF / ENTRY FOR INTERFEROMETER, BAL.
FXFD
DELAY
HLT
FXBK
DELAY
HLT
JMP INF+1 / RECYCLE.
$

```

Figure C-16. PCHK PROGRAM LISTING.

Figure C-17. RATR PROGRAM DIAGRAM.

<pre> *1200 STRT=6705 SLRT=6706 RFRV=6707 DELAY=4160 RATR, CLA / ENTRY TAD YLOC / INITIALIZE DCA Y TAD NPTS DCA MORE </pre>		<pre> / ORDER WORD-LOW ORDER WORD / COMPLETE-PUT IN LO ORDER FA. </pre>
RTA,	<pre> 6703 / START EACH READING. UL 6714 / DELAY CLA ISZ Y / INDEX ISZ Y / DATA ISZ Y / ADDRESS TAD Z 36 / 0-2 DCA THAF </pre>	<pre> / LOAD HI ORDER FA TAD C27 DCA Z 44 / LOAD FP EXPONENT JMS I Z 7 / ENTER FP PGM FNOR FPUT I Y FEXT ISZ MORE / FINISHED ALL POINTS? JMP RTA / NO, TAKE NEXT POINT JMP I CALC / YES, GO TO LS FIT ROUTINE </pre>
RTH,	<pre> CLA / START EACH HALF READING DCA BINO DCA RY TAD Z 27 / 0-9 DCA NOBT </pre>	<pre> / HIGH ORDER WORD STORE / LOW ORDER WORD STORE / NUMBER OF POINTS COUNTER / HALF WORD COUNTER / BINARY WORD STORE / BIT COUNTER / ROTATING BIT STORE </pre>
RTB,	<pre> CLA CLL CML /ENTRY FOR SUCCESSIVE BITS TAD RY RAR DCA RY JMS CONV JMP TEST </pre>	<pre> / ADDR OF LEAST SQUARES RTN / ADDR OF DATA ARRAY -3 / ENTRY FOR VOLTAGE COMPARISON / FORM NEW / TRIAL WORD </pre>
TEST,	<pre> CLA TAD BINO TAD RY DCA BINO CLA CLL ISZ NOBT / FINISHED THIS HALF? JMP RTB / NO, DO NEXT BIT ISZ THAF / YES, WHICH HALF WAS IT? JMP .+2 / FIRST, GET LAST HALF JMP ADJ / LAST, ADJUST TO FP FORMAT TAD BINO SLRT DELAY DELAY DCA HOW JMP RTH </pre>	<pre> / ADDR OF LEAST SQUARES RTN / ADDR OF DATA ARRAY -3 / ENTRY FOR VOLTAGE COMPARISON / FORM NEW / TRIAL WORD </pre>
ADJ,	<pre> TAD BINO DCA LOW TAD HOW CLL RAR CLL RAR CLL RAR DCA HOW TAD LOW CLL RAR CLL RAR CLL RAR DCA LOW TAD HOW AND MSK9 CLL RTR </pre>	<pre> / SHIFT HIGH ORDER WORD / 3 BITS RIGHT / SHIFT LOW ORDER WORD / 3 BITS RIGHT / MASK OUT 9 MOST SIGNIFICANT / BITS IN HIGH ORDER WORD- / ROTATE REMAINING BITS TO HIGH / ORDER POSITION-ADD TO LOW </pre>
<pre> </pre>		<pre> / ORDER WORD-LOW ORDER WORD / COMPLETE-PUT IN LO ORDER FA. / SHIFT HIGH ORDER WORD / 3 BITS RIGHT / LOAD HI ORDER FA TAD C27 DCA Z 44 / LOAD FP EXPONENT JMS I Z 7 / ENTER FP PGM FNOR FPUT I Y FEXT ISZ MORE / FINISHED ALL POINTS? JMP RTA / NO, TAKE NEXT POINT JMP I CALC / YES, GO TO LS FIT ROUTINE / HIGH ORDER WORD STORE / LOW ORDER WORD STORE / NUMBER OF POINTS COUNTER / HALF WORD COUNTER / BINARY WORD STORE / BIT COUNTER / ROTATING BIT STORE / ADDR OF LEAST SQUARES RTN / ADDR OF DATA ARRAY -3 / ENTRY FOR VOLTAGE COMPARISON / FORM NEW / TRIAL WORD </pre>
<pre> </pre>		<pre> / POLARITY CORRECT? / YES / NO, REVERSE IT / RECHECK POLARITY / WHICH POLARITY? / NEGATIVE NUMBERS </pre>
<pre> </pre>		<pre> / RATIO-TRAN VOLT HI? / NO / YES / POSITIVE NUMBERS </pre>
<pre> </pre>		<pre> / TEMPORARY STORAGE REG / DATA ADDRESS REGISTER / 0-26 </pre>

Figure C-18. RATR PROGRAM LISTING.

HOW and LOW. Contents of these registers are modified such that the complete word is contained in Bits 6 through 11 of HOW and Bits 0 through 11 of LOW. These items are stored in the high-order floating accumulator (0045) and low-order floating accumulator (0046) of the floating-point program (digital 8-5-S). Finally, the constant exponent is stored in the floating-point program exponent register (0044) to complete the floating-point representation of the ratio-transformer word. The floating-point program is then entered to normalize this number and store the results. Next, the number-of-points counter (NOBT) is tested to determine whether all data points have been processed. If not, the RTA program is reentered to process the next reading. If so, control goes to the least-squares fit routine (LS).

Type Out (TYP OUT)

Introduction - This program, diagrammed in Figure C-19 and listed in Figure C-20, is used to type the output format and gain-status messages.

Requirements - The TYP OUT program occupies Locations 4200 through 4377 in the computer and uses the delay subroutine stored in Page zero.

Description - The program is entered automatically at Location 4200 from the executive program (EXEC) by a jump-to-subroutine (JMS) instruction. The command to drive the fixture back is given to insure that the fixture is in the proper starting position, and the delay subroutine is entered to allow relays to actuate. Next, the address of the calling instruction is tested to determine whether the type out is format, gain low, or gain high. This operation is accomplished by checking Bits 5 and 6 of the address. If both bits are "0", the EXEC calling instruction address is below 4240 and the format is to be typed. Similarly, if Bit 5 or 6 is a "1", the gain-low or gain-high message, respectively, is to be typed. This information is used to set the starting address of the appropriate character string into the current character address register (CUCH). The teletype print command is given to set the teleprinter flag in preparation for typing the character string.

TYP - This subprogram performs the actual type out. The character to be typed is loaded into the accumulator and tested for end-of-string coding (7777). When this code is detected, control is returned to the calling instruction +1.

Otherwise, the program waits for the teleprinter flag to be set indicating the teletype is ready to print the character. The print command is then given and the current character address register incremented in preparation for the next character. Finally, control is returned to TYP for printing the next character.

Figure C-19. TYP OUT PROGRAM DIAGRAM.

*4200		TYP,	CLA	/ ENTER CHAR TYPE LOOP	Q		L
A=301			TAD I CUCH	/ GET CHARACTER	CLN		RET
C=303			SPA	/ END OF CHAR STRING?	RET		LNF
D=304			JMP I TYP0UT	/ YES, RETURN TO CALLING PGM	LNF		LNF
E=305			TSF	/ NO, WAIT FOR TP FLAG	LNF		L
F=306			JMP --1		M		EYE
G=307			TLS	/ TYPE CHARACTER	F		N
H=310			ISZ CUCH		R		E
K=313			JMP TYP	/ DO IT AGAIN	CLN		A
L=314		C10,	0010		RET		R
M=315		C140,	0140		LNF		EYE
N=316		CUCH,	0	/ CURRENT CHAR ADDR REGISTER	LNF		T
O=317		CHAD,	4240	/ CHAR STRING START ADDR	F		Y
Q=321		*4240			R		CLN
R=322			G	/ GAIN HI	E		SPAC
T=324			A		Q		END
V=326			EYE		CLN		\$
X=330			N		SPAC		
Y=331			SPAC		X		
DSH=255			H		X		
CLN=272			EYE		K		
EYE=311			END		C		
RET=215			G	/ GAIN LO	RET		
LNF=212			A		LNF		
END=7777			EYE		LNF		
SPAC=240			N		V		
FXBK=6704			SPAC		O		
DELAY=4 60			L		L		
TYP0UT, 0	/ ENTRY		O		T		
FXBK			END		CLN		
DELAY			RET	/ FORMAT	SPAC		
CLA			LNF		X		
TAD TYP0UT	/ GET CALLING INST ADDR		M		V		
AND C140			DSH		RET		
CLL RTL			RET		LNF		
RTL			LNF		LNF		
RAL			LNF		R		
SNA	/ FORMAT?		D		A		
JMP ++4	/ YES		A		N		
SPA CLA	/ NO, GAIN LO OR HI?		T		G		
JMP ++3	/ LO		E		E		
JMP ++3	/ HI		CLN		CLN		
TAD C10	/ GET FORMAT ADDR		RET		SPAC		
TAD C10	/ GET GAIN LO ADDR		LNF		X		
TAD CHAD	/ GET GAIN HI ADDR		LNF		X		
DCA CUCH			R		M		
TLS	/ TYPE TO SET FLAG		E		EYE		

Figure C-20. TYP0UT PROGRAM LISTING.

Displacement Increments Subroutine (XINC)

Introduction - This subroutine uses the gaging-range code to generate and store an array of twenty-five octal numbers that represent displacement increments between LVDT datum points. The program is diagrammed in Figure C-21 and listed in Figure C-22.

Figure C-21. XINC PROGRAM DIAGRAM.

Requirements - The XINC subroutine occupies Locations 1400 through 1476 in the computer. It also uses the gaging range data (0112) and one auto-indexing register (0010) in Page zero.

Description - The program is entered at Location 1400 by a jump-to-subroutine (JMS) instruction in the executive (EXEC) program. Control is returned to the calling instruction +1 when all increments have been stored.

The increments are stored consecutively from 1445 through 1476 in three operations. First, the ten 5-percent increments starting from one extreme of the gaging range are stored. Next, the five mixed increments (2.5, 1.25, 2.5, 1.25, and 2.5 per-

```

*1400
XINC,      0          / ENTRY
           CLA         / INITIALIZE
           TAD XLOC
           DCA Z 10
           TAD Z 40-2
           DCA TWO
THAF,      TAD C10     / SET INCREMENT COUNTER
           DCA ENUF    / FOR HALF 5% INCREMENTS
           TAD Z 112   / GET GAGING RANGE INC- 5%
           DCA I Z 10  / STORE IN X-ARRAY
           ISZ ENUF    / FINISHED HALF 5% INC?
           JMP -3      / NO, DO ANOTHER
           ISZ TWO     / YES, WHICH HALF?
           JMP CNTL    / FIRST, GET CENTRAL INCS
           TAD XLOC    / LAST, RESET STORAGE
           DCA Z 10    / ADDRESS REGISTER
           JMP I XINC  / RETURN TO CALLING PGM
CNTL,      CLA         / SET INCREMENT
           TAD Z 40-5  / COUNTER FOR
           DCA ENUF    / CENTRAL INCREMENTS
MORE,      TAD Z 112   / GET GAGING RANGE INC- 5%
SHFT,      RAR         / CHANGE TO 2.5% OR 1.25%
           DCA I Z 10  / STORE IN X-ARRAY
           ISZ ENUF    / FINISHED CENTRAL INCS?
           JMP MOD     / NO, MODIFY SHFT & DO ANOTHER
           JMP THAF    / YES, GET 2ND HALF 5% INCS
MOD,       TAD SHFT    / CHANGE SHFT
           CLL RTR     / FROM
           CML         / RAR TO RTR
           RTL         / OR FROM
           DCA SHFT    / RTR TO RAR
           JMP MORE
XLOC,      1444        / FIRST ADDR OF X-ARRAY
C10,       0-12
ENUF,      0          / INCREMENT COUNTER
TWO,       0          / HALF ARRAY COUNTER
           S

```

Figure C-22. XINC PROGRAM LISTING.

cent) near the null point are generated and stored. And finally, the last ten 5-percent increments are stored to complete the array.

Maintenance Program (LVDT-MTN)

Introduction - This program, diagrammed in Figure C-23, enables the computer to be used in maintaining and troubleshooting the other equipment.

Requirements - The LVDT-MTN program utilizes computer memory locations, as shown in Figure C-24. It does not require any other programs or routines to operate.

Description - The program consists of individual subprograms to check a specific part of the system, subroutines, and constants used by more than one of these subprograms. Each subprogram is entered manually from the console, and the subroutines are entered automatically from subprograms as required.

The Type End routine is used to signal the operator that a test is finished. It will type END on the teletype and the computer will halt. If the Continue switch is actuated, the program recycles, preventing the operation from accidentally destroying part of the program.

The TYP OUT subroutine types a string of characters. It is entered by a JMS instruction with the starting address of the character string in the accumulator. Characters are then typed until the stop code (777) is encountered. Program control is automatically returned to the subroutine calling instruction +1.

The Delay subroutine is used to allow time for relays and valves to actuate. The contents of the accumulator is maintained during the delay since this determines which devices are actuated in some cases. At the end of the delay, interface flip-flops are cleared, and program control is automatically returned to the subroutine calling instruction +1.

Refer to the section on Maintenance for a description of operations performed by each subprogram.

LVDT-D-XXX: LVDT Data Codes

The data code tapes simply store the appropriate codes for excitation voltage, excitation frequency, and gaging range. The codes are stored in their respective registers in Page zero, and the appropriate teletype character codes are stored in the format-type out subroutine (WRT). Voltage codes are 0 through 7 for 0 through 7 volts. Frequency codes are 2400 and 4000 for 5 and 10 kc, respectively. The gaging-range code is 0120 (octal) for each 0.005 inch. The four tapes listed in Figure C-25 are for the most commonly used combinations of voltage, frequency, and gaging range. Tapes for other combinations can be made easily.

Figure C-23. MAINTENANCE (LVDT-MTN) PROGRAM DIAGRAM.

```

/ LVDT-MTN
/ MAINTENANCE PROGRAM
DELAY=4160
FXFD=6701
FXSP=6702
STFE=6703
FXEK=6704
SLRT=6705
DCA DSC2
RFRV=6707
RSFF=6712
GX1=6721
GX2=6723
GX4=6727
/
/ CONSTANTS
*0060
C10, 0010
C4K, 4000
C5K, 5000
CM2, 7776
CM3, 7775
CM4, 7774
CM7, 7771
CM9, 7767
/
/ TYPE "END" ROUTINE
*0100
TYPEND, CLA
TAD END
JMS TYP / TYPE
HLT
JMP TYPEND / TYPE IT AGAIN
END, 4000 / END" CHAR STRING
/ VOLT & FREQ DATA
*0113
0002 / 2 VOLTS
*0110
4000 / 10 KC
/ TYPEOUT SUBROUTINE
*0140
TYP, 0 / ENTRY
DCA NXCH / STORE CHAR STRING ADDR
TIS
CLA
TAD I NXCH / GET NEXT CHAR
ISZ NXCH
SMA / FINISHED?
JMP +3 / NO
CLA
JMP I TYP / YES, RETURN TO CALLING PGM
TSF
JMP +1
TIS
JMP AGN0 / DO ANOTHER
/ ADDR OF NEXT CHAR
NXCH, 0
/ DELAY SUBROUTINE
*0160
DLY, 0 / ENTRY
DCA TEMP / STORE AC
TAD Z CSK / TIME BIAS
DCA CNT / INITIALIZE COUNT REGISTER
TAD TEMP / RESTORE AC
ISZ CNT / DELAY FINISHED?
JMP +1 / NO
RSFF / YES
JMP I DLY / RETURN TO CALLING PGM
CNT, 0 / DELAY COUNT REGISTER
TEMP, 0 / TEMPORARY STORE
/
/ DEVICE SELECTOR, PART 1
*0200
CLA
TAD Z CM2
DCA SETCNT / INITIALIZE
TAD INTCH
DCA CHAR
TAD INST1
DCA DSC2
TAD INTC
DCA DSC1
TAD Z CM7
SKP
ANTS, TAD Z CM4 / START EACH SET
DCA CMDCNT
ANTC, RSFF / START EACH COMMAND
DSC1, 0 / 1ST HALF COMMAND
DSC2, 0 / 2ND
TAD CHAR
JMS TYP / TYPE COMMAND
HLT
TAD CHAR
TAD Z C10
DCA CHAR / INCREMENT CHAR ARRAY REG
ISZ DSC1
ISZ CMDCNT / FINISHED THIS SET?
JMP ANTC / NO, DO ANOTHER
ISZ SETCNT / YES, WHICH SET?
SKP / 1ST
JMP +4
TAD INST2
DCA DSC2 / CHANGE 2ND HALF COMMAND
JMP ANTS / DO 2ND SET
RSFF
JMP TYPEND / TYPE "END"
CHAR, 0 / CHARACTER ARRAY REG
INTCH, 4010 / INITIAL CHAR ARRAY ADDR
INST1, 7000 / NOP INSTRUCTION
INTC, 6701 / INITIAL COMMAND
CMDCNT, 0 / COMMAND COUNTER
INST2, 6714 / 2ND HALF CMD OF 2ND SET
SETCNT, 0 / SET COUNTER
/ DEVICE SELECTOR, PART 2
*0260
RSFF
GX1
HLT
GX2
HLT
GX4
HLT
JMP TYPEND / TYPE "END"
/ DEVICE SELECTOR, PART 3
*0270
LAS
DCA CMD
CMD, 0 / CHANGEABLE COMMAND
JMP CMD / REGENERATE COMMAND
/
/ AC DECODER & BUFFER, PART 1A
*0300
RSFF
6703 / UL
6714 / RT
DELAY
DELAY
AGN1, CMA / START
HLT
RSFF / RECYCLE
JMP AGN1
/ AC DECODER & BUFFER, PART 1B
*0320
RSFF
6702 / RE
6714 / SET
DELAY
DELAY
SLRT
DELAY
DELAY
CMA
AGN2, STRT
HLT
RSFF
DELAY
JMP AGN2 / RECYCLE
/ AC DECODER & BUFFER, PART 2
*0340
RSFF
CMA
STFE
HLT
RSFF
JMP AGN3 / RECYCLE
/ FIXTURE & CONTROL
*0400
PGN1, RSFF
FXFD
HLT
RSFF
FXSP
HLT
RSFF
FXEK
HLT
JMP BGN1 / RECYCLE
/ INTERFEROMETER
*0500
PGN2, RSFF
FXFD
HLT
RSFF
FXEK
HLT
JMP BGN2 / RECYCLE
/ V & F SELECT, VOLT
*0600
CMA
AGN4, RSFF
6702 / RE
6714 / SET
DELAY
IAC
STFE
HLT
RSFF
DELAY
JMP AGN4 / RECYCLE
/ V & F SELECT, FREQ
*0640
RSFF
CLA
AGN5, 6702 / RE
6714 / SET
DELAY
TAD F5
STFE
DELAY
HLT
CLA
6702 / RE
6714 / SET
DELAY
TAD F10
STFE
DELAY
HLT
JMP AGN5 / RECYCLE
F5, 2400 / SKC CODE
F10, 4000 / 10KC CODE
/
/ RATIO TRAN & CONTROL
*0700
RSFF
6702 / RE
6714 / SET
DELAY
CLA
TAD Z 0113 / EXCIT VOLT CODE
TAD Z 0110 / EXCIT FREQ CODE
STFE
DELAY
CLA / INITIALIZE REGISTERS
TAD Z CM2
DCA HFCNT
TAD Z CM9
DCA BTCNT
STL
RAR / SET BIT 0
STRT
HLT / DIVIDED OUTPUT
RSFF
DELAY
ISZ BTCNT / FINISHED THIS HALF?
JMP AGN6 / NO, DO NEXT BIT
ISZ HFCNT / YES, WHICH HALF?
SKP / FIRST, DO LAST
JMP +6 / LAST
CLA
SLRT
DELAY
DELAY
JMP HLF / UL
6703 / RT
6714
DELAY
DELAY
JMP TYPEND / TYPE "END"
0 / BIT COUNTER
0 / HALF COUNTER
/ SIGNAL AMPLIFIER
*1000
CLA / ENTRY FOR ZERO, BAL, & PHASE
6702 / RE
6714 / SET
DELAY
GX4
DELAY
TAD Z 110
TAD Z 113
STFE
DELAY
DELAY
LAS
SNA CLA / PHASE?

```

Figure C-24. MAINTENANCE (LVDT-MTN) PROGRAM LISTING.

	JMP DSPLY	/ YES, DISPLAY FOR PHASE ADJ.	B=302		L
	STRT		D=304		R
	DELAY		E=305		T
	LAS		F=306		STOP
	SPA CLA	/ ZERO OR BAL?	K=313	*4070	
ZERO,	JMP BAL	/ BALANCE	L=314		RTN
	6703	/ UL	M=316		LNF
	6714	/ RT	P=320		R
	DELAY		Q=322		F
READ,	ADC		R=323		R
	AND Z CM2	/ DROP BIT 11	T=324		V
	DELAY		U=325		STOP
	DELAY		V=326	*4100	
	DELAY		X=330		RTN
BAL,	JMP READ	/ RECYCLE.	DSH=255		LNF
	CLA		ONE=261		S
	GX1		TWO=262		P
	DELAY		RTN=215		R
	DCA BINO		LNF=212		DSH
	TAD Z CM9		STOP=7777		ONE
	DCA ENUF		*4000		STOP
	TAD Z C4K			RTN	*4110
	DCA RY			LNF	
AGN,	CLA			E	RTN
	TAD BINO			N	LNF
	TAD RY			D	R
	STRT			STOP	E
	DELAY		*4010		S
	ADC			RTN	E
	DELAY			LNF	T
	SMA	/ POSITIVE VOLTAGE?		F	STOP
	JMP .+4	/ YES, CARRY ON.		X	
	RFRV	/ NO, MAKE IT POSITIVE.		F	RTN
	DELAY			D	LNF
	JMP AGN	/ RECHECK POLARITY		STOP	U
	TAD REF	/ 9.37V	*4020		L
	SMA CLA	/ V>REF?		RTN	R
	TAD RY	/ NO, KEEP THIS BIT.		LNF	T
	TAD BINO	/ YES, DROP 11.		F	STOP
	DCA BINO			X	
	TAD RY			S	RTN
	CLL RAR	/ SET RY FOR NEXT BIT.		P	LNF
	DCA RY		*4030	STOP	S
	ISZ ENUF	/ FINISHED?		RTN	P
	JMP AGN	/ NO, TRY ANOTHER.		LNF	R
	TAD BINO			S	DSH
	SLRT			T	TWO
	DELAY			F	STOP
	DELAY			E	
DSPLY,	ADC			STOP	
	AND Z CM2	/ DROP BIT 11	*4040		RTN
	SMA	/ IF POSITIVE VOLTAGE,		LNF	
	CIA	/ DISPLAY AS NEGATIVE.		F	
	DELAY			X	
	DELAY			P	
	DELAY			K	
	JMP DSPLY	/ RECYCLE.		STOP	
REF,	7600			RTN	
RY,	0	/ ROTATING BIT REGISTER	*4050	LNF	
PINO,	0	/ BINARY NUMBER STORE		S	
ENUF,	0000			T	
INF,	RSFF	/ ENTRY FOR INTERFEROMETER BAL		R	
	FXFD			T	
	DELAY			STOP	
	HLT		*4060		RTN
	FXRK			LNF	
	DELAY			S	
	HLT				
	JMP INF+1	/ RECYCLE.			
/ CHARACTER STRINGS					

Figure C-24. (Continued).

```

/ LVDT-D-2-10-10
/ DATA TAPE
*0113      0002      / V = 2 VOLTS
*0110      4000      / F = 10 KC
*0112      0240      / R = 10 MIL
*2340      0262      / 2
*2323      0261      / 1
              0260      / 0
*2354      0261      / 1
              0260      / 0
              $

```

```

/ LVDT-D-2-10-20
/ DATA TAPE
*0113      0002      / V = 2 VOLTS
*0110      4000      / F = 10 KC
*0112      0500      / R = 20 MIL
*2340      0262      / 2
*2323      0261      / 1
              0260      / 0
*2354      0262      / 2
              0260      / 0
              $

```

```

/ LVDT-D-3-5-10
/ DATA TAPE
*0113      0003      / V = 3 VOLTS
*0110      2400      / F = 5 KC
*0112      0240      / R = 10 MIL
*2340      0263      / 3
*2323      0260      / 0
              0265      / 5
*2354      0261      / 1
              0260      / 0
              $

```

```

/ LVDT-D-3-5-20
/ DATA TAPE
*0113      0003      / V = 3 VOLTS
*0110      2400      / F = 5 KC
*0112      0500      / R = 20 MIL
*2340      0263      / 3
*2323      0260      / 0
              0265      / 5
*2354      0262      / 2
              0260      / 0
              $

```

Figure C-25. LISTING OF LVDT DATA TAPES.

APPENDIX D

DEVICE SELECTOR COMMANDS

Table D-1 lists the device selector commands for the system.

Table D-1
DEVICE SELECTOR COMMANDS

Mnemonic	Octal	Description
FXFD	6701	Moves fixture forward; latches; reset by RESET, FXSP, and FXBK.
FXSP	6702	Stops fixture; latches; reset by RESET, FXFD, and FXBK.
STFE	6703	Sets excitation frequency and voltage from AC; latches; reset by RESET.
FXBK	6704	Moves fixture back; latches; reset by RESET, FXFD, and FXBK.
STRT	6705	Sets ratio transformer from AC and transfers preamp input; preamp transfer. latches; reset by RESET.
SLRT	6706	Sets ratio transformer from AC and latches; unlatched by ULRT and RESET.
RFRV	6707	Reverses phase-of-reference voltage; cleared by RESET.
NDSF	6711	Skips on negative direction count from interferometer.
RSFF	6712	Resets IOT flip-flops.
	6714	Negates 670X commands.
SPR-1	6701 U 6714	Operates spare relay.
RESET	6702 U 6714	Resets the latching relays, RFRV relay, and the preamp transfer relay.
ULRT	6703 U 6714	Unlatches ratio-transformer relays.
SPR-2	6704 U 6714	Operates spare relay.
FX1	6705 U 6714	Indexes fixture but not presently used.
	6706 U 6714	Decoded but not used.
	6707 U 6714	Not decoded.
GX1	6721	Resets amplifier gain-relay matrix for nominal gain.
GX2	6723	Sets amplifier gain-relay matrix for 2X nominal.
GX4	6727	Sets amplifier gain-relay matrix for 4X nominal.