HECU-3584

UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are
not, in general, reported herein.

- PART I: STUDY PROGRAM ON HIGH-SPEED COMPUTER
- PART II: SWITCHING CIRCUIT THEORY
- PART III: MATHEMATICAL METHODS
- PART IV: ILLIAC USE AND OPERATION -
GENERAL LABORATORY INFORMATION

September, 1957

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PART I
STUDY PROGRAM ON HIGH-SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre.

1. The Summary Report

A summary report on the design of a computer has been completed and issued as Digital Computer Laboratory Report No. 80 entitled "On the Design of a Very High-Speed Computer". The summary and conclusions of this report are reproduced here:

"On the basis of the work reported herein the Digital Computer Laboratory of the University of Illinois concludes that it is feasible to construct a very fast digital computer in which the transistor circuits developed in that Laboratory would be used.

The results of two design studies are discussed. One involves a minimum of buffer storage in the form of transistor registers and is outlined in the body of Chapter 3 while the other involves a moderate amount of buffer storage in the form of a small-capacity, high-speed, random-access buffer memory and is discussed in the appendix to Chapter 3. The former design is emphasized because it is felt that its equipment requirements can be presently met.

In it two controls are used, arithmetic control and advanced control, as well as buffer storage for instructions and operands, and by such means various units of the computer are kept in simultaneous operation. For example B-modifications, memory accesses and complicated arithmetic operations such as a double-length, add-product instruction may be performed concurrently. Short but powerful inner loops may be stored outside the memory and acted upon by the control. Many of the gains in speed in the control and arithmetic unit are dependent upon asynchronous operation of these units.

The relative speed of the proposed computer compared to that of existing machines depends upon the problem being solved. For problems dominated by arithmetic operations it is estimated that the proposed computer will be 100 to 200 times faster than computers such as Illiac. For problems dominated by logical and combinatorial operations, this factor of gain in speed will be at least 50.

The proposed computer has a random-access word-arrangement memory of 8192 words of 52 bits each with an access-time of 1.5 μ s.

The arithmetic unit is designed so that the digits of a multiplier are sensed and acted upon in such a way that the use of the adder is reduced. Furthermore "carry registers" are used in this unit and carries are assimilated only when necessary. It is expected that the proposed computer will have an average multiplication time between 3.5 and 4 μ s, addition times (with assimilation) of .3 μ s and division times of 7 to 20 μ s.

The computer, aside from input-output facilities, will contain approximately 13,000 transistors, 38,000 diodes, and 42,000 resistors. The transistors are expected to be Western Electric transistors, type GF-45011.

The basic circuits built from these transistors have operation times of from 5 to 40×10^{-9} second depending upon the circuit."

2. Transistor Procurement and Testing

Nine Western Electric GF-45011 transistors were received and tested during the month. Preliminary plans were made for a production-type transistor tester in anticipation of receipt of several hundred transistors.

PART II

SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

The techniques for designing distributive circuits are being applied to the design of the control of the computer described in Digital Computer Laboratory Report 80. These techniques were described in previous progress reports. They have been used, to date, only in the design of relatively simple circuits, and the purpose of the present effort is to learn more about the difficulties involved in using them to design a relatively complicated circuit.

A partially ordered set of C-signals is set down as the initial description of the behavior of the circuit. Here, the C-signals correspond to operations which are to be performed by the circuit and the ordering relations between them correspond to chronological ordering or "causation" relations between these operations. The setting down of a chart of such operations and relations presupposes a given initial state of the circuit. In practice, however, one wishes to design circuits having variations of behavior corresponding to many initial states. To take account of such variations of behavior with the present techniques would require that a separate partially ordered set of C-signals be given for each initial state. Such a multiple listing would be prohibitive in practice, and for this reason an attempt has been made to condense all of these descriptions into the form of a single chart.

One way of achieving such a condensation is to associate each ordering relationship with the conditions under which it is valid. Thus, if the ordering relationships are represented by directed lines on the chart, one may write a Boolean condition above each which is required for its validity.

A second technique is also used to simplify the resulting chart. This involves relaxing the condition (File No. 225, page 6, point C) that if a C-signal (α, i) is in Σ , the set of C-signals, and $\alpha > 1$, then $(\alpha - 1, i)$ is also

in Σ and $(\alpha - 1, i) \leq (\alpha, i)$. If one replaces this with the weaker condition that if (α, i) and (β, i) are both in Σ and $\beta \leq \alpha$ then $(\beta, i) \leq (\alpha, i)$, one achieves a certain arbitrariness in the selection of the integers α and β corresponding to given operations. No weakening of the theory is actually produced by this change, and yet it becomes possible to make many simplifications in a composite chart of the type required to describe a complicated circuit.

Thus, experience in the design of a complicated circuit has led to the adoption of two new techniques to facilitate the handling of composite charts representing the behavior of a circuit under various initial conditions. A more efficient way of describing the handling of information is still being sought. It is also hoped that a consequence of such a method would be some way of determining which of the ordering relations among the various operations in any given description are required for the correct functioning of the circuit and which may be eliminated.

PART III
MATHEMATICAL METHODS

1. Program Library. (Supported by Office of Naval Research under Contract N6ori-07130.)

T-6 Fast Arcsine. This program uses an expression of the form

$$\sin^{-1} x = cx + \frac{a \cdot x \cdot |x|}{b - |x|}$$

to obtain values of $\sin^{-1} x$ in the range 0 to 84° which are accurate to better than a degree. Only 2.6 milliseconds are required for the calculation.

2. Numerical Methods (This work is supported in part by the Office of Naval Research under Contract N6ori-07130).

A program for finding eigenvalues and vectors has been completed which will handle matrices up to order 65. This new routine uses the drum for storage. It uses the method of Givens to obtain eigenvalues and an extension due to Wilkinson to obtain the vectors. In Wilkinson's method the eigenvectors of the tri-diagonal form are found, and a subsequent rotation by the transformation matrix gives the eigenvectors of the original. This program has the disadvantage that the vectors will not be orthogonal unless the eigenvalues are distinct.

A comparison of the speed of the present program and that of a program using the Jacobi method is given in the following table of times. In the limit of a 65th order matrix the Jacobi method is estimated to be slower by a factor of 3.

Order	Jacobi	Times (mins. and secs.)
		Givens-Wilkinson
5	00.20	00.30
10	01.30	01.40
15	04.10	03.40
30	27.45	15.30
45		41.00
55		64.00

Assuming the time is a function of the form $an + bn^2 + cn^3$, where n = order of matrix, the following coefficients were calculated.

	Jacobi	Givens-Wilkinson
a	.03	.096
b	.003	.00764
c	.000903	.000213

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During August specifications were presented for 7 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 1053. Numbers followed by T are for theses.

1053 Animal Science. Fitting "Bent Straight Line". It is frequently necessary to fit a line to data from nutrition and other biological experiments which hypothetically follow a straight line in the first part of the range of abscissas and, continuous with this line, another straight line (that is, another slope) for the rest of the range of abscissas. This problem will be solved by the computer because the abscissa of the bend point is a nonlinear function of the data in the normal equations.

1054 T Computer. Design of Circuits from a Tolerance Viewpoint. A Monte Carlo method is used to evaluate successive steps in a synthesis of circuits with component tolerances. A statistical approach is used throughout the problem to arrive at the solution which has the highest probability of satisfactory performance.

1055 Student Counseling Bureau (Chicago). Prediction of Academic Survival. All freshmen at the Chicago Undergraduate Division are given a battery of tests to determine academic survival. This type of analysis is a recurrent one since it is desirable to ultimately arrive at a method of accurate prediction.

1056 Computer. Last Moving Point Flipflop Analysis. A number of linear algebraic equations are solved giving output voltages, currents and powers of a two-transistor last moving point flipflop. The variables used in the equations are tolerances, power supply voltages, resistor values, and diode and transistor characteristics.

1057 Psychology. Personality Structure Verification and Measurement. In order to develop more highly saturated measures of objective test personality factors, Pearson product moment correlations will be obtained of intact tests with estimates of the factor score and of single digit test item scores with estimates of factor scores.

1058 Dairy Science. Analysis of Growth and Production Data from Crossbreeding. Milk and fat production data and growth data will be used to evaluate the effects of various breeding factors.

1059 Psychology. Language Community Factor Structure. Data in the form of semantic evaluations of nonlinguistic signs has been gathered from three separate language groups (Spanish, English and Navajo). It is proposed that each of the three separate collections of data be analyzed to determine the presence or absence of similarity of factor structure for these data from the language groups.

Table I shows the distribution of machine time for the month of September.

Table I

	Hrs:Min.
Regular Maintenance	24:56
Unscheduled Maintenance	:54
Drum Engineering	42:48
R.A.R.	5:09
Leapfrog	41:35
Wasted	:02

Use by Departments

Computer	28:57
Physics	4:56
Control Systems Lab.	64:18
Structural Research	119:55
Struct. Res. (AF 24994)	25:45
Theor. and Appl. Mech. (ORD 593 IC)	:03
Psychology	15:29
Electrical Engineering	3:28
Chemistry	54:26
Agriculture	19:17
U.S. Dept. Public Health	:50
Ill. Dept. Public Welfare	:08
Miscellaneous	33:10
Demonstrations	:14
	<hr/> 486:20

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for September.

TABLE III

Control Errors	3
Punch Errors	1
Drum Errors	6
Scope Errors	1
Unknown	<u>2</u>
Total	13

TABLE II

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUP- TIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
9/3/57	20:00	:00	0		:00	:41	0
9/4/57	19:58	:02	2	(1) Possibly white switch trouble (control) (2) Light out on "B" gate punch No. 4	:00	1:12	0
9/5/57	20:00	:00	0		:00	1:50	0
9/6/57	20:00	:00	0		:00	:47	0
9/9/57	20:00	:00	0		:00	1:14	0
9/10/57	20:00	:00	0		:00	1:00	0
9/11/57	18:07	1:53	1	(1) Head connector in cable to track 288 of drum shorted.	:00	:26	0
9/12/57	20:00	:00	0		:00	1:06	0
9/13/57	20:00	:00	0		:00	:42	0
9/16/57	19:44	:16	3	(1) Drum error (2) Drum error (3) Drum error	:00	1:09	0
9/17/57	19:37	:23	2	(1) Unknown (2) Drum error	:00	:50	0
9/18/57	19:59	:01	1	(1) Control error (?)	:00	:53	0
9/19/57	19:59	:01	1	(1) White switch trouble (control)	:00	1:00	0
9/20/57	20:00	:00	0		:00	:40	0
9/23/57	19:33	:27	1	(1) Unknown	:00	1:48	0
9/24/57	20:00	:00	0		:00	3:20	0
9/25/57	20:00	:00	0		:00	:39	0
9/26/57	20:00	:00	0		:00	1:02	0
9/27/57	19:57	:01	1	(1) Drum error	:02	:40	0
9/30/57	19:59	:01	1	(1) Scope error (film jammed)	:00	2:31	0
TOTALS	396:53	3:05	13		:02	23:38	0

Reports and Seminars

Seminars

"Storage and Switching by Magnetic Elements," by Dr. Jan A. Rajchman
RCA Research Laboratories, September 24, 1957.

Personnel

On May 28, 1957 the University Board of Trustees voted that the Digital Computer Laboratory be a department in the Graduate College effective September 1, 1957. R. E. Meagher was appointed Head of the Laboratory. The Department Advisory Committee consists of Professors L. D. Fosdick, D. B. Gillies, D. E. Muller, W. J. Poppelbaum, J. E. Robertson, J. N. Snyder, and A. H. Taub.

The personnel associated with the department and hence the contributors to this report are:

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Bivins, Robert L., AEC Fellow
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Clark, Miss Helen B., Secretary
Clements, Virgil F., Jr. Laboratory Mechanic
Donaghue, Hugh, NSA Fellow
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Lopeman, Harold E., Electronics Engineer for Illiac
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Mullin, Albert A., 1/2-time Research Assistant
Olsen, Warren G., 1/2-time Draftsman
Patnaik, Surendranath, 1/2-time Research Assistant
Pelg, Edmund, Jr. Electronics Technician
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Russell, Miss Ramona J., Computer Operator I
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Snyder, James N., Res. Assoc. Prof. of Physics (started Sept. 1)
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Tabb, Mrs. Susanne F., Clerk-Stenographer II
Taub, A. H., Res. Prof. of Appl. Math.
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Wenta, Joseph V., Sr. Electronics Tech. for Illiac
Wiseman, Neil E., 1/2-time Research Assistant
Yu, Hwa-Nien, Research Assistant

Student Assistants

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Parsh, Harry
Washburn, David (started Sept. 16)

University of Toronto Staff at Illinois

Smith, Kenneth C., Research Assistant

DIGITAL COMPUTER
UNIVERSITY OF ILLINOIS
FINANCIAL REPORT
SEPTEMBER 30, 1957

	DIGITAL COMPUTER	U. S. A.E.C. 415	DIGITAL COMPUTER IND. COST	SOCIAL SCIENCE RESEARCH COUNCIL	COMPUTER SERVICE	NATIONAL SCIENCE FOUNDATION	U. S. NAVY TASK 15	U. S. NAVY TASK 30	TOTAL
Free Balance	9,708.13 ¹	22,917.38 ²	2,061.85	700.00	43,533.64	25,978.08 ³	28,499.18 ⁴	17,548.58 ⁵	150,946.84
Equipment	4,291.71				49,904.80				54,196.51
Materials	1,645.25	28,813.42			98,721.87	334.93		78.45	129,593.92
Sal./Wages	25,350.92	33,164.98			168,274.29	4,821.88	750.02	58,814.99	291,177.08
Overhead		12,283.94				886.10	279.38	22,790.80	36,240.22
Workmen's Comp.		659.23				73.94	15.00	1,173.23	1,921.40
Retirement		740.35			163.20	18.07			921.62
Travel	281.40	1,356.05			1,971.01	165.95		1,565.90	5,340.31
Tele./Teleg.	16.15	64.65			1,805.00	21.05		72.65	1,979.50
Building	--	--			365.78				365.78
Totals	31,585.43	77,082.62	--	--	321,205.95	6,321.92	1,044.40	84,496.02	521,736.34

1. Through June 30, 1958 (Exp. & Wages)

2. Through November 30, 1957

3. Through August 31, 1958

4. Through October 31, 1958

5. Through June 30, 1958

Funds Expended - Previous Allowances.

1,071,907.34

Total Expenditures, 2/1/49 to date.

1,593,643.68

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Krabbe, Shirly P., Sr. Electronics Tech. for Illiac
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The Department Advisory Committee consists of Professors L. D. Fosdick, D. B. Gillies, D. E. Muller, W. J. Poppelbaum, J. E. Robertson, J. N. Snyder, and A. H. Taub.