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Beam Lead Device and Hybrid Microcircuit Testing

Presented by Dr. R. E. Markley

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Product Testing Technology
and Automation Seminar

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INTRODUCTION

The growth of the hybrid microcircuit-thin film technology has been phenomenal in the last few years. This growth may be directly related to the space saved by employing this technology rather than its older cousin, the printed wiring board technology, and by the increasing availability of thin-film material, equipment and component chips. A hybrid microcircuit is the interconnection of unpackaged components (semiconductor chips) on a ceramic substrate by a thin metal film sputtered on the substrate surface. Such a microcircuit requires considerably less assembly space in the final product than does an electrically equivalent printed wiring board assembly.

In the past, the fabrication of hybrid microcircuits has typically been a closed-loop process where the microcircuit manufacturer also controls the fabrication of the semiconductor chips. The open exchange of information between the chip and circuit fabricating areas has been cited as an important factor contributing to the success of the Safeguard Program at both Texas Instruments and Motorola.

What of the manufacturer, then, who does not manufacture semiconductor chips, but does plan to manufacture hybrid microcircuits in large quantities--what testing processes should be established to insure a smooth and reliable flow of multi-vendor chips to the hybrid microcircuit bonding area, and what additional testing processes must be developed in order to test the hybrid microcircuits? These questions were posed to Bendix more than two years ago, and constituted the basis for the automatic handling and testing processes which will be outlined in this paper.

COMPONENT TESTING PROCESSES

The hybrid microcircuit components which posed testing problems fell into two physical categories: semiconductor or beam lead device (BLD) chips, including transistors, diodes, zeners, uni-junction transistors, and resistors; and packaged metal-oxide-semiconductor large-scale-integration (MOS/LSI) circuits. The BLD chips posed severe handling problems, whereas the MOS/LSI circuits presented considerable testing problems.

BEAM LEAD DEVICES

The conclusions and recommendations resulting from a short term process development study indicated that BLD chips must be purchased from device suppliers in etch-separated arrays. Since the devices are precisely located in an etch-separated array, they can be automatically positioned, probed and tested in large quantities if the necessary probing and testing equipment is developed and linked together to form a composite BLD test system. The proposed method of purchase, BLD chips in etch-separated arrays, was not the existing method of supply practiced by device manufacturers because device yield would then be revealed to the customer. Instead, the manufacturer supplied the customer with vendor-tested good devices randomly oriented on glass slides; this shipping method prohibited automatic probing and testing by the customer.

The recommended method of BLD purchase and the proposed development of a compatible BLD probe/test system were presented to both Bendix Kansas City and Sandia Albuquerque personnel. Sandia had concurrently been exploring the possibilities of a BLD carrier which could hold the BLD and also establish contact with the beam leads when perfected. A decision was made to pursue both proposed BLD handling/testing processes, with Bendix continuing the development of the etch-separated array technique and Sandia pursuing the development of a BLD carrier.

The Etch-Separated Array

An etch-separated array of beam lead devices consists of some 2000 to 3000 devices precisely located in a 1.5 to 2.0 inch diameter array as depicted in Figure 1. The array is formed by placing the unetched silicon wafer face-down on a wax-covered sapphire disk. The wax serves as the necessary holding medium. The wafer is lapped to a thickness of approximately 2 mils, photo techniques are employed to establish the grid pattern for etching, and the devices are then chemically etch-separated. The leads of each separated device are interdigitated with the leads of adjacent chips which maximizes the number of devices formed on the wafer, but tends to complicate automatic sorting processes following electrical testing.

The BLD manufacturer typically performs DC testing of each device in the array. All electrically rejected devices are inked to facilitate manual device sorting. A section of a vendor-tested array is depicted in Figure 2. The probe marks and ink dots are visible on the chips. Following testing, the manufacturer neutralizes the wax and manually sorts to eliminate rejects by randomly placing the good devices on a glass slide for shipment to the customer. However, this shipping method excludes automated device testing by

Figure 1. Etch-Separated BLD Array

Figure 2. Array Section, Probed and Inked

the customer. The etch-separated array, vendor-tested and inked as shown in Figure 2, does provide the necessary prerequisite for automated customer testing.

Negotiations with Texas Instruments, Motorola, and Raytheon led to agreements for the purchase of beam lead devices in etch-separated arrays. The purchased arrays are vendor-tested and device samples are randomly removed from the array for further testing prior to array shipment.

The Probing System

Specifications for a high volume BLD array probing system were drafted and presented to Teledyne TAC and Electroglas, two of the major probing equipment manufacturers. A purchase order was released to TAC for the development of the system. A review of the final specifications, a review of the development progress, and a preliminary system prove-in per Bendix specifications were all conducted at TAC. Final system prove-in was conducted at Bendix.

The probing system consists of two units, the base prober depicted in Figure 3 and the peripheral control unit shown in Figure 4. The system may be characterized by the following features and capabilities:

- The system can accommodate any array size up to 3 inches.
- The devices may be probed with either probe cards or adjustable probes.
- When interfaced for synchronous operation, the system can position and contact over 40,000 devices per hour, assuming zero loading and testing times.
- The system may operate in any one of four modes: (1) manual, for operator setup; (2) automatic sequential testing, for sequential positioning and probing of BLD chips synchronized with chip testing; (3) automatic selective retesting, for selective retesting of chips based on previously established test classifications; and (4) automatic selective inking, for stand-alone chip inking based on previously established test classifications.
- A high-speed punch and reader are available for punching or reading the device test classification and the corresponding XY coordinates of the device.
- One-to-one even parity error checking codes are used with error detection, correction, and clearing capabilities.

Figure 3. Base Prober

Figure 4. Peripheral Control Unit

- Programmable features include XY device index sizes, reference chip XY coordinates, read class, write class, and ink class.

The BLD Test System

The BLD test system consists of the TAC PS-100 probing system interfaced to the Lorlin Impact-100 Test System as depicted in Figure 5. The Impact-100, shown in Figure 6, is a PDP-11 computer-controlled, discrete semi-conductor test system with the following features and capabilities:

- This test system is designed to perform DC, pulsed DC, and AC tests on transistors, diodes, and SCR's.
- The system can be programmed for a limited degree of FET parameter testing.
- Five-station simultaneous operation is possible with a station-assigned teletypewriter, or each station may have a dedicated teletypewriter.
- Device types, polarities, go/no-go testing and datalogging may be freely intermixed among the stations.
- Device test programs may be created on-line with no interruption of testing.
- All communication between the system and the operator is in simple English through the teletypewriter.
- The Impact-100 contains a high speed punch and reader for datalogging, programming, and program storage.

The initial hardware and software interfacing between the TAC and Lorlin systems was developed by Lorlin per Bendix specifications. Final interfacing was conducted at Bendix. The probing system was interfaced to MULTIPLEX STATION 3 of the test system. Collector, base, and emitter Kelvin leads which compose the test cable are terminated through supressor coils approximately six inches from the device probe tips. The test cable between the two systems is about 14 feet long. A data correlation study between the main test station, STATION 1, and STATION 3 was conducted satisfactorily using both probe cards and adjustable probes at STATION 3.

The interaction between the two systems is synchronous where an operating cycle is initiated by a TEST START signal generated by the probing system which has contacted a device for testing. The test system performs the programmed test sequence on the device, establishes a device test classification by generating a TEST COMPLETE signal and TEST CLASS data for the probing system.

Figure 5. BLD Test System

Figure 6. Semiconductor Tester

The probing system acts on the returned signals in a programmed sequence which may consist of both device inking and punching of device classification and coordinates, followed by the automatic positioning and contacting of the next selected device in the array which concludes a BLD test system operating cycle.

The BLD test system can currently test transistors, diodes, zener diodes, SCR's and resistors. Many transistor and diode arrays have already been tested on the system with very satisfactory results. The observed system throughput was in excess of 3,000 devices per hour which included 12 tests per device with 100 percent datalogging on the high speed punch. The throughput of the system is directly a function of the number of tests performed on each device and the quantity of test data which is logged on punched tape.

Device variables test data can be logged directly by system tape punch, or the data (including the device XY coordinates) can be logged on a Semiconductor Test Acquisition and Control System (STACS). STACS is a PDP-11 computer-controlled, disc-operated system with auxiliary magnetic tape storage. The disc memory capacity is in excess of ten megawords while the seven-channel magnetic tape unit can accommodate 2400 feet of tape for additional storage. This system functions as a data compiler, processor, and analyzer. Raw data from the BLD system are readily converted to statistical variables, or moon-maps may be plotted on the STACS line printer. The moon-map, a plot of the tested array of chips with each chip position symbolized by a pass or fail character, provides an immediate visual overview of the array quality.

Probing Beam Lead Devices

The probing or contacting of a BLD within the array is depicted in Figure 7 where the probe tips of the probe card are in contact with the leads of the device. Since the pattern formed by the tips is designed to match the beam lead pattern of the device, two associated conventions have been established in conjunction with the design and fabrication of probe cards. First, the array is always placed on the prober vacuum chuck with the distinguishable beam lead of each device pointing forward toward the operator. Second, the usable paths forming the sunburst pattern on the probe card are divided into collector, base, emitter, and edge sensor families to permit a universal card interconnect with the test system. These conventions give the card fabricator considerable flexibility in physically locating the collector, base, and emitter probes on the card, and insure that the probes of any card which is inserted into the card holder/connector are correctly connected to the test system. The edge sensor probe tips are always connected to the same two card paths which insures correct sensor connection to the probing system.

Figure 7. Probing the BLD Array

Individually XYZ-adjustable probes may be used to probe the leads if a probe card is not available. In such a case, a separate probe mounting ring is used. Each probe may be connected to either the collector, base, or emitter test leads by separately connecting each probe lead to the correctly colored socket located on the probe ring adapter card. The adapter card also contains the suppressor coils which terminate the Kelvin test leads.

When the probe tips contact the beam leads, the resulting scrubbing effect leaves a depression on the beam leads as depicted in Figure 8. A lead degradation study was conducted to answer the following questions: 1) what is the optimal tip force which should be used during probe testing, and 2) how many times can the leads be probed before lead bond integrity is jeopardized. The study was conducted using both probe cards and adjustable probes. In both cases, twenty-five categories were developed with a minimum sample size per category of sixty. The two independent variables per category were tip overtravel and number of contacts. The overtravel was varied from one to five mils in one-mil increments, and the number of contacts per lead was also varied from one to five. The tungsten probe tips were designed for a contact force of four grams per mil of overtravel and a nominal 1.5 mil tip diameter. A typical case of selective lead degradation is depicted in Figure 9 where the beam lead has been probed three times with a tip overtravel of two mils. The conclusions of this study verified the results of an earlier study at Bendix where optimum tip overtravel was found to be between two and three mils, and the permissible number of times which the beam lead could be probed was found to be four contacts.

A second study was conducted to determine the maximum current which could be safely forced through the probe tips before permanent damage such as tip carbonization occurred. A ceramic substrate containing gold paths was used to simulate the beam lead. The independent variable in this study was the amplitude of the current pulse. The width of the current pulse was fixed at one millisecond. The tungsten probe card tips were able to support a pulse current of 200 milliamperes before a permanent upward shift in contact resistance was detected at 250 milliamperes. The experiment included more than 1000 contacts and fixed amplitude current pulses occurring at the minimum cycle time of the system. The conclusion drawn from this study was that the tips can support 200 milliamperes, one millisecond current pulses provided the voltage drop resulting from the contact resistance does not hinder the interpretation of the test data. The contact resistance can become a significant factor since the contact resistance per tip was found to be about 150 to 200 milliohms. Additionally, the contact resistance from tip to tip can legitimately vary by a factor of four because a 1.5 mil nominal tip diameter has a fabrication tolerance of ± 0.5 mil.

Figure 8. Probed Beam Leads

Figure 9. Selective Lead Degradation

Sample Testing

While the developed BLD test system possesses the capability of high volume, 100 percent and selective device testing, certain device tests cannot be performed by this system. Examples of such tests are high current tests, HTRB tests, and power burn-in tests. To conduct such tests on beam lead devices, samples are removed from the array and bonded on transistor headers such as the one illustrated in Figure 10. The combination of probe testing data and sample testing data is used to measure the integrity of the BLD lot which is usually composed of one or more BLD arrays, all from the same wafer run.

The device samples, bonded on headers, constitute a destructive process since the devices cannot be used as pieceparts in support of production. One potential application of the BLD carrier, now being developed at Bendix as a process development activity is the creation of a non-destructive BLD sample testing process. A prototype model of the BLD carrier is a modified version of a Barnes 029 carrier (Figure 11). The clamp, inserted and engaged in slots in the carrier, serves to hold the beam lead device in position and provides the contacting force between the leads and the carrier paths. The carrier is designed to be compatible with existing handling and fixturing equipment.

Sorting and Visual Inspection

Once the beam lead devices are tested on the BLD test system, the next step is device sorting and visual inspection. The objectives of this phase of the process are to transfer electrically good devices from the etch-separated array into a second array, and to perform a visual and dimensional inspection of the transferred devices.

A semi-automatic BLD transfer system (Figure 12) was developed by TAC per Bendix specifications. A tested array of etch-separated devices is placed on a temperature-controlled input chuck. The chuck temperature is elevated to soften the wax, but not to the extent that would permit drifting of the oriented devices. An uninked device is positioned for pickup and a foot switch is depressed. A heated vacuum collet contacts the back of the chip for a controlled period of time, the vacuum is enabled, and the collet is raised and rotated 90 degrees to the chip placement position at the temperature-controlled output chuck. The collet is lowered and the chip is placed on a glass slide resting on the output chuck. A positive pressure is enabled through the collet to aid chip detachment during placement and to purge the collet following placement. After placement the output chuck is indexed a programmed distance and the collet is returned to the home position which completes a transfer cycle. A section of an

Figure 10. BLD Sample Testing

Figure 11. BLD Carrier

Figure 12. BLD Transfer System

expanded array of transferred devices which is built on the glass slide is shown in Figure 13. The residual wax which remains on the chip during transfer serves as the holding medium between the chips and the glass slide. Depending on the source of the purchased devices which determines the wax characteristics, about 300 devices per hour can be transferred.

An automatic BLD transfer system has now virtually replaced the semiautomatic system, with an increase in the transfer throughput from 300 to 1000 devices per hour. The automatic system functions similarly, except the unit is controlled by the test classification/XY coordinate tape generated by the BLD test system. Devices per test classification are automatically positioned for transfer based on the XY device coordinates. The automatic system also has a front-side and back-side visual inspection capability, plus a programmable output chuck.

To have an additional degree of control over the wax of the etch-separated arrays, an ashing system similar to the one depicted in Figure 14 is utilized. The ashing unit has a five-inch chamber within which an rf-excited oxidizing atmosphere can be developed. With an etch-separated array located in the chamber, the developed atmosphere reduces the quantity of wax on the array. The degree of reduction is a function of energy and time, both of which are controllable.

Visual and dimensional inspection of chips in the expanded array is performed on the microvideo system depicted in Figure 15. The magnified image of the chip is displayed on a viewing screen for inspection. Programmable lines may be superimposed on the image to measure the various dimensions of the chip. Following visual inspection the expanded BLD array is stored or shipped to the microcircuit bonding area. The complete BLD receiving inspection process is depicted in Figure 16.

MOS/LSI CIRCUITS

The incorporation of an LSI circuit into a product design permits many digital tasks to be compressed into one package. For example, the estimated gate complexity of the MOS/LSI circuits which require testing at Bendix Kansas City is approximately 2000 gates. If these 2000 gates were all of the quad-two input NAND variety, then 500 integrated circuits and the interconnect wiring would be required to duplicate the LSI circuit functions. The assembly space required for 500 integrated circuits is obviously much greater than that required for the LSI package.

Since an LSI circuit encompasses a vast number of logic functions, the test requirements placed on such a component are also of the same magnitude. Additionally, since the circuit represents a

Figure 13. Expanded BLD Array

Figure 14. Ashing Equipment

Figure 15. BLD Visual Inspection Equipment

Figure 16. Complete BLD Receiving Inspection Process

considerable investment, protection of the circuit, including its cantilevered leads, is essential.

LSI/Hybrid Carrier

The circuit is protected during handling and testing by a Bendix-designed carrier (Figure 17), which is used for both the LSI circuits and the next assembly hybrids. The design permits automatic feeding, Kelvin contacting, and device serialization up to 9999.

LSI Test System

The LSI test system (Figure 18) is a Fairchild Sentry 600 System and a double Delta chamber. This system may be characterized by the following features and characteristics:

- The double Delta chamber serves as a preconditioner chamber and a test chamber. When the carriers are placed in the chamber magazines, all handling is automatic and under the control of the Sentry 600.
- Each carrier serial number is detected by the combined use of fiber optic light pipe, carrier code holes, and photo sensors.
- The test head can accommodate a maximum of 60 active LSI leads or pins. Each pin has dedicated drivers and load electronics located on the test head performance board (Figure 19).
- The test head pin electronics is directly controlled by the high-speed control unit. This unit contains a 60 by 1024-bit RAM which is loaded from the main computer. The 60-bit words and the word sequencing controls the testing of the LSI via the pin electronics.
- The main computer is the working memory of the system and consists of 16K of memory structured for 24-bit words.
- The computer may be programmed from card reader, magnetic tape, magnetic disc, or video keyboard. Both the tape and the disc (Figure 20) have direct memory access to the computer. The programming language is FACTOR, which is closely related to FORTRAN.
- The tape unit consists of one deck for programming and a second deck for test data storage. Both decks can accommodate 2400-foot reels, and nine-channel heads permit an 800-bit/inch/channel read/write density.
- The system also includes a line printer for on-line hardcopy recording.

Figure 17. LSI/Hybrid Carrier

Figure 18. LSI Test System

Figure 19. Ambient Test Head

Figure 20. Syster I/O Equipment

The system performs fault tests, DC parametric tests, switching time tests, and functional tests. The test rate for the MOS/LSI circuits is 250KHz due to the high input impedance of the circuits, although the system is designed for a maximum test rate of 5MHz. A typical number of microtests performed on each LSI circuit is on the order of 1,750,000. The MOS/LSI system can completely test and datalog such an LSI circuit in about 12 minutes.

HYBRID TESTING PROCESSES

The hybrid microcircuit (Figure 21) is formed by bonding the component beam leads to the thin film metallization which has been sputtered on the ceramic substrate. When circuit fabrication is completed the unit is secured in a carrier and is then ready for electrical testing. Some types of hybrids require active trimming in addition to or in conjunction with electrical testing. Thus, a hybrid will see at least one automatic testing process and sometimes two processes in order to pass electrical inspection.

ACTIVE LASER TRIMMING

The active laser trimmer (Figure 22) is a PDP-8E computer-controlled system, which trims the tantalum nitride resistors on the hybrid microcircuits for preselected values of output functions such as voltage, current, frequency, and time interval. The hybrid microcircuits are mounted on a two-position handler. Each half of the handler is swung 180 degrees to place the part under the YAG laser. If closer alignment is required, a software routine in conjunction with a TV viewing system and a joystick is used to correct any remaining X, Y and θ errors.

The laser beam is positioned with an XY table driven by stepping motors. The positioning resolution is 0.3125 mils. The TV camera is mounted on top of the XY table and looks through the main objective lens of the laser. A crosshair in the TV camera is aligned to the laser spot.

All loads, input connections, and monitoring connections are mounted on or plugged into the probe ring (Figure 23). All interconnections can be easily moved since neither soldering nor splicing is required.

The measurements, inputs, laser firing, table speed, and table direction are controlled by the computer. The complete computer system consists of the 16 thousand word memory computer and a 1.6 megaword disc. Trim programs are written in FORTRAN. These programs contain information on each circuit transfer function and related trim resistor, and permit predictions on the length of cut based on measurements taken prior to laser firing. These

Figure 21. Hybrid Microcircuit

Figure 22. Active Laser Trimmer

Figure 23. Trimmer Probe Ring

predictions allow rapid trimming of short duration events with long duty cycles. Also, since the trimmer does not power up or monitor the circuit while the laser is firing, interference resulting from reflected laser light beaming on sensitive semiconductor devices near the resistor is eliminated.

All operator/computer interface is managed by the operating system. The operator may select either a manual mode or an automatic mode of operation. The manual mode allows the operator to determine the length and direction of the trim. This mode is typically used for rework and development, while the automatic mode is used for production trimming.

A hybrid received at the system usually requires about five cuts. With a cutting rate of about 50 mils per second and a beam width of approximately 0.5 mils, the time required to trim a hybrid is between one and two minutes. A conservative estimate of trimming throughout is 250 circuits per day. This estimate includes both setup time and downtime.

HYBRID ELECTRICAL TESTING

The hybrid microcircuits are electrically tested on both an in-house test system (Figure 24) and a test system designed at Sandia Albuquerque. Both systems are fully automated and are quite similar to each other. With a few exceptions, both systems possess the following features and characteristics:

- The automatic handling and contacting, and the test temperature environment are realized by a triple Delta chamber. This chamber is similar to the MOS/LSI chamber, except that both preconditioning and postconditioning temperature gradients are programmable.
- The chamber test head contactor can establish Kelvin contact simultaneously with 76 hybrid leads, if necessary.
- Each type of hybrid has a dedicated test head adapter. Sets of addressable 8-bit by 32-word ROM's are used within each adapter to control all line switching and loading requirements.
- Some types of hybrids may also be contacted for testing at a second station consisting of a probing unit. This station is presently used to contact/test hybrids which are not fully assembled.
- The heart of the system is a HP2100 computer with 16K of memory. The memory size is increased by a 2.5 megaword disc memory where acceptance test programs, first functional check

Figure 24. Hybrid Test System

programs (pretrim testing), pretrim data, and calibration programs are stored.

- Multiprogrammer units are used to extend the number of computer I/O slots. Each unit contains a maximum of 15 control cards, each of which may be used to control data routing, force/sense instrumentation-to-test line switching, test station-to-test line switching, or the temperature chamber. Both the multiprogrammer units and the cards are computer addressable.
- Some of the force/sense instrumentation within this system includes three programmable and eight fixed power supplies, programmable pulse generator (variable repetition rate, delay, amplitude, offset, rise time, and fall time), digital voltmeter (voltage, resistance, and sample/hold), and a counter/timer (10MHz time base with a 10 ns resolution via time interval averaging).
- The system contains a video keyboard for operator interaction, a line printer for hardcopy data output, and a tape punch for program maintenance.

A total of 86 hybrids can be loaded into the carrier magazines at any one time. The hybrid load is preconditioned in the upper Delta chamber where both temperature gradient and soak time are program controlled. When the soak time requirement is satisfied, the first carrier is dropped into the test chamber and forced into contact with the test head contactor. The carrier/hybrid serialization is detected at this time, followed by the electrical testing of the hybrid. Following testing, the carrier is retracted from the contactor and dropped into an accept or reject magazine located in the postconditioning chamber. The sorting operation is directly a function of the test results. The next carrier is then dropped into the test chamber and the cycle is repeated.

The system throughput is about two minutes per hybrid in the test chamber. This two minutes includes only about one second of power-on time, with the remaining portion consumed in system housekeeping chores. If 86 hybrids are loaded into the preconditioning chamber, the system throughput (including preconditioning, soak, postconditioning and testing at ambient plus two other temperatures) is 86 hybrids in about 7 hours, or 5 minutes per hybrid. The estimated monthly throughput is 1500 hybrids, including hybrid retesting and system downtime.

CONCLUSIONS

Two levels of automatic testing processes have been developed and are operational at Bendix Kansas City. These processes are

dedicated to the support of high-volume hybrid microcircuit production. Process development activities are presently underway to expand both process levels to include rf component and rf hybrid testing.

Some of the development activities being conducted in the rf component area include rf small signal transistor handling and testing, low picofarad rf diode junction capacitance measurement, and rf power transistor testing. The first two activities are concerned with the development of automatic processes, whereas the third area is directed toward broadband impedance matching in conjunction with high power testing.

The development activities in the rf hybrid area are directed toward automatic rf handling and testing processes, including environmental testing.