UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are
not, in general, reported herein.

- Part I: Study Program on High Speed Computer
- Part II: Mathematical Research and Programming
- Part III: Mathematical Analytical Program
- Part IV: Illiac Use and Operation -
General Laboratory Information

September, 1956

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PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415. This contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contract N6ori-07130 and Contract N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computing Centre and Department of Physics.

High Speed Memory

Conventional magnetic-core memories have cycle times not shorter than about 6 microseconds. The main factor fixing this minimum time is the limitation placed on the currents used by the method of selecting a particular core to read or store information. Figure 1 without the dotted lines shows one digit-plane of a con-

Figure 1. Digit-Plane Windings
(Sensing winding not shown)

ventional memory. Figure 2 shows the waveform of currents in one X and one Y winding and in the Z winding which passes through all cores of the digit-plane.

Figure 2. 2:1 Selection Ratio
(Full line rewrite 0
Dotted line rewrite 1)

The core at the intersection of the chosen X and Y winding has a resultant current I during the "read" pulse as shown in the bottom graph. Any other core on the chosen X winding or Y winding will have a current $I/2$ which must not be sufficient to alter permanently the magnetic state of the core. Thus the "selection ratio" (i.e. the ratio of current in the selected core to the maximum current in any other core) is 2:1. On the "rewrite" pulse the Z winding carries a current of 0 or $+I/2$ depending on whether a "1" or a "0" is to be stored. Again the selection ratio is 2:1.

Methods of arranging windings to give an $n:1$ selection ratio have been suggested¹ and some work has been done with a 3:1 ratio,² but no attempt has been described to apply these methods to the design of a memory faster than 6 microseconds.

One arrangement giving a 5:1 selection ratio is shown in Figure 1 with the dotted lines and Figure 3. The X, Y, and D windings are so arranged

Figure 3: 5:1 Selection Ratio

1. Minnick and Ashenhurst, J. Appl. Physics, 26:575 (1955).

2. National Bureau of Standards Report, Program on Computer Components, October, 1954-March 1955.

that one winding from each set passes through the selected core and that no other core is threaded by more than one of these windings. The Z winding carries a current $-I/2$ during the "read" pulse and the chosen X, Y and D windings carry a current I . As can be seen from Figure 3 the resultant current through the selected core is $5/2 I$, while the currents in other cores are 0, $I/2$ or $-I/2$. Thus the selection ratio is 5:1. When the selection ratio is higher, then the net driving currents are larger and the turnover time is shorter.

A somewhat different way of overcoming the current limitation is the "word-arrangement" memory,^{2,3} illustrated by Figure 4 and Figure 5. In this

Figure 4. Word Arrangement

Figure 5. Word-Arrangement Pulses

2. See footnote on page 2.

3. J. M. Wier, A Dynamic Magnetic Core Memory, Report 54, Digital Computer Laboratory, University of Illinois, January, 1953.

arrangement one winding (marked W) passes through cores representing all the bits of a single word. In reading information from the memory the current through the appropriate W winding is not limited by any selection ratio. In rewriting the selection ratio with the waveforms shown would be 3:1.

Many variations of these arrangements are possible and with each of them the reduction in time is accomplished at the expense of more driving equipment, higher power, and in some cases more complex wiring of the memory cores. The most promising of the memories studied so far is the "word-arrangement" memory. Provided rather serious problems of current regulation and heat dissipation can be overcome a cycle-time of two to three microseconds seems possible.

Switching Properties of Magnetic Cores

In designing circuits involving storage cores or switch cores it is usual to use time-average values of output voltage, effective magnetizing resistance, etc. Actually these quantities vary widely during a cycle even with constant switching current. Some experiments are being carried out in an attempt to obtain a better approximation to actual properties of ferrite cores which is still simple enough to use in design problems.

Eccles-Jordan Flipflops

A study has been made of Eccles-Jordan type flipflops to find a set of circuit constants which would meet a set of tolerance conditions using the SB-100 surface barrier transistors. A program was written for Illiac to do this. This program was reported on at the Association for Computing Machinery in August, 1956.⁴ The restrictions which were imposed were:

- 1) resistor tolerance $\pm 2\%$,
- 2) power supply voltage tolerance $\pm 3\%$,
- 3) nominal positive supply voltage 25v,
- 4) minimum collector voltage 0.1v (to prevent saturation),
- 5) minimum binary signal 2v,
- 6) SB-100 transistors, but no diodes,

⁴ G. H. Lechner, Report 72, Digital Computer Laboratory, September, 1956.

- 7) signal output load up to 0.5 ma,
- 8) alpha range 0.92 to 0.95 in one series of tests,
- 9) maximum collector voltage 20v,
maximum collector dissipation 30mw,
maximum collector current 5 ma.

With all of these restrictions it is believed that a design does not exist. However, if the maximum collector current or the maximum collector dissipation is increased a design could be found. Figure 6 shows a plot illustrating these things. Similarly if α could be restricted to 0.95 to 0.98 a design could be found.

These remarks provide an example of using the Illiac to find designs of these relatively straight-forward circuits.

The NOT circuit has been studied from an experimental standpoint using the surface barrier transistors. This is very similar to the flipflop problem, of course.

Figure 6. Region of Possible Flipflop Designs

Test Equipment for Fast Circuits

A number of units of test equipment have been assembled and tested which can be used to observe the operation of dc coupled circuits. A listing of these units follows.

EFP-60 Pulser. Characteristics:

Output pulse +1v into 93 ohm cable at +150v level
50 μ s duration with rise time less
than 8 μ s

Synch. pulse separate output +0.5v into 93 ohm
cable at ground level

The circuit uses an EFP-60 with plate to cathode feedback. The free dynode is used as the output terminal and a full 6J6 cathode follower provides a separate synchronization pulse output. Degenerative dc feedback is applied to the grid of the EFP-60 to increase the amplitude stability. The circuit is constructed in a small brass chassis with very short leads. The supply voltages required are the same as the amplifier to be described later.

Relay Pulser. A pulser using a Western Electric 275C mercury wetted relay was constructed. The duration of the pulse is determined by the length of coaxial cable used, and the repetition rate is 100 cps maximum. Pulses up to 10v have been formed with rise times less than 4 μ s.

A second relay pulser was built in which the relay was disassembled and mounted in a coaxial structure. This provided a better match to the lines since the relay as originally built by Western Electric has leads inside about two inches long. No decrease in rise time was observed with the second pulser but this was probably due to the 150 feet of RG-62/U cable which is necessary to delay the pulse to allow for the start of the sweep.

A low loss large diameter coaxial cable with $Z_0 = 47\Omega$ was built to permit the fastest possible pulse from the relay pulsers even though such rise times cannot be observed at present. This coaxial cable may be used directly with the second relay pulser or with the first one with suitable modification of the matching network.

Display Equipment. In order to be able to observe the waveforms of fast transistor circuitry a wide band distributed amplifier was built using four EFP-60's.

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Characteristics:  .Gain      10 output not terminated
                  .          5 output matched
                  .Rise Time  8  $\mu$ s
                  .Output     positive 10v maximum
                  .          negative 20v maximum

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The "delay lines" consist of 10 foot sections of RG-62/U cable with matching sections at each tube connection. DC feedback is applied to each tube to stabilize the current and, therefore, to a first order the gain of the amplifier.

A cathode follower using a 6BC4 triode, $g_m = 10,000$, with a gain of one-half was also constructed to drive the amplifier. The input capacity of this unit is 10.5 uuf direct and 6.5 μ pf with a 2:1 attenuator. Series peaking is employed in the input to the cathode follower so an over-all rise time of 8 mps is preserved for the amplifier with cathode follower direct, and 6 mps with the 2:1 attenuator is obtained.

Boolean Studies on Speed-Independent Circuits

A. Since speed-independent distributive circuits may be completely characterized by an initial state and a set of Boolean functions describing the nodal behavior, an investigation has begun to make possible the synthesis of the functions producing a circuit with prescribed behavior. The process of synthesis will be programmed for the Illiac to provide a useful tool for the circuit designer.

The development is through lattice theory and is begun by showing that the set of signals in a circuit completely characterizes a C-state diagram which is distributive. In general a speed-independent circuit may either cycle or reach equilibrium. In the latter case the partially ordered set of signals is finite while in the former it is countably infinite. However, a cycling circuit will eventually repeat (i.e., the C-state lattice will have a repetitive structure) so that the partially ordered set may be written in a finite manner by listing the coverings by congruences. At present methods of characterizing this partially ordered set are being studied with respect to ease of interpretation by a digital computer program.

B. The present library program (Q - 3) used for analyzing complete circuits for speed independence will be replaced by a more useful and more complete program. The new program will have the following characteristics:

- (1) up to 78 nodes will be allowed;
- (2) a cycling detection test will be provided;
- (3) auxiliary equations not corresponding to nodes may be employed;
- (4) a state may be designated as disallowed and a stop will occur if this state is attained;
- (5) output indicating semimodular, distributive or totally sequential circuits will be more completely indicated.

The program will make use of the magnetic drum, incorporating a number of checks such as sum checks and overwriting tests. The compiler is now almost complete.

Relative Memory Sizes. Sorting

One of the important problems arising in connection with relative sizes of fast and slow memories is the sorting problem. A proper solution to this problem will affect design considerations. We consider here a method which minimizes accesses to the slow speed store.

Consider a random access memory (called core memory) and a serial memory (called drum memory). Let N_p words to be sorted be held initially on the drum and suppose that N is the number of words which, held in the core memory, can be correctly sorted into relative order among themselves without additional storage space.

A. Separate the words to be sorted into p N -word blocks $N_1, N_2, \dots, N_p$ in any manner (presumably as they occur), read N_1 into the core memory and mesh it in blocks of $1, 2, \dots, N/2$. Store the sorted block N_1 back on the drum and repeat for $N_2, \dots, N_p$.

B. Next divide each of the sorted blocks N_i into k equal blocks $N_{i1}, N_{i2}, \dots, N_{ik}$ each of size N/k where N_{i1} are the N/k largest elements of block i (in correct order), N_{i2} are the N/k next largest elements, etc.

Read N_{i1} , $i = 1, 2, \dots, p$ into the core store, marking the last word of each block in some way. Mesh these into correct order by successive meshes of pairs of blocks, pairs of results, etc. This new sequence Q_1 , correctly sorted, has the property that if X_1 is the first element in Q_1 which was a

last element of any block N_{i1} , then X_1 and all larger elements are sorted into their final order, for each is larger than any element in N_{ij} for $j \geq 2$ since each is larger than the last (smallest) element in N_{i1} . This in turn is larger than any element in N_{ij} for $j \geq 2$ because N_i is in its correct order. Thus the elements X_1 and above may be stored away on the drum in their final form.

If X_1 was the last element of N_{i1} , read in block N_{i2} and also, if space permits, read in a number of other blocks N_{j2} which are going to run out soon (i.e., whose last element in the core memory is near X_1). The resulting blocks are first meshed among themselves and then meshed with the previous list beginning with the word after X_1 . This new ordered list also has the property that the elements beginning with the last element of the first block N_{ij} to run out and running up to the maximum are correctly ordered in their final form and may be stored on the drum. This process is continued until the meshing of $N_1, N_2, \dots, N_p$ has been completed.

This process, if drum transfers are disregarded, is an $N \log N$ method. It requires 2 drum reads and 2 drum writes per number. If the average waiting time for one block N_{ij} is assumed to be 8 to 24 ms (the time to read 1,000 to 3,000 words), this system has the advantage that if k is correctly chosen we read about $k/2$ blocks, thus reducing the waiting time to get the first two blocks out to from $8/(k/4)$ to $24/(k/4)$ milliseconds. After that the first steps in the meshing process can continue during waiting time for the drum.

The problem is to choose the optimum k for given N_p . This should be done so that the average amount of sorted data written on the drum at each writing period (B) is about half the data since meshing is most efficient if blocks have equal size. A Monte Carlo model has been constructed for experimenting rapidly with random numbers on the Illiac to test the efficiency and to develop empirical rules for finding k .

The method applies to meshing N_q numbers out of a set of N_p numbers, so another possibility is to do the meshing in several stages. The results of the experiments will be used to decide whether or not this is useful.

Register Number Study

The variations of the multiplication-addition operation, $a * b + c$, suggested by several numerical computations, have been summarized into the following 3 cases:

- (1) (a) and (b) vary; (c) is fixed;
- (2) (a) and (b) are fixed; (c) varies;
- (3) (a) and (c) are fixed; (b) varies;

where (a) denotes the address of a, etc. Examples of calculations which might use these variations of $a \cdot b + c$ and orders for representing them are as follows.

A. Scalar Multiplication: $\sum_k a_{ik} b_{kj}$. The numerical computation would be carried out as: $\text{----- } a_{13} b_{31} + [a_{12} b_{21} + [a_{11} b_{11} + 0]]$. Here (a) and (b) vary; (c) is fixed. The orders for carrying out this calculation would be:

51 (n)
 MS_i (m) : (1) $[Q \cdot m + 2^{-39} A] + S_1$
 (2) $A \longrightarrow (S_i)$
 (3) $Q \longrightarrow (A)$

The address (m) specified the multiplicand.

B. Polynomial Evaluation: $\sum_{i=0}^n a_i x^{n-i}$. The numerical computation would be carried out as: $\text{----- } x [x [x a_0 + a_1] + a_2] + a_3 \text{-----}$. Here (a) and (b) are fixed; (c) varies. The order for carrying out this calculation would be:

NS_i (n) : (1) $[Q \cdot S_1 + 2^{-39} A] + n$
 (2) $A \longrightarrow (S_i)$
 (3) $Q \longrightarrow (A)$
 (4) reset Q

The address (n) specifies the addend.

C. Simpsons Integration: $\int_a^b f(x) dx$. The numerical computation would be carried out as: $\frac{1}{b-a} \int_a^b f(x) dx = \frac{1}{3n} [f_0 + 4f_1 + 2f_2 + 4f_3 + \dots + 4f_{n-1} + f_n]$. Here (a) and (c) are fixed; (b) varies. The order for carrying out this calculation would be:

PS_i (n) : (1) $S_2 \longrightarrow (Q)$
 (2) $[Q \cdot n + 2^{-39} A] + S_1$
 (3) $A \longrightarrow (S_i)$
 (4) $Q \longrightarrow (A)$

The address (n) specified the multiplicand.

It should be noted that:

(1) The general notation for the above orders would be $MV(n)$, $NV(n)$ and $PV(n)$, thus permitting full use of the variation character. When $V = S_1$ the multiplication is assumed to be carried out on the algebraic values of the operands, and the S_1 specified the particular S register to which the most significant part of $a \cdot b + c$ is transferred.

(2) If the addition is suppressed (denoted by $\bar{}$), the operation $a \cdot b + c$ becomes $a \cdot b$. In general then, $\bar{MV}(n)$ may include any of the ILLIAC multiplication orders. A particularly useful result of this innovation is the order $\bar{PV}(S_2)$ which, if $x = S_2$, forms the product x^2 , while $\bar{PS}_2(S_2)$ would replace x by x^2 in (S_2) .

(3) Although the function of these orders is similar to that of 2 - address and 3 - address orders, the single address structure of the ILLIAC order code is still maintained. Each order specified one address; however, the address of the supporting S register involved is implicitly specified by the order type. That is, M implies that the contents of a given S register, say (S_1) , will be added to the product; N implies that the multiplicand will be taken from a given S register, say (S_2) , etc. The innovation of introducing a third address, i.e., substituting S_1 for V, has been discussed before.

(4) A fourth case, viz., (a) and (c) are variable, (b) is fixed can be included in the case C by the following order pair (assuming $A = 0$ and $b = S_2$).

LS_1 (c)
PV (a)

A pseudo 3 - address order may also be considered for addition. Such an order might be

US_i (n) : (1) $S_1 \longrightarrow (A)$
 (2) $A + n$
 (3) $A \longrightarrow (S_i)$

where here, again, the address S_1 is implicitly specified by the order type U.

The following results were obtained after programming Library Routine S3, Logarithm, for PAC-1-2-3. A new order $\bar{PV}(n)$ was used in this routine.

	W*	OA	IA	TS
Illiac	14	$7 + 7 (39) + 2m$	$6 + 7 (39) + 3m$	3
PAC - 1	$13\frac{1}{2}$	$5 + 3 (39) + 2m$	$6 + 6 (39) + 3m$	2
PAC - 2	13	$1 + 2m$	$6 + 6 (39) + 3m$	1
PAC - 3	13	1	$6 + 6 (39) + 3m$	0

(1) m is defined by:

$$\log_2 x = \log_2 2^{-m} + \log_2 W; 1/2 \leq W < 1$$

(2) The quantity (39) denotes the number of passes through the loop determining $\log_2 W$.

It will be noted that the value of IA is almost constant although OA is reduced to its minimum. This is because the sequence of numerical operations of the corresponding Illiac program was followed. The orders of the PAC codes chosen, which followed the Illiac pattern, did not lend themselves to any combinations arising in the logarithm routine. This indicates a need to investigate in the direction of significant departure from Illiac methods.

* W = number of words

OA = accesses for operands

IA = accesses for instructions

TS = temporary storage

PART II

MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

A final description is being prepared of the program for solving systems of simultaneous linear algebraic equations using the magnetic drum. The program will solve about 140 equations by the elimination method.

Library routines N-5 and N-6 which read fractions and integers from tape and put them on the drum are being combined into one routine with the following characteristics:

- (1) Sum checks are provided.
- (2) A word count of the number of words recorded on the drum is obtained.
- (3) Integers and fractions may be arranged as desired on the tape.
- (4) First drum locations of sequences, if desired, may be determined from the tape.

PART III

MATHEMATICAL ANALYTICAL PROGRAM

(This work is supported in part by National Science Foundation Grant G-2794)

A study is being made of the Einstein field equations for the gravitational field due to a plane symmetric distribution of a perfect fluid undergoing adiabatic motion. It is hoped that the results previously obtained for isentropic motions may be generalized to this case. A co-moving coordinate system is used. In this coordinate system the metric tensor involves only three functions. However because the motion is not isentropic the stress energy tensor is not directly given in terms of these three dependent variables. Nevertheless by considering the pressure as a prescribed function of the coordinates one may obtain equations for the components of the metric tensor. These equations are being studied in special cases. It is planned to solve them numerically if analytic solutions cannot be obtained.

Two new techniques for the numerical integration of systems of ordinary first-order differential equations with given initial values have been investigated. Work has been begun on further investigation of the numerical solution of Sturm-Liouville problems. This will supplement the work done during the last two years.

PART IV
ILLIAC USE AND OPERATION -
GENERAL LABORATORY INFORMATION

Machine Use

During September specifications were presented for 7 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 868. Numbers followed by T are for theses.

868 Midwestern Universities Research Association. The Motion of a Particle in a High Energy Accelerator. This problem involves the solution of four coupled nonlinear differential equations by means of the Runge-Kutta method.

869 Psychology. Analysis of Q-Sort Descriptions of Abnormal Children. Factor analyses and other statistical studies will be made.

870 Electrical Engineering. Radiation Field Produced by a Slotted Wave Guide. The radiation field excited by an incident wave on a slotted wave guide is solved using a number of parameters.

871 T Speech Department. Relationships between Vocal Responses to Delayed Auditory Feedback and Certain Personality Measures. Disturbances in speech are produced by playing back the speech after it has been delayed slightly. The amount of disturbance produced in this way is correlated with various speech measures and personality measures.

872 University of Michigan. Selection of Medical Students. Various data collected on medical students at the University of Michigan are to be analyzed statistically.

873 Physics. Relativistic Two-Body Dynamics Problem. This program is designed to calculate energies and angles resulting from bombarding a particle of mass m_2 with a projectile particle of mass m_1 . The formulas computed by the program carry out the transformations into a center of mass coordinate system.

874 Structural Research. Analysis of Flat Slabs and 2-Way Slabs. The problem is a series of analyses of flat slabs and 2-way slabs under various loading combinations. The problems to be solved by the Illiac are algebraic, linear simultaneous equations which are obtained by the method of finite differences.

Table I shows distribution of machine time for the month of September.

TABLE I

Regular Maintenance	27:57
Unscheduled Maintenance	18:15
Drum Engineering	35:33
R.A.R.	4:19
Leapfrog	48:39
Wasted	:01
<u>Use by Departments</u>	
Computer Group	5:00
Physics	20:53
Control Systems Lab.	7:38
Structural Research	2:04
Struct. Res. (DA-11-02-ORD1980)	:16
Struct. Res. (AF 24994)	:29
Psychology	11:55
Psychology (MD 620)	6:04
Electrical Engineering	3:27
Elec. Eng. (AF 3220)	1:21
Chemistry	49:01
Agriculture	6:30
MURA	165:24
Ill. Dept. of Public Welfare (Coan)	10:44
Ill. Dept. of Public Welfare (Hurley)	5:25
University of Michigan	1:42
Demonstrations	1:25
Miscellaneous	29:45
Total	463:47

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for September.

TABLE III

Reader Errors	11
Punch Errors	0
Control Errors	2
Memory Errors	1
Drum Errors	4
Scope Errors	1
2L type Error (leapfrog)	4
Unknown	5
Total	<u>28</u>

TABLE II

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
9/4/56	20:00	:00	0		00	1:10	0
9/5/56	19:52	:08	1	(1) Coupling on Reader "B" broken	00	1:22	0
9/6/56	19:59	:01	1	(1) Tape tore in reader "B"	00	1:32	0
9/7/56	20:00	:00	0		00	1:29	0
9/10/56	13:14	6:46	2	(1) Memory position 2 ⁻¹² error (2) Open filament in V-18 reg. selection chassis	00	1:08	0
9/11/56	20:00	:00	0		00	:56	0
9/12/56	19:50	:10	1	(1) Drum error. Drum routines would not read back to Illiac without error.	00	1:22	0
9/13/56	19:59	:01	1	(1) Film jammed in cassette	00	1:05	0
9/14/56	20:00	:00	0		00	1:02	0
9/17/56	18:44	1:16	2	(1) Cross talk on drum (2) Light out on reader "B"	00	:58	0
9/18/56	19:58	:02	2	(1) Unknown (2) Unknown	00	1:11	0
9/19/56	13:33	6:27	3	(1) Unknown (2) Unknown (3) 2L type failure, Leapfrog	00	:55	1
9/20/56	17:45	2:15	6	(1) 2L type failure, Leapfrog (2) 2L type failure, Leapfrog (3) Dirt on sprocket hole of reader "K" (4) Reader "K" error (5) 2L type failure, Leapfrog (6) Unknown	00	3:09	3
9/21/56	19:59	:01	1	(1) Reader "K" error	00	2:31	0
9/24/56	19:18	:42	5	(1) Reader "K" error (2) Reader "K" error (3) Reader "K" error	00	1:44	0

TABLE II

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
9/25/56	20:00	:00	0	(4) Control (5) Reader "K" error	00	1:01	0
9/26/56	19:58	:02	2	(1) Reader "B" error, voltage setting too low	00	1:01	0
				(2) Drum Failure	00	1:36	0
9/27/56	19:59	:01	1	(1) Drum error	00	2:41	0
9/28/56	20:00	:00	0		00	3:15	0
TOTALS	362:08	17:52	28		00	28:27	4

Comments on the Illiac and Related Equipment

A new photoelectric tape reader control logic was reviewed in anticipation of its installation in the machine. This logic allows the tape brake to be applied immediately after the character is read. The tape is permitted to stop either on the sprocket hole of the character read last or on the sprocket hole of the next character to be read or anywhere inbetween. In the present tape reader control the last sprocket hole had to be passed by before braking could occur. The extra stopping time effectively allowed the reader is that corresponding to the time from the beginning to the end of a sprocket hole.

The regular maintenance of the drum memory is now arranged so that tubes are checked about every three months as compared to every six months as previously planned. During the month in the regular running of drum test codes a total of 23 errors occurred during 33 hours of test codes. A new test code due to Mr. Carter has been more helpful than previous ones in locating intermittent playback errors. The 6AU6 preamplifier tube has been replaced in about one-half of the units by a type 6136.

The new photoelectric tape comparer was completed by the shop and put into regular use in the Teletype Room. A similar high-speed reperforator unit for the Teletype Room is being built in the shop.

Reports and Seminars

Reports

Laboratory Report No. 72, "Designing Computer Circuits with a Computer," by Gene H. Lechner, September 17, 1956.

Seminars

"An Introduction to Error Detecting and Correction Codes, by G. A. Metze, September 25, 1956.

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