Adding Memory to the PDP-9*

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Although it was designed more than six years ago, the PDP-9 is still not an obsolete machine. Software is currently maintained by the Digital Equipment Corporation (DEC), because of the PDP-9's program compatibility with the currently-marketed PDP-15. The latter machine uses TTL integrated circuits but is only marginally faster (cycle time of 0.8 μ sec compared to 1.0 μ sec) than the discrete DTL logic of the PDP-9. The PDP-9 actually executes one instruction (Increment and Skip if Zero) faster than the PDP-15 by using fewer machine cycles.

The major problem for PDP-9 owners interested in upgrading the capabilities of their machine is that its obsolete discrete DTL logic and below ground logic levels (0 to -3V) make the addition of memory prohibitively expensive. The price for an additional 8K of PDP-9 core memory purchased from DEC has varied over the years but is currently in the neighborhood of \$10,000 or more than \$0.06 per bit. Used memories are cheaper, but because the PDP-9 is not obsolete, they are difficult to find.

For these reasons, the University of Minnesota School of Physics decided to interface a TTL memory system to its PDP-9 used for data acquisition in high energy physics. The memory selected was a Model 684 core memory system manufactured by

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Fabri-Tek, Inc., Minneapolis, Minnesota. The cost of the memory card set purchased from Fabri-Tek was less than \$0.01 per bit.

PDP-9 Memory System

The basic PDP-9 is supplied with an 8,192 word by 18 bit MC70B core memory, which requires one μ second for a read-modify-write cycle. The modify time is about 200 nsec, giving the MC70B a "full cycle time" of less than 800 nsec, reasonably fast even by recent core memory standards. The high speed of the original memory severely restricts the maximum cycle time of an added memory system.

The interface between the MC70B core memory and the PDP-9 central processor (CP) is shown in Table I and Figure I. A minimum number of timing and control signals are interchanged between the memory and the CP. The CP provides a clock pulse for overall system synchronization and a Start Memory level to indicate the need for a memory reference during the forthcoming cycle. The memory produces a Memory Strobe signal isochronous with the Sense Amplifier Data Outputs and a Memory Done level just prior to the end of the cycle. Both Address and Data Inputs are transferred to the memory through the Memory Buffer (MB) register. The MB holds the address during the first half of the cycle and the input data during the latter part of the cycle.

The standard method of adding memory to the PDP-9 requires the attachment of a KG09B Memory Extension Control and an additional MC70B unit (renamed MM09A,B,C) for each increment of 8K words added up to the 32K words capacity of the machine.

The Memory Extension Control logic augments the program counter with two additional bits and establishes a two bit address register to hold the location of the current memory bank. It determines which bank is to be addressed, ensuring that indirect addresses, monitor calls, auto-index references, interrupts and data channel transfers reference the correct memory bank. The KG09B is located in the ME09B chassis above the console in the main bay of the PDP-9. The chassis also holds the Memory Parity and Memory Protect logic. The chassis is installed and its backplane is wired by DEC for all three options when any one is ordered.

Fabri-Tek 684 Memory System

The Fabri-Tek 684 Memory System is a 3-D, 3-wire core memory designed for a "full cycle time" of 650 nsec. The access time, measured from a stable address input to a stable data output, is guaranteed less than 320 nsec. This memory is just fast enough for easy interfacing to the PDP-9 since some time is required for the input and output level shifting. It was selected over a number of competing systems, both semiconductor and core, for reasons of speed, price, non-volatility and convenient access to the manufacturer.

The 684's interface requirements, shown in Figure II and Table II, are substantially similar to those of competing memory systems. Not all the signals are needed for a simple PDP-9 interface; the additional signals could be used to implement direct memory access at TTL levels either synchronously or asynchronously with the PDP-9. The 684 memory is started

with a Cycle Initiate signal and the write portion of the cycle is restarted after the modify time by a Cycle Continue signal. The Address Inputs and the Data Inputs are supplied to the memory on separate lines which can be wired together to reduce the cabling between the 684 and the Extended Memory Interface. A Master Reset clears the 684's logic and a Data Save signal insures the non-volatility of stored data during a power off condition. The basic outputs from the 684 are the Data Out signals and a Data Available signal which indicates when the output data is valid.

University of Minnesota Extended Memory Interface

The University of Minnesota Extended Memory Interface (EMI) is designed to make the Fabri-Tek 684 memory look to the PDP-9 like one or more MC70B units. The EMI requires the use of a KG09B Memory Extension Control or its equivalent to handle switching between memory banks. The EMI is compatible with the original MC70B installed in the PDP-9, but it can also be used to provide the entire memory requirements of the system.

The EMI consists of five wire-wrapped circuit boards plugged into a card file located just above the ME09B assembly. A continuous backplane and ground mesh is hardwired between the ME09B and the EMI. All signals between the PDP-9 and the EMI are transferred through this backplane except for the Sense Amplifier Outputs which are directly cabled to the CP.

The EMI uses integrated circuitry as much as possible to provide ease of assembly, compactness and reliability. The input circuitry which converts all signals from negative logic to TTL levels uses a fast, dual channel, integrated sense

amplifier (SN75107) with a typical delay time of 17 nsec. The inputs to the 684 memory are driven by a high-current-sinking, TTL open-collector gate (7438), which can drive four lines from each integrated package. The Sense Amplifier Outputs to the PDP-9 are strobed when the output data from the 684 memory is valid using Schottky TTL gates (74S00). The output level converters, which change the signals from TTL to negative logic levels, are dual-channel, standard hybrid circuits (DH0034). The timing circuitry of the EMI is implemented with standard TTL logic. Basic delays are established using delay lines to provide stability, but all delays can be trimmed by adjusting the RC constants of eight integrated monostable multivibrators (74121). The +5 volt power for the EMI is derived from the PDP-9's +10, -15 volt power supplies using integrated point-of-load regulators (LM309 for the positive and LM320 for the negative supplies). Schematics and descriptions of the EMI circuitry and installation details are available from the author.

Conclusion

The University of Minnesota has expanded its PDP-9 memory to the full 32K words capacity of the machine. The expansion from 8K to 16K words, entailing the construction of the EMI, was the most difficult part of the project. This phase also produced the most dramatic increase in machine flexibility. With 16K words of memory, the PDP-9 can use the improved FORTRAN compilers F4S and F4X and fully exploit the I/O device independence of the Advanced Software System. The expansion from 16K to 32K was both relatively inexpensive and

technically simple. This latter addition further expands the complexity of problems which can be handled by the PDP-9.

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Table I
PDP-9 CP to Memory Interface

<u>Signal</u>	<u>Purpose</u>	<u>Origin</u>	<u>Type</u>	<u>Assertion Level</u>
Clock	System synchronization	CP	Pulse	-3V
Start Memory	Indicates need for memory reference cycle	CP	Level	-3V
Power Clear	System reset	CP	Pulse	-3V
Memory Buffer 0-17	Address and data	CP	Level	GND
Memory Strobe	Data output present	MEM	Pulse	-3V
Memory Done	Memory not busy	MEM	Level	-3V
Sense Amplifier Outputs 0-17	Data output	MEM	Pulse	-3V
Power OK*	Voltages and temperatures in memory within operating limits	MEM	Level	-3V
AM Sync*	Halts CP for direct memory access	MEM	Level	GND

* Not used in basic Extended Memory Interface

Table II

EMI to Fabri-Tek 684 Interface

<u>Signal</u>	<u>Purpose</u>	<u>Origin</u>	<u>Type</u>	<u>Assertion Level</u>
Cycle Initiate	Start memory cycle	EMI	Pulse	GND
Cycle Continue	Restart write portion of cycle	EMI	Pulse	GND
Address Inputs 0-14	Address to memory	EMI	Level	+3V
Data Inputs 0-17	Data to memory	EMI	Level	+3V
Master Reset	Clear memory logic	EMI	Pulse	GND
Data Save	Shutdown memory during power off to retain data	EMI	Level	GND
Data Outputs 0-17	Data from memory	MEM	Level	+3V
Data Available	Valid data output	MEM	Level	GND
Full/Split*	Determines type of memory cycle	EMI	Level	GND for split
Read/Write*	Determines type of cycle	EMI	Level	GND for write
Late Data Strobe**	Alters data entry time	EMI	Level	+3V for normal time
Memory Busy**	Indicates memory active	MEM	Level	GND

* Permanently wired to GND for simple PDP-9 application

** Not connected for simple PDP-9 application

FIGURE CAPTIONS

Figure I--Timing diagram for the signals interchanged between the PDP-9 central processor and the MC70B memory.

Figure II--Timing diagram for the signals interchanged between the Extended Memory Interface and the Fabri-Tek 684 memory.

Figure III--Simplified schematic of the level conversion circuitry.

- Notes:
1. Address assumed to be 0 and data assumed to be 1.
 2. AM Sync must be at ground during this time to halt CP during next cycle.

Note: Address and data out assumed to be zero; data in assumed to be 1.