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**A MODIFIED INSTRUCTION SET
FOR THE
FFTF INSTRUMENTATION PROTOTYPE**

W. D. DRAPER

AUGUST, 1967

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A MODIFIED INSTRUCTION SET
FOR THE
FFTF INSTRUMENTATION PROTOTYPE

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W. D. Draper

INTRODUCTION

The Fast Flux Test Facility (FFTF) Instrumentation Prototype general purpose digital computer is being used for hybrid computer studies, direct digital control studies, and process control software development. The instruction set of the digital computer did not include an increment-to-the-accumulator instruction, a one's complement subtract instruction, or a three-way branch instruction. The need for these instructions was apparent in the application for which the Instrumentation Prototype was being used. The central processor of the digital computer was modified to include these instructions for the purpose of providing greater programming flexibility, and to perform the given functions with fewer instructions, in less time.

SUMMARY

The FFTF Instrumentation Prototype programming flexibility has been increased by making some inexpensive hardware changes in its instruction set. Changes include the addition of CAS (Compare and three-way Skip), SUB (one's complement subtract), and IAC (Increment the Accumulator) instructions.

BACKGROUND

The FFTF Instrumentation Prototype is a general purpose, solid state, digital-data processor and controller similar to the Digital Equipment Corporation PDP-7. It includes KSR-35 teletype, high speed paper tape reader and punch, Type 550 DEC tape, 8K core memory, the hardware arithmetic option, and 16 levels of priority interrupts. The basic instruction set includes both memory reference and augmented instructions. Memory reference instructions store or retrieve data from core memory; augmented instructions do not.

Memory reference instructions include arithmetic, logic, data handling, and program control operations. A memory address (Bits 5-17) is specified as part of a memory reference instruction. The contents of the addressed memory location are used by the processor in executing the instruction. The indirect Bit (Bit 4) indicates an indirect address. The remainder of the word (Bits 0-3) is the instruction code. Most memory reference instructions require two computer cycles (3.5 μ sec). The first cycle fetches the instruction itself. The second cycle fetches the data addressed and executes the instruction. All memory reference instructions can be executed indirectly.

Augmented instructions include both Operate and IOT (Input/Output/Transfer). The Operate Class Instructions are micro-coded and are used to perform operations on the Accumulator, Link, and Program Counter (shift, clear, complement, skip, etc.). Bits 5-17 specify what operation the processor is to perform. Each bit represents a unique operation. A number of different operations can be performed by selecting several bits in the same instruction. IOT instructions enable the processor to communicate with external devices, send control information and transfer data. Some I/O devices require extra time for certain operations. The select-codes for these devices generate slow-cycle-request signals, which insert 500 nanosecond delays between Timing Pulses 6 and 7, and between Timing Pulses 7 and 1 of the timing pulse generator. A slow-cycle-request increases the cycle time from 1.75 μ sec to 2.36 μ sec.

MODIFIED INSTRUCTION SET

The Instrumentation Prototype's standard instruction set uses all of the sixteen available memory reference codes. Therefore, any new instruction must replace one in the standard set. This presented a problem because all of the programs currently available use the standard instruction set. To maintain their usefulness without extensive rewriting, the new instructions may be selected by means of setting a flip-flop. This flip-flop, (MOD-1C25) shown in Figure 1, may be set or cleared under program control, or by a momentary spring loaded toggle switch on the console. The switch, labeled MOD-NORM, permits the selection

FIGURE 1. Modified Instruction Set for IP-7,
Compare and Skip Modification (CAS)

of either the standard or normal (NORM) instruction set, or the modified (MOD) instruction set. The instructions used to set or clear the MOD flip-flop are Modified Instruction Clear (MICL), and Modified Instruction Set (MIST).

IAC is a new Operate Instruction with a code not previously used. It is not affected by the MOD-NORM switch, so it is available with both instruction sets.

COMPARE AND SKIP (CAS)

The Compare and Skip (CAS) instruction code is 540000. It replaces the Skip-if-Accumulator-Different (SAD) instruction when the modified instruction set is chosen. CAS is a two-cycle instruction and initiates a slow-cycle-request during its Execute cycle. CAS requires 4.11 μ sec for execution. If an indirect address is used, execution time is increased to 5.86 μ sec.

The SAD Instruction (standard) permits the programmer to compare the Accumulator (AC) with a memory location (Y); it increments the Program Counter (PC) if they are different, causing the next instruction to be skipped. If the programmer wishes to know whether the number contained in Y is larger or smaller than that contained in the AC, he must save the contents of the AC in a temporary storage location, complement the AC, add Y, check for a positive or negative Accumulator, skip accordingly, and restore the contents of the AC.

The CAS instruction combines all the operations described above. If the instruction CAS Y is executed, the results would be as follows:

- If Y is less than the AC, the PC will not increment.
- If Y is equal to the AC, the PC will increment by one.
- If Y is greater than the AC, the PC will increment by two.

Example

Compare the AC to location Y and branch on $Y < AC$, $Y = AC$, and $Y > AC$.

Standard Instruction Set

Operation	Time (μ sec)		
:			
DAC TEMP	3.5	}	14
CMA! CLL	1.75		
ADD Y	3.5		
LAC TEMP	3.5		
SZL	1.75		
JMP (Y > AC)	.	}	17.5
SAD Y	3.5		
JMP (Y = AC)	.		
JMP (Y < AC)	.		

Note: Original content of the link is lost.
Time required is 14 μ sec if Y > AC,
or 17.5 μ sec if Y < AC.

Modified Instruction Set

Operations	Time (μ sec)
:	
CAS Y	4.11
JMP (Y < AC)	.
JMP (Y = AC)	.
JMP (Y > AC)	.

Note: Original content of the link is not disturbed.
Time required is 4.11 μ sec.

In Table I, timing pulses T-1 through T-7 are generated by the central processor. For a description of terms used, the reader should refer to the PDP-7 Users Handbook (Digital Equipment Corporation, F-75) and Figure 1 of this report.

SUBTRACT (SUB)

The Subtract (SUB) instruction code is 340000. It replaces the Two's complement Add (TAD) instruction when the modified instruction set is chosen. SUB is a two-cycle instruction requiring 3.5 μ sec for execution.

To subtract a number from the accumulator on a standard PDP-7, it is necessary to complement the accumulator (CMA), add memory location

"Y" (ADD Y), and complement the accumulator (CMA) again. This requires three locations and four cycles (7 μ sec).

The SUB instruction makes it possible to perform all of these operations in one location and two cycles (3.5 μ sec).

TABLE I

FETCH CYCLE:

T6 Complement the Accumulator
 CLEAR MAC
 CLEAR PAC
 CLEAR OV

EXECUTE CYCLE:

T3 SET MAC if MB $\emptyset$ (1) and AC $\emptyset$ (1)
 SET PAC and OV if MB $\emptyset$ ($\emptyset$) and AC $\emptyset$ ($\emptyset$)
 AC XOR MB $\Rightarrow$ AC

T4 AC CARRY
 +1 to PC and END CARRY if AC $\emptyset$ CARRY and MAC not set

T5 END CARRY if MAC is set

T6 +1 to PC if AC $\neq \emptyset$ and PAC set
 SET OV if PAC is set
 Complement the Accumulator

T7 +1 to PC if AC $\neq \emptyset$ and OV set
 +1 to PC if AC = $\emptyset$
 AC XOR MB $\Rightarrow$ AC

FOLLOWING FETCH CYCLE:

T1 AC CARRY
 T2 END CARRY if MAC is set

Example

Subtract location Y from the contents of the AC

Standard Instruction Set

Operation	Time (μ sec)
.	
.	
CMA	1.75
ADD Y	3.5
CMA	1.75

Note: Time required is 7.0 μ sec.

Modified Instruction Set

Operation	Time (μ sec)
.	
.	
SUB Y	3.5

Note: Time required is 3.5 μ sec.

SUB complements the Accumulator at T1 of the execute cycle, performs a one's complement Add (ADD), and completes the operation by again complementing the AC at T7 of the Execute Cycle. (See Figure 2.)

INCREMENT ACCUMULATOR (IAC)

The Increment Accumulator (IAC) instruction code is 742000. The accumulator is incremented at event-time-three, and the instruction requires one cycle (1.75 μ sec) for execution.

The standard PDP-7 processor does not have an equivalent to the increment accumulator instruction. To add one to the accumulator you must "ADD Y" or "TAD Y" where the content of location "Y" is one. ADD "Y" or TAD "Y" requires a location for the instruction and a location for "Y", and requires two cycles (3.5 μ sec). The IAC instruction adds one to the accumulator in one cycle (1.75 μ sec). IAC can be microprogrammed with CLA to set the accumulator to one (the equivalent of LAC "Y" where "Y" contains one).

IAC may be microprogrammed (combined) with any operate-instruction not occurring at event-time-three. The only exception is that it may be microprogrammed with CML (complement the link at event-time-three).

FIGURE 2. Modified Instruction Set for IP-7,
Subtract Modification (SUB)

The "Rotate Accumulator Left" and "Rotate Accumulator Right" instructions are selected by operate-codes having Bits 13 or 14 set respectively. When either is selected, the rotate will occur twice if Bit 7 is set. Before the addition of the IAC instruction, setting Bit 7 without either Bit 13 or 14 did nothing. It now causes the Accumulator to be incremented (increased by one). No switching is required. A previously unused gate has been wired to generate an end carry pulse at event-time-three if conditioned by an operate code having Bit 7 set and Bits 13 and 14 not set. The IAC gate (1-J-10) is wired as follows:

Input "D" is the "OP2" pulse from 1-J-7-D
 Input "E" is MBB7 (1) from 1-J-5-E
 Input "H" is MBB13 (0) from 1-F-16-H
 Input "F" is MBB14 (0) from 1-F-15-H
 Output "L" (IAC goes to the "End Carry" pulse amplifier 1-H-3-F.)

The IAC Instruction is now a permanent part of the Instrumentation. Prototype Instruction set and may be used accordingly.

FIGURE 3. Increment Accumulator

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