UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are
not, in general, reported herein.

- Part I: Study Program on High Speed Computer
- Part II: Mathematical Research and Programming
- Part III: Mathematical Analytical Program
- Part IV: Illiac Use and Operation -
General Laboratory Information

June, 1956

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PART I
STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415. This contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contract N6ori-07130 and Contract N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computing Centre and Department of Physics.

During the past year the Laboratory has been working on research on circuits and logical design for a very high-speed computing machine. Effective June 1, a contract sponsored jointly by the Atomic Energy Commission and the Office of Naval Research will make it possible to devote more of the Laboratory's effort to this program. The program generally intends to study both theoretically and experimentally a high-speed computer using direct-coupled asynchronous circuits with binary operation times from one state to another of about 25 μ ps. In order to summarize the scope of the work which the Laboratory has in mind, the following three sections have been extracted from the proposal to the Atomic Energy Commission covering this work.

Circuits

During the summer and fall of 1955 the Laboratory has investigated circuits using both vacuum tubes and transistors with operation times of less than 50 millimicroseconds. An operation time here is taken to mean the total time to change from one binary state to another, starting from the beginning of a signal and ending with sufficient output signal to actuate the next operation. An operation time is the time which is additive for elementary circuits when a serial sequence of operations is considered. It includes all delays due to any cause. An operation time is to be distinguished from a rise time which would ordinarily be shorter. Several circuits are probably satisfactory in this speed range using either vacuum tubes or transistors. Recently the α -cutoff frequency of junction transistors has increased to a high enough value to make them appear more promising. Figure 1 shows a flipflop and gate circuit which has been tested with an operation time of about 21 μ ps using surface-barrier transistors. This circuit has not been completely analyzed for tolerances and neither has a

complete set of appropriate, and, or and not circuits. Calculations on individual circuits and experiments on them indicate that circuits of this speed can probably be achieved. As a part of this proposal a set of circuits with operation times of 25 μ s or less would be worked on with the intention of using them in a general purpose machine. This circuit work has been carried out with the support of the Office of Naval Research.

The operation time for circuits of the type used in Institute for Advanced Study type machines such as the Illiac, is about 1.0 microsecond. Thus the elementary circuits proposed here are 40 times faster than the elementary circuits used in the Illiac.

Figure 1

Crosscoupled Flipflop using Surface Barrier Transistors
Operation Time: About 20 millimicroseconds to 50% point.

A linear dimension of a final machine could be imagined to be as much as 3 meters. Since the velocity of light is 3×10^{10} cm./sec. the resulting transit time under the most favorable circumstances would be 10^{-8} second. Thus the proposed circuits would have operation times only 2-1/2 times as long as 10^{-8} second and it is clear that some attention will need to be applied to keeping the machine small. Since the circuits are expected to be asynchronous, at least in part, the dimensions of the machine, if large, will tend to slow up those operations which require the information to go over the whole dimension of the machine. Register operations may be included in this group but the effect on speed should not be large. Of course, every effort will be made to keep the physical machine as small as possible.

Form of Circuits

The logical interconnections of a computer can be classified as being ac coupled or dc coupled and synchronous or asynchronous. Most machines have been largely ac coupled and synchronous in nature. The most important exception to this is the I.A.S. group of machines which are at least partly dc coupled and in part asynchronous. The Digital Computer Laboratory at the University of Illinois has concentrated on asynchronous work in all of its efforts. Work on the algebra for this type of logic has been carried out. The experience of the Laboratory in using this type of logic has indicated that it contributes to reliability although reliability is a hard thing to measure and other factors besides the direct-coupled asynchronous features contribute to it. Asynchronous circuits, although harder to design, may be readily serviced. The asynchronous type of circuit and logic obviate the problems arising due to the information transit time discussed in the previous section. The asynchronous logical work has been supported in part by the Office of Naval Research.

Machine Organization

The design of a machine with a particularly fast arithmetic unit and with presently available memory systems poses serious organizational problems to prevent making the arithmetic unit wait for the memory. This will make necessary a study of the organization of the machine to make the most use of the speed of the arithmetic unit. The use of one or more additional registers would make it

possible to do more operations without referral to the high-speed memory. An important new instruction would be one that can combine an addition and a multiplication in one operation.

Balance of Memory and Arithmetic Unit

A study was made of the cost in time that would be paid in solving a problem of the type described below if a very high-speed computer was assumed to have a modest sized low access time memory and a large high-access time back-up memory in contrast to a large capacity low-access time memory. The type of problem considered was assumed to have the following characteristics: N words could be used to calculate $N - k$ words which replaced an equal number of the original words and were used as the original words. The study was based on some remarks made by H. H. Goldstine in a private communication.

By assuming characteristics for the different access times that seemed in accordance with current engineering practices it was shown that the percentage increase in the time referred to above behaved essentially as

$$R = c \left(\beta_1 + \frac{\alpha_1/k + \beta_1/2}{N/k-1} \right)$$

It was then shown that in certain cases only a fifteen percent loss in computing time was the price paid from by an eight-fold decrease in the size of memory.

Transistor Test Computer

In June the transistor test computer was finally completed and it was possible to test some of its performance characteristics. As explained previously (see May, 1955, December, 1955, January-May, 1956 reports) this machine provides the proving ground for a set of dc-coupled transistorized logical elements having rise times of about 1 μ s. The input-output impedance ratio of these units is sufficiently high ($\sim 10:1$) to permit their use in all points without having to specify the load conditions. A complete report on this test unit is being prepared but a summary of some of its characteristics follows.

Machine Type: Parallel, asynchronous, dc-coupled
 Registers: $\overline{AA} \overline{QQ} R^3 R_3$

Register Capacity:	4 binary digits
Memory:	Non-destructive core memory. 4 words, each one having 2 bits for the instruction and 4 for the number to be operated on.
Instruction Types:	Add, subtract, multiply, divide
Addition Time:	140 μ s (including memory access)
Subtraction Time:	140 μ s (including memory access)
Multiplication Time:	620 μ s (including access and A $\rightarrow$ Q shift)
Division Time:	620 μ s (including access and Q $\rightarrow$ A shift)
Number of Transistors:	752
Number of Diodes:	498
Power Consumption:	75W
"One"-level:	+2V (nominal)
"Zero"-level:	-2V (nominal)
Gating Voltage:	+4V (nominal)
Tolerances:	5% on supply voltages and resistors. $\alpha > .92$, $f_{\alpha} \geq 1$ MC.
Characteristic Rise-Times:	1 μ s
Types of Plug-in Units:	Single-ended flipflop (F) and last moving point single-ended (F') Bridge modulator gate (G), combination with driver (G') power gate driver (P) Not-circuit (N), and level restorer (L) 2 and 3 input <u>and</u> (A and A'), and or (O and O') Memory pulser (M), read-out amplifier (R), delay-circuit (Δ) Isolation diodes (D) and clear driver (C)

Experimental Tests on Speed-Independent Logic

Experimental work has been carried out on the design of several circuits including "A" chassis of the kind used in Illiac and binary counters which are believed to be strictly speed-independent as recently devised here. A program for Illiac has been used to analyze the speed-independence of circuits and several practical designs have been considered.

PART II
MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office
of Naval Research under Contract N6ori-07130.)

Continued Fraction Expansions

Study was made of a continued fraction routine for computing a large number of different functions. It uses a straightforward technique and makes use of the previously mentioned rational fraction routine for calculating exact coefficients. It is hoped that the study will lead to additional library programs which will have advantages in speed and memory requirements over the usual power series approximations to functions.

Magnetic Drum Use

Further work was done on the automatic use of the drum bootstrap with existing programs and in making some modifications of the input routines on the drum. The space requirement was shortened by about six words at the expense of introducing some additional complication into the calculation of key words. Since this calculation is done only once and is already complicated, the added complexity makes little difference.

Logical Design

The effects of a number of parameters of logical design (e.g., register arrangement, operation speeds, access time, complexity of instructions) are being studied by writing programs in various instruction codes.

Program Library

The following five programs were added to the library in June. Program V-7 was prepared by Professor W. C. Jacob of the Department of Agronomy.

V-7 (206) Provide Sets of Random Numbers From 1 to N. This is a program of the auxiliary library which uses V-3 to provide pseudo-random numbers and selects sets from them.

P-16 (214) Infraprint. 56 Words. This is an integer or fraction print routine which will print exactly rounded fractions or exact integers to n decimal places where $1 \leq n \leq 12$. It may be entered in any of 8 ways with a standard entry to provide a variety of kinds of output.

- N-11 (215) Input a Sequence of Fractions or Integers. 25 Words. This program will read n place signed decimal numbers with $0 \leq n \leq 12$ from the tape. Fractions are correctly rounded on conversion with an error not exceeding 2^{-40} and integers are converted exactly.
- Q-3 (217) Complete Circuit Analyzer. Complete Program. This is a program of the auxiliary library. It is designed to aid in the study of speed-independent circuits and analyzes complete circuits for speed-independence when given a description of the nodal equations and the initial state. The routine is limited to circuits with 39 nodes and having no more than $(703 - 4n - k)/6$ states per cycle; n is the number of nodes and k is the number of integers and plus signs required to describe the circuit. Only in extreme cases is more than 10 minutes required by the program.
- X-1 (218) Decimal Order Input. 25 Words. This is a modification of the Illiac standard input routine. It is stored on the magnetic drum and need not be included on any program tape. It is faster than the old version (serial number 18) and provides room for one more parameter by reducing the number of temporary storage locations to two. Entries to it are as before except for one little-used one and it occupies the same memory positions as the old version.

PART III
ANALYTICAL PROGRAM

(This work is supported in part by National
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Work is progressing on a code to integrate the Einstein field equations for a static, spherically-symmetric space-time in which there exists a perfect fluid whose caloric equation of state is arbitrary. The determination of these equations of state by the use of various distribution functions, which give the number of particles in a given volume of phase space, is under study. The purpose of this study is to rewrite the caloric equation of state so that the density is a function of pressure and another variable entering into the Einstein field equations.

A study has been initiated on the integration of the Einstein field equations for the gravitational fields due to a plane-symmetric distribution of a perfect fluid in adiabatic but non-isentropic motion.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During June specifications were presented for 19 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 908. Numbers followed by T are for theses.

809 T Chemistry. Electrostatic Deposition on Cylinders. Use of the Runge-Kutta method will be made to calculate trajectories for certain ranges of the variables and then an inverse interpolation will be used to select another boundary value. Results are given as collection efficiency.

810 T Education. Ethnocentrism and Rigidity Analysis. Standard programs in the Illiac and Psychology Program Libraries will be used to determine the relationships among ethnocentrism, rigidity, anxiety and social acceptability. Data have been collected on 160 students.

811 Electrical Engineering. Aperture Distribution. A number of integrals will be evaluated to calculate the field due to a uniform plane wave in a long narrow slot in an infinite conducting plane.

812 T Psychology. A Psychophysical Investigation of Triangular Form. Standard library routines will be used to estimate the projections of each of a set of triangles on k "psychological dimensions" in a euclidean space. The values on each dimension will be predicted from a set of physical measures of the triangles using a linear regression equation.

813 Bureau of Economic and Business Research. Illinois Employers Labor Force Anticipation. Library Routine K-12 will be used to obtain the necessary correlation coefficients to explain the factors influencing the labor force anticipations of Illinois employers.

814 T Electrical Engineering. Calculation of Surface Brightness. An equivalent electrical network is used to represent the light flux and its corresponding interreflections within an enclosure. Surface brightnesses are obtained by solving this network, the solution being obtained from sets of simultaneous linear equations.

815 Psychology. D-Statistic. This is a profile analysis with 20 items per profile and 8 profiles per subject.

816 Physics. AG-Cyclotron. This is a study of radial oscillation in a spiral ridge cyclotron. Runge-Kutta integrations will be carried along orbits with several different sets of boundary conditions.

817 Electrical Engineering. Depth of Penetration. The problem is an antenna study in which the depth of penetration is calculated as a function of 3 parameters.

818 Illinois Department of Public Welfare. Child Personality Structure. Data for this problem were gathered from a large number of 6-8 year old school children. They will be analyzed with centroid factor analyses and rotation procedures with the results being plotted with the cathode ray tube output.

819 Computer. Verify Transistor Flipflop. The program evaluates the maximum range of output levels for given tolerances, supply voltages, and resistor values. The computation consists of the evaluation of a set of 5 algebraic formulas.

820 State Water Survey. Precipitable Water Inflow for the State of Illinois. Data from 4 weather stations are used to compute and check precipitable water inflow, with 3 stations yielding data to compute inflow, and the last being used to check obtained data.

821 Chemistry. Charge Distribution in Molecules. The problem consists of calculating multipoles of the charge distribution of molecules using molecular orbital wave functions which are linear combinations of Slater atomic orbitals. The calculation is done in two stages; the first involving moment integrals and the second involving solution of matrix equations.

822 T Electrical Engineering. Location of the Roots of the Minimum Function. The problem is concerned with the locations of poles and zeros of the minimum function.

823 T Institute of Communications Research. A Comparison of Semantic Judgements for Two Cultural Groups. Osgood's Semantic Differential will be used to investigate the semantic judgements of Japanese and American cultural groups. The problem is essentially a series of factor analyses, between the two groups and between sexes within each group.

824 T Agricultural Economics. Farm Planning in Southern Illinois. Linear Programming Routine M-15 will be used to develop farm plans for typical farms in southern Illinois. Emphasis will be placed on various dairy alternatives.

825 Physics. Meson Phase Shift Determination. A set of five simultaneous non-linear equations are to be solved by determining the minimum of a function of the five-phase shifts. The minimization will be carried out with Library Routine H-5.

826 Electrical Engineering. Polynomial Coefficients. This program is used to calculate the coefficients of the polynomial obtained from the continued fraction expansion of a ladder network.

827 T Agricultural Economics. Soil Bank Study. Library Routine M-15 will be used to determine benefits from compliance with government soil-bank programs on typical farms in northern Illinois.

Table I shows distribution of machine time for the month of June.

TABLE I

Regular Maintenance and Engineering	42:14
Unscheduled Maintenance	17:15
Drum Engineering	32:03
R:A.R.	6:58
Leapfrog	43:20
Wasted	:16

TABLE I (Cont.)

<u>Use by Departments</u>	
Computer Group	10:27
Physics	38:31
Control Systems Lab.	67:13
Structural Research	4:23
Struct. Res. (AF 24994)	5:45
T.A.M. (Task 53)	2:31
Psychology	22:23
Psychology (MD 569)	1:39
Electrical Engineering	12:58
Elec. Eng. (AF 3220)	2:31
Chemistry	34:46
Agriculture	18:42
MURA	159:55
Inst. Comm. Res.	6:19
Elec. Eng. (Nobs 64732)	2:07
Dairy Science (9B1-B2)	:05
Ill. Public Welfare Dept. (44-32-66-342)	2:21
Ill. Public Welfare Dept. (Hurley)	1:19
Demonstrations	1:20
Miscellaneous	18:59
	<hr/> 556:20

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M. and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M., and 7:00 A.M. the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind,

a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 P.M. period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for June.

TABLE III

Drum	3
Control	2
Arithmetic Unit	3
Input-Output Unit	0
Punch	4
Reader	4
Memory	3
Power Supply	2
Unknown	6
Total	<hr/> 27

Comments on Auxiliary Drum Memory

During the month the head to drum spacing was decreased in such a way that the center-to-peak signal voltage from each head increased from 50 mv to

TABLE II

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DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
6/1/56	19:59	:01	1	(1) Two different results from same tapes	:00	:43	0
6/4/56	20:00	:00	0		:00	:51	0
6/5/56	19:57	:03	3	(1) Drum won't stay in synch. (2) " " " " " (3) Drum failure	:00	:58	0
6/6/56	19:57	:01	1	(1) 42 changed to 4K on R.H. side	:02	1:07	0
6/7/56	20:00	:00	0		:00	:43	0
6/8/56	20:00	:00	0		:00	:50	0
6/11/56	20:00	:00	0		:00	:50	0
6/12/56	20:00	:00	0		:00	1:27	0
6/13/56	20:00	:00	0		:00	1:11	0
6/14/56	20:00	:00	0		:00	1:08	0
6/15/56	20:00	:00	0		:00	1:20	0
6/18/56	19:45	:09	1	(1) Hangs up on 0-leftshift when reading in. Suspect white switch.	:00	1:07	0
6/19/56	17:31	2:25	4	(1) Two different results from same tapes. (2) Unknown error but a.c. line voltage is believed to have changed. (3) Memory error 0-1 position 2 ⁻²⁴ (4) -300V. Drum power supply failure	:04	:38	0
6/20/56	17:01	2:59	4	(1) Two different results from same tapes. (2) Punch "5" punched a K as an F (3) Suspect Reader K error (4) Leapfrog failed, Memory position 2 ⁻²⁴	:00	1:02	1
6/21/56	16:41	3:19	3	(1) Hang-up when started due to white switch (2) Hanging up (Leapfrog) broken wire to "B" gate on punch (3) Leapfrog failure indicated a punch "5" error.	:00	:45	1

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TABLE II (Continued)

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DATE	RUNNING OK TIME	REPAIR TIME	INTERRUP- TIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
6/22/56	18:49	1:11	4	(1) Tube failure (5844) in RI (2) Leapfrog due to reader "J" (3) -300V. Illiac power supply failure. (4) Leapfrog failure due to tube failure in RI	:00	2:13	2
6/25/56	19:32	:27	2	(1) Punch "3" not punching clean holes (2) Reader "B" bulb burned out.	:00	1:04	1
6/26/56	15:13	4:47	3	(1) Leapfrog failed, wouldn't print out. Sum check incorrect. (2) Two different results from same tape. (3) Tube failure in RI same as noted 6-22	:00	:58	2
6/27/56	19:59	:01	1	(1) Two different results from same tapes	:00	:51	0
6/28/56	20:00	:00	0		:00	1:01	0
6/29/56	20:00	:00	0		:00	1:26	0
TOTALS	404:24	15:23	27		13	22:13	6

60 mv for a 40 KC signal. As a result, intermittent drum test code failures caused by crosstalk were eliminated and the average gain tolerance ratio increased from 2.0 to 3.3.

A thermosthwitch was installed on the drum shell and the drum ac turn-on circuits were modified so that the drum motor is stopped if either the shell temperature rises to 38° or if the cooling unit blower is turned off.

Personnel

The personnel associated with the group and hence the contributors to this report are:

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