TEN-BIT SAMPLE AND HOLD OR
PEAK HOLD CONVERTER

BDX-613-1066

Published January 1974

Prepared by:
S. E. Grant
Department 864

Technical Note

NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Atomic Energy Commission, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

Technical Communications

**Kansas City
Division**

MASTER

DISTRIBUTION DOCUMENT

WTFD
Jeg

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

TEN-BIT, SAMPLE AND HOLD OR PEAK HOLD CONVERTER

The Circuit is basically a high speed Analog-to-Digital Converter (ADC) modified to retain only the peak amplitude. The peak hold feature is digital in nature and as such has no droop.

The analog input is buffered by U9 and then applied to a comparator and a difference amplifier. The comparator U8-A compares the output of the Digital-to-Analog Converter (DAC) (U10 and U12) and the analog input. If the input is greater than the DAC output, U8-A enables flip-flop U2-A. Flip-flop U2-A is needed to synchronize the asynchronous comparator with the clock to insure an adequate clock pulse width and to inhibit the oscillatory action of the comparator when the input is changing slowly.

The clock frequency is generated by the astable multivibrator made up of U1-A and U1-B. The output of flip-flop U2-A is applied to the up-down counters U3, U4, and U5. If the DAC used has complementary inputs such as the MN325 Micro Network DAC, the counters would be hooked up as a DOWN counter. If the DAC has positive inputs, simply hook up the counter as an UP counter and wire up the RESET instead of the SET inputs.

The counter will increase the DAC output until the input signal equals the DAC output, at which time the comparator disables U2-A and the operation stops.

In an effort to increase the speed of the circuit without requiring correspondingly higher device operating speeds, additional circuitry was added to provide high speed slew rate capability whenever the input was ≈ 0.7 volts greater than the DAC output. Amplifier U13 provides a difference signal of the input and the DAC output. Comparator U8-B compares this difference voltage against a reference voltage of 0.7 volts. If the error is sufficient, comparator U8-B enables flip-flop U2-B and, via the exclusive or gate U6-A, inserts

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Atomic Energy Commission, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

THE BENDIX CORPORATION

KANSAS CITY DIVISION

KANSAS CITY, MISSOURI

A prime contractor for the
Atomic Energy Commission
Contract Number AT(29-1)-613 USAEC

an extra pulse into counter U4, causing Bit 5 to increase by 1 count. Bit 5 is weighed at 0.156 volts, and this extra count will therefore not exceed the input.

The loop response time of the high slew-rate section is slower than the DAC portion and thus clocking is a bit critical. By using the output of Bit 2 on counter U5 for the clock to flip-flop U2-B, a delay of 4 clock periods is obtained. This allows the high slew-rate comparator time to determine if the last extra pulse was sufficient or whether another extra pulse is required. In this way, comparator U8-B senses an error >0.7 volt, inserts an extra pulse, and waits 4 clock periods before it can insert another extra pulse. Flip-flop U2-B is reset by gate U7-A after it has inserted the extra pulse.

The circuit begins operation upon receipt of a reset pulse. The enable to the counters (sample gate) allows operation of the circuit during a selected time period. One-shot U11 is shown here with a sample time of 60 microseconds. It is used to generate a sample interval at the trailing edge of the reset pulse by jumpering the sample gate to the output of the one-shot.

The time to reach peak for a 10-volt input square wave is approximately 15 microseconds with a clock frequency of 10 MHz. This represents a maximum sine wave tracking frequency of about 8 kHz.