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A METHOD OF IMPROVING ANALOG
COMPARATOR CALIBRATION ACCURACY

Special Report

Prepared by:
J. R. Doussard

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**Kansas City
Division**

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Department 864**

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A METHOD OF IMPROVING ANALOG COMPARATOR CALIBRATION ACCURACY

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Prepared by J. R. Doussard, D/864

A new calibration technique has been developed to set the limit values of analog-type voltage comparators. The merits of this technique include improved accuracy in setting the limit values, reduced calibration time, and digital readout of the as-found limit values and the comparator hysteresis.

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THE BENDIX CORPORATION

KANSAS CITY DIVISION

KANSAS CITY, MISSOURI

**A prime contractor for the
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SUMMARY

Product performance specifications often require monitoring of signal lines for minimum and maximum dc levels and pulse amplitudes. Monitoring is usually done on a Go/No-Go basis since a recorded value is not required. This type of signal monitoring can be done with an analog-type voltage comparator. The integrated circuit analog voltage comparator is widely used in this application since it is both accurate and economical.

The accuracy of the voltage comparator will depend on the accuracy of the instrumentation used in setting the comparator threshold level (limit value) and the comparator threshold stability. The threshold stability can be determined by recording the as-found threshold level during the calibration check.

A closed-loop ramp-generator calibration technique has been developed to provide digital-voltmeter readout of the comparator threshold level. The as-found comparator threshold level is automatically determined during the calibration check when this calibration technique is employed. This technique minimizes the time spent in conducting the calibration and provides an accurate measurement of comparator hysteresis.

DISCUSSION

One of the many problems encountered in test equipment design concerns dynamic limit processing on a Go/No-Go basis of pulse-type waveforms. This processing can include pulse counts of minimum amplitude and width, limit processing of dc levels, measurement of timing intervals, and other measurements. An integrated circuit voltage comparator can be a simple, accurate, and economical device for implementing this type of signal processing.

The integrated-circuit voltage comparator is simple in operation since it is essentially a bistable device that changes state when a predetermined threshold level is exceeded. It is inherently accurate if the required error voltage in excess of the threshold is a small percentage of the threshold value and if the drift of the threshold level is a small percentage of the allowable error tolerance of the measured parameter. The integrated circuit voltage comparator is suitable for this application because it is a high gain device that switches state in the nanosecond range and because its chip-type construction minimizes thermal drift. Mass production technology, coupled with quality control, has made this type of device economically attractive for automated tester use.

One of the disadvantages of this type of analog limit processing is the amount of time spent in calibrating the voltage comparators. This results from the multitude of signal levels that must be processed. Each signal level requires an individual comparator which must be accurately calibrated. The calibration of each comparator usually requires a specific amplitude which must be generated to calibrate the comparator threshold level. This process can be time consuming and should be avoided if a better calibration technique can be devised.

Another complication of this signal processing technique concerns the accurate setting of the comparator threshold level. A signal of calibrated amplitude and width is normally used to adjust the threshold level. An amplitude error of 0.5 to 1.5 percent is not uncommon for the calibration signal pulse, requiring that the comparator be adjusted to compensate for this inaccuracy. There is a need for a better calibration technique in which the accuracy limitation in setting the threshold level is determined by calibration instrumentation with inaccuracies in the range of 0.1 to 0.01 percent. An accuracy requirement of this magnitude requires the use of digital-type instrumentation. For that reason, all threshold levels should be measured using a digital voltmeter (DVM).

Another possible limitation in using this technique involves determining the as-found threshold level. This is a significant measurement because it is indicative of the threshold stability. Threshold stability is an important factor in maintaining the integrity of the tester performance after calibration. It is second only in importance to the initial calibration accuracy. A convenient method of checking the threshold level stability is to include the as-found threshold level in the recorded calibration data and thereby establish a threshold stability performance level. This information can be used as a limiting criterion in determining the calibration interval. Thus, the as-found threshold level should be included in the periodic calibration check.

Any improved calibration technique devised for adjusting the threshold level of a voltage comparator should minimize the time spent in conducting the calibration and allow the as-found threshold level to be checked for an out-of-tolerance condition while maintaining or improving the calibration accuracy. In some instances, the comparator hysteresis may need to be measured; therefore, any improved technique should provide an accurate method of making this measurement.

The ideal technique for determining the threshold level of a voltage comparator is to gate the comparator with a voltage ramp that will steady-state out at the threshold level without overshoot. This dc level is then measured by a DVM. If the steady state threshold level is then allowed to ramp down to a new steady state value without undershoot until the comparator changes state and this value is measured by a DVM, the hysteresis (the difference between the measured values) can be calculated.

This calibration technique eliminates the tedious task of calibrating a signal source because the signal source automatically ramps to the as-found comparator threshold level and is read out on a DVM. If the threshold level must be changed, the comparator potentiometer can be adjusted and the new value can be measured with the DVM. The hysteresis of the comparator can be measured by ramping the threshold voltage to a lower dc level and measuring this value when the comparator output changes state. Figure 1 shows a block diagram of this calibration technique.

The block diagram of the closed-loop ramp calibration generator shown in Figure 1 also shows waveforms that are typical for the system operation. Basically, the generator is composed of a well regulated dc voltage source that is used as the forcing function for an integrator. The integrator produces a voltage ramp that is buffered by a memory hold circuit with unity gain. The memory circuit output is an accurate reproduction of the input, scaled to the appropriate limit by the range switch. The voltage ramp is then monitored by a DVM and used as the signal voltage for a typical analog amplitude comparator to be calibrated.

The analog amplitude comparator is normally biased into negative voltage cutoff by a predetermined threshold level. However, when the amplitude of the voltage ramp exceeds the comparator threshold level by approximately 1 to 2 millivolts, the comparator switches into the positive saturated output-voltage state. The output voltage of the amplitude comparator then activates a solid state transistor switch, removing the integrator input-forcing voltage and allowing the integrator to steady-state out at the amplitude comparator threshold level. This threshold level can be read accurately on the DVM.

At the option of the calibration technician, the output voltage of the amplitude comparator can be used to initiate a reset timer which resets the integrator and memory-hold circuit to zero voltage and allows the cycle to repeat. In this mode (AMPLITUDE) of operation, the DVM will display the amplitude comparator threshold level as a single value.

If a hysteresis measurement on the comparator is a calibration requirement, the reset switch is left in the hysteresis mode and the ramp voltage is allowed to decay until the voltage comparator output state changes. The DVM monitor in this mode of operation ranges between two values. The difference in the two values is the comparator hysteresis.

Use of an interval counter to calibrate a typical pulse width comparator is also illustrated in Figure 1. The positive output-voltage pulse of the amplitude comparator initiates the interval counter count. At the same time, this output voltage pulse is integrated by an RC network and the count is stopped when the amplitude of this voltage integral exceeds the threshold level of the width comparator. The digital readout of the counter is a direct measure of the pulse-width comparator limit value.

Figure 1. Block Diagram of Closed-Loop Ramp Calibration Generator