LA-5430-MS

INFORMAL REPORT

LA-5430-MS

175
12-6-73

24,507

Nova Branch-Driver Operation

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UNITED STATES
ATOMIC ENERGY COMMISSION
CONTRACT W-7405-ENG-36

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Printed in the United States of America. Available from
National Technical Information Service
U. S. Department of Commerce
5285 Port Royal Road
Springfield, Virginia 22154
Price: Printed Copy \$4.00; Microfiche \$1.45

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LA-5430-MS
Informal Report
UC-32

ISSUED: October 1973

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Nova Branch-Driver Operation

by

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Supported by the USAEC Division of Research

This report supersedes LA-4682-MS

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NOVA BRANCH-DRIVER OPERATION

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ABSTRACT

The Branch Driver (BD) is the interface between a Nova or Supernova computer I/O and a multicrate CAMAC system.

The first section of the manual discusses the operation and design specification of the BD and has a description of the instructions used. The complete set of non-CAMAC instructions for the BD is given.

The manual also contains programming examples for several types of modules and the standard function codes for CAMAC. A complete set of schematics is available, but is not included.

The Branch Driver (BD) is the interface between a Nova or Supernova computer I/O and a multicrate CAMAC system, and was designed to CAMAC specifications 4600a. The crate controllers are the standard Type "A's" (Fig. 1.).

The BD was designed with TTL logic and the CASH hardware system, and is housed in a DC-01 chassis. The chassis has a 5V, 5A power supply. The BD has only a programmed mode of operation.

The computer I/O connectors on the BD are parallel AMP connectors. This allows for a daisy-chain I/O. If the BD is the last unit in the chain, install the terminator IC's; if not, remove the IC's. The total I/O length should be <50 ft.

The daisy-chain I/O going to the type "A" controller from the BD is called the "branch port." Five terminator IC's are designed into the BD for the BD termination, but can be removed. The BD has one Hughes connector, but a second can be added if desired. The chain is from one type "A" to the next, up to seven; the last unit goes to a terminator which may be in a CAMAC module or external. For short branch ports, the last terminator may not be

required. The port length determines the skew set into the one-shots in the port. The shorter the branch, the faster the cycle.

The dataway cycle is 1-1.6 μ sec and, depending on the length of the branch, several hundred additional nsec are added. Branch cycle time should be 1.5-2 μ sec.

The length of the branch is limited by the cycle time and cable losses. The standard port is single-ended and, with #24 twisted-pair cable, is limited to 50 ft.

In addition to CAMAC specifications 4600a, 4100a and "How to Use the Nova" were used as references.^{1,2,3}

The BD was assigned a device code of 40 octal; this can be changed with wiring changes on the RC-2 address header. Any mask bit (9-15) can be assigned with instruction MSKO to disable the BD interrupt. Mask bit one was assigned. This interrupt, if enabled, is set by branch demand signal from all the crates. It is in "OR" of all the L-requests in the crates.

Fig. 1 CAMAC CRATE CONTROLLER TYPE A
(diagram shown for double-width unit)

With generation of interrupt from L-request, the computer identifies the unit interrupting with an INTA instruction which reads in the address of highest priority-interrupting device. The BD is wired for octal 40 as address. This can be changed with wiring change on the address header, RC-2.

The INTA Instruction generates a BG operation which is called a "graded-L" operation. This command reads the L pattern from all on-line crates into the 24-bit read buffer. The L's from all crates are OR'ed into one word. The pattern can be read into the computer with DIB/DIC instructions. In some systems the L's will be taken to a grader unit, where an address is generated for the highest priority L and that address is then supplied to the computer over the read lines. This address could be a jump to the appropriate routine. Without a grader, the L pattern has to be examined within the computer.

If the system is operated such that the interrupt can break into a chain of events, then the command and data buffers should be saved and restored

after the interrupt (if appropriate). The save/re-store must be done with computer instructions.

The Nova-CAMAC instructions are shown in Table I. The instructions set was chosen to be program-compatible with the NOVA Crate controller.

- DOA ac, 40 Loads the command register with FNA and modifier bits. The bit assignments are shown in Table I, as well as the modifier bits code. The incrementing is done with an pulse generated at the completion of each CAMAC cycle.
- DIA ac, 40 Read command register into ac. Used for testing and saving registers.
- DOB ac, 40 Load write buffer 16-1 with contents of ac, 0-15.
- DOC ac, 40 Load write buffer 16-17 with contents of ad, 8-15, BCR's 1-7 with contents of ac, 1-7.
- DIB ac, 40 Read buffer 16-1 into ac, 0-15.
- DIC ac, 40 Read buffer 24-17 into ac, 8-17 BCR's into ac, 1-7, BX in 0.

NOTE: DOB's and DOC's can be executed only if the

Write Function Code (F16) is in the A Register.

In command mode the Read-Write buffers are used because CAMAC uses a 24-bit word, while Nova is 16-bit. In BG or graded-L mode, the read lines and buffer register are loaded with the sum of the L's from all crates on-line. L23-L0 is loaded into Read buffer 24-1. If L grading is used, the address of the highest priority L is in the read buffer.

The BCR's are the crate address; each crate has a separate line. Bit 1 of the BCR register is bit 1 of ac. The branch has 7 BCR lines and 7 BTB lines. The BCR register can be loaded from the DOC instruction bits 1-7 or a BTB mask. If a crate is on-line and the DOC instruction requests it be set, it is stored in BCR register. The register can be tested with DIC. In a graded-L operation, the BCR register is loaded with all on-line crates, then operation is initiated. The pattern can be checked with the DIC instruction. The crate number is selected at the type "A" controller with a switch. Care must be taken in setting up a branch to be sure two controllers do not have the same number. The branch driver does not have a time-out feature for BTB's and with an error on this line, the BCR's test will be very useful. If required, a one-shot can be added to time-out if BTB's do not respond in 10 μ sec. If BD is used for a one-crate system, then the BCR line could be wired on or add switches for the BCR pattern.

NIOS 40 Start branch operation, sets busy. The BTA signal, which is the CAMAC start is 3 gate delays from the start pulse. Start also sets the branch busy F-F and resets the branch demand F-F, which is what generates an interrupt of L-request in the system.

SKPEN 40 Skip if branch busy.

SKPBZ 40 Skip if branch not busy.

SKPDN 40 Skip if Q=1 for last command.

SKPDZ 40 Skip if Q=0 for last command. The Q F-F and Interrupt F-F are reset with start, clear, and IORST.

IORST BZ operation, which is a Branch Initialize overrides all other commands. It is a 10 μ sec. pulse on the port BZ line. The system cannot be used for 10 μ sec. with an IORST instruction.

INTA ac Was explained with interrupts. Used to identify source of interrupt and if BD was the source, then starts a graded-L operation. Doing an INTA instruction will change the contents of BCR register and read buffer. Following an INTA, BCR will contain 1's for all on-line crates. If this is a problem, then these registers must be read into the computer before INTA and restored after INTA, if the BD was the interrupt and the register status is needed.

MSKO ac The IORST instruction enables all interrupts and they must be masked off with the MSKO instruction and the appropriate bit pattern in ac. A one-bit at the assigned Data X location will disable interrupt; a zero bit will enable. Bit 1 has been assigned BD.

C-suffixed Clears command register, FNA and modifier bits set to zero.

S-suffixed Start branch operation--same as NIOS.

P-suffixed Not used with program mode.

BASIC SYSTEM STRUCTURE

A CAMAC crate has 25 single-width module N stations. They are numbered left to right from the front. The type A controller rests in 24 and 25; therefore, 1-23 are open for modules. Each module may have several registers addressable with the 4-bit subaddress A. Each crate has a number, switch-selected in the type A controller. The number selected is the BCR and BTB number for the crate. The branch can have up to seven crates, 1-7 numbered. The crate (BCR) and N station is the address of any module and the A subaddress selects the register within a module. The function to be accomplished in the module is specified with a 5-bit function code. The 32 standard functions are listed in Table II. The FNA is stored in the command register with the two modifier bits, i.e., the function, station number, and the subaddress. The crate number is in the BCR register. The data buffers are 24 bits long and two computer instructions are required to read or load the buffers. For a write operation, load the command register then the data buffer and the BCR register, followed by a CAMAC start pulse, S or NIOS. If data is accepted,

then Q=1 response can be tested and used to increment address. For a read operation, the BCR register and command register are loaded and followed with a start pulse. The Q=1 response indicates data is in a buffer and can be read into the computer.

Programming Examples

Example 1: Read 24-bit scaler (Model 2550).

(Assume BD has device address of 40_8 and BCR register correct.) The scaler is at station 5 and the third scaler of quad and modifier bits is not used.

```
LDA 3,STORE ; Set storage index.
LDA 0,C ; Fetch command.
LOOP: DOAS 0,40 ; Load C-register and
              read scaler.
DIC 1,40 ; 8 MSB into 8-15 of ac.
STA 1,0,3 ; Store.
DIB 1,40 ; 16 remaining bits.
STA 1,1,3 ; Store.
,
,
,
```

C: 2+120+0 ; Command A=2, N=5, F=0.

STORE: (address of data storage)

The above example will work for Nova and probably for Supernova; however, after the DOAS instruction which starts CAMAC, the next instruction is a DIC and this could be a problem if the CAMAC cycle time is greater than the time between the start pulse and the read-in of the data. Also, without testing the Q response of the operation, there is not any assurance the operation was successful. If the cycle time is not a problem, then Q could be tested by adding the following instruction after DOAS:

```
SKPDN 40 ; Test for Q=1.
JMP Loop or Error Q=0 Try command again.
Error message.
```

With a fault in the system, the above example could result in an endless loop, unless one put in a time-out loop of some type. You could try 5 times, then generate an error message. If timing is a problem, then speed up CAMAC, or put an NIO instruction after DOAS and before Q test.

Example 2: Read 32, 24-bit scalars using modifier bit. The scalars are at stations N1-8 and are Model 2550. BD address 40_8 and BCR register set correctly.

```
SUBO 2, 2 ; Clear ac.
LDA 0, COUNT-1
STA 0, COUNT
LDA 3, STORE ; Storage index.
LDA 0, C ; Command.
DOA 0,40 ; Load C reg. and start
          read.
```

```
LOOP: NIOS 40
      NIO ; Delay if required.
      SKPDN 40 ; Test Q=1.
      NIOS 40 ; Q=0, Tried to read A4.
      INC 2,2 ; Count Q=1 responses.
      DIC 1,40 ; 8 most sig.
      STA 1,0,3 ; Store.
      DIB 1,40 ; 16 bit.
      STA 1,1,3 ; Store.
      INC 3,3 ; Increment Store Index
      INC 3,3
      DSZ COUNT
      JMP LOOP
      LDA 0, COUNT-1 ; No. of Q=1 responses req.
      SEQ 0,2 ; Test No. of Q=1 responses.
      JMP ERROR ; Incorrect Q=1 count.
      ,
      ,
      ,
```

```
C: 20+140000 ; Command A0, N1, F0
          MA=MN=1.
      40 ; Initial value of loop
          3210
COUNT: 0 ; Loop counter.
```

STORE: (ADDRESS)

Example 3: Clear scaler in Example 2.

```
LDA 0, COUNT+1 ; Set up loop.
STA 0, COUNT
LDA 0,C ; Get command.
DOA 0,40 ; Load C register.
LOOP: NIOS 0,40 ; Start.
      DSZ COUNT
      JMP LOOP
      ,
      ,
      ,
COUNT: 0
      10 ; Value of loop counter.
C: 20+14000+4000 ; Command A=0, N=1, F=9,
          MN=1.
```

The clear function on each quad scaler can be wired to clear all four scalers with one command. If this is unsatisfactory, then each scaler has to be addressed, as the auto increment feature of the BD will not operate without a Q=1 response.

Example: Read ADC's (Model 2243). N=11, 12
BD address 40₈, BCR register set.

```
LDA 3,STORE      ; Storage index.
LDA 0,C          ; Get command.
DOAS 0,40        ; Load C register, read ADC.
NIO 0            ; Delay if required.
SKPDN 40         ; Test Q=1
JMP ERROR        ; Q=0.
DIBS 1,40        ; Read in data 1-16.
STA 1,0,3        ; Store data ADC #11.
SKPDN 40         ; Test Q=1.
JMP ERROR
DIBS 1,40
STA 1,1,3        ; Store data ADC #12.
LDA 0,C+1        ; Clear command.
DOAS 0,40        ; Load C, clear ADC #11.
NIO 40           ; Clear ADC #12.
```

C: 260+40000 ; A=0, N=11, F=0, MN=1.

260+11000+40000 ; A=0, N=11, F=9, MN=1.

STORE: (ADDRESS OF DATA STORAGE)

Reads 9 bits into 2⁰ to 2⁸ of branch. MSE is overflow.

Example 5: Read fast coincidence latch (Jorway Model 63). N=14, BD=40.

The unit has a control word which is a mask for inputs, also the L line must be enabled. Command (F-2) will read and reset the latches at time S=2,

or use F(0), F(9) separately to read and reset. Z disables L, resets control word and latches.

```
LDA 0,MASK      ; Mask for latches.
Ini- DOB 0,40    ; Output to BD.
tia- LDA 0,C+2   ; Command to control word.
lize : DOAS 0,40 ; Store mask in CW.
module LDA 0,C+1 ; 2nd command.
for DOAS 0,40    ; Enables L.
event '
'
'
After LDA 3,STORE ; Read and reset command.
inter- LDA 0,C
rupt DOAS 0,40    ; Start CAMAC, read and re-
set.
NIO 0            ; Time delay if required.
DIB 1,40         ; Read in-latch data.
STA 1,0,3        ; STORE
'
'
'
MASK: 7777      ; First 12 latches ON.
C: 2000+340     ; A=0, F=2, N=14, read and
reset.
32000+340      ; A=0, F=26, N=14, enable L.
20000+340      ; A=0, F=16, N=14, load CW.
STORE: (ADDRESS)
```

First 10 bits of latch are stored in 2⁰ to 2⁹ of BD and register reset. In the read routine, the Q response is not tested because if incorrect, the data is lost anyway. If this is unsatisfactory, then the latches can be read with F(0) command and the Q tested; if correct, then store, then reset the latches with an F(9) command.

TABLE I
NOVA-CAMAC INSTRUCTIONS

DOA ac,40 Load crate or branch command (FNA, mode).
DIA ac,40 Read command into computer.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MA	MN	F ₁₆	F ₈	F ₄	F ₂	F ₁	N ₁₆	N ₈	N ₄	N ₂	N ₁	A ₈	A ₄	A ₂	A ₁

Nova word
CAMAC command

N - station address, A - subaddress, F - function code

MA MN Modifier bits

0 0 No action.
1 0 Increment subaddress A.
0 1 Increment station address N.
1 1 Increment A, if Q=1; increment N and reset A, if Q=0.

DOB ac,40 Load data buffer 16- 1 with ac 0-15.
DOC ac,40 Load data buffer 24-17 with ac 8-15, BCR's 1-7.
DIB ac,40 Read data buffer 16- 1 into ac 0-15.
DIC ac,40 Read data buffer 24-17 into ac 8-15, BCR's 1-7, X Flag into 0.
Note: BCR's 1-7 use data bit 1-7 (each "BCR" bit selects one crate, can have up to 7 crates). Crate number is set into type "A" controller with switch.

NIOS 40 Start branch operation with command in branch.

Branch Driver

SKPDN 40 Skip if Q=1.
SKPDZ 40 Skip if Q=0.
SKPEN 40 Skip if Branch Busy.
SKPBZ 40 Skip if Not Busy.

INTA code into bits 10-15 of ac and start BG.
DIB ac,40 and DIC ac,40 used, then to read L pattern into computer, L₁₅-L₀ into 0-15 and L₂₃-L₁₆ into 8-15.

MSKO ac Set mask interrupt flags (one bit disables interrupt).
IORST BZ operation INITIALIZE.
C-suffixed It does a Branch Driver clear operation.
S-suffixed Start branch operation.

TABLE II
THE FUNCTION CODES

No.	Function		F 16	F 8	F 4	F 2	F 1	No.
0	Read Group 1 Register	)	0	0	0	0	0	0
1	Read Group 2 Register	)	0	0	0	0	1	1
2	Read and Clear Group 1 Register	)	0	0	0	1	0	2
3	Read Complement of Group 1 Register	)	0	0	0	1	1	3
4	Non-standard	)	0	0	1	0	0	4
5	Reserved	)	0	0	1	0	1	5
6	Non-standard	)	0	0	1	1	0	6
7	Reserved	)	0	0	1	1	1	7
8	Test Look at Me	)	0	1	0	0	0	8
9	Clear Group 1 Register	)	0	1	0	0	1	9
10	Clear Look at Me	)	0	1	0	1	0	10
11	Clear Group 2 Register	)	0	1	0	1	1	11
12	Non-standard	)	0	1	1	0	0	12
13	Reserved	)	0	1	1	0	1	13
14	Non-standard	)	0	1	1	1	0	14
15	Reserved	)	0	1	1	1	1	15
16	Overwrite Group 1 Register	)	1	0	0	0	0	16
17	Overwrite Group 2 Register	)	1	0	0	0	1	17
18	Selective Overwrite Group 1 Register	)	1	0	0	1	0	18
19	Selective Overwrite Group 2 Register	)	1	0	0	1	1	19
20	Non-standard	)	1	0	1	0	0	20
21	Reserved	)	1	0	1	0	1	21
22	Non-standard	)	1	0	1	1	0	22
23	Reserved	)	1	0	1	1	1	23
24	Disable	)	1	1	0	0	0	24
25	Increment Preselected Registers	)	1	1	0	0	1	25
26	Enable	)	1	1	0	1	0	26
27	Test Status	)	1	1	0	1	1	27
28	Non-standard	)	1	1	1	0	0	28
29	Reserved	)	1	1	1	0	1	29
30	Non-standard	)	1	1	1	1	0	30
31	Reserved	)	1	1	1	1	1	31

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