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Westinghouse Astronuclear Laboratory

OPERATIONAL MANUAL AND ACCEPTANCE TEST PROCEDURES
FOR
ETS-1 AVERAGE AND REJECT CHASSIS (Log Nuclear Instrumentation)
Model 938J166G01

MASTER

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Procedures for ETS-1 Average and Reject
Chassis (Log Nuclear Instrumentation)
Model 938J166G01

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ETS-1 AVERAGE AND REJECT CHASSIS OPERATIONAL MANUAL

(Log Nuclear Instrumentation)

1.0 INTRODUCTION

This operational manual contains the general description, theories of operation, alignment procedures, maintenance and repair data, and interconnection diagrams for the WANL ETS-1 Average and Reject Chassis for the Log Nuclear Instrumentation system.

1.1 General Description

The WANL ETS-1 Average and Reject Chassis is a rack mounted, wholly self-contained, all solid state electronic averaging and rejection circuit. It is a card rack assembly mounted in a chassis drawer. The instrument electronically averages the input signals, automatically rejects any input outside of an adjustable "reject" band from this average and provides an output signal equal to the average of the inputs not rejected and an output signal proportional to the period (rate of change) of the average signal.

The instrument has provision for manually rejecting inputs and inhibiting the automatic rejection of channels. Redundancy in the averaging system insures that a single instrument failure will not result in loss of the output average signal.

2.0 GENERAL DATA

2.1 Safety Precautions

None other than standard, good-practice safety precautions need to be observed. No high voltages, other than ± 15 VDC from the external primary power source,

are present in the unit. The maximal voltage is 30 volts DC. If it should become necessary to perform corrective maintenance, component removal, or service, prudence dictates that the unit should be disconnected from the primary power source by disengaging the multi-pin power connector, J1, or by performing such activity during system down-time.

2.2 Weight and Dimensions

The WANL ETS-1 average and rejection circuit has the following gross physical characteristics:

Weight	lbs.
Dimensions	19" wide
	19" deep
	7" high

2.3 Power Requirements

Primary power for the WANL ETS-1 Average and Reject Circuit is plus and minus 15 VDC. This power is obtained from a source external to the unit and enters the unit, along with other circuits, via a multipin 16 connector, J1.

2.4 Heat Dissipation

All components have been selected to the end that special subsystem heating, cooling, or ventilation is not necessary. Adequate separation of modules and printed circuit assemblies provide satisfactory up-draft.

2.5 Salient Design Characteristics

The Average and Reject Chassis mounts all solid state components, with minimal use of moving parts, variable controls, adjustments, and switches consistent with

optimal performance. While designed to good commercial practices this equipment embodies the high standards required by military specifications. All components are unusually rugged, sturdily built, and held to close tolerances without overload. Long term (40,000 hours), trouble free operation is assured throughout the nonobsolescent life of the equipment.

3.0 AVERAGE AND REJECT CHASSIS DETAILED DESCRIPTION

3.1 The Average and Reject Chassis contains printed card modular circuitry in the following major services: Averaging Networks, Averaging Amplifiers, Comparators, Trigger Pulse Amplifiers, Flip Flops, Auto-manual reject Circuits, Buffers, and a period amplifier. Westinghouse Drawing 936J166 shows the locations of these major modules. Figures 1, 2, and 3 are photographs of the top view, front view, and bottom view of the unit.

3.2 Resistors

Resistors are a military standard (1% RN); wire wound where necessary.

3.3 Capacitors

Capacitors are of military standards or superior.

3.4 Transistors and Diodes

All transistors and diodes are military standard or superior, and are silicon.

3.5 Operational Amplifiers

All operational amplifiers are of the highest grade, purchased to the maximum in reliability testing and performance.

Figure 2

Front View - Average and Reject Chassis Log Neutronic System

Figure 3

Bottom View - Average and Reject Chassis Log Neutronic System

3.6 Chassis

Aluminum alloy - sheet stock, bolt and rivet construction. Card slots are plastic.

3.7 Meters

Meters are Westinghouse KX241.

4.0 INSTALLATION INSTRUCTIONS

4.1 Average and Reject Chassis

The following procedure should be used for the proper installation.

Mount the removable part of the chassis guides at the desired selected level in a standard 19-inch rack. WANL Drawing 936J166 gives the mounting dimensions, plan view, and construction details of the chassis, panel, and connectors.

Refer also to Westinghouse Astronuclear Drawing 938J901 (Wiring Diagram). This drawing shows, in addition to the internal wiring, the external service connections that are to be made to the unit, via the connectors at the rear of the chassis.

5.0 PRINCIPLES OF OPERATION

The average and reject chassis averages the input signals, establishes a reject band around this average (this reject band is adjustable within the equipment), rejects any one channel that is outside this band, and provides an output signal equal to the average of the inputs not rejected.

Remote operation of instrument relays allows for manual rejection of up to a total of two channels (all three cannot be rejected) and for reactivating a channel

which has been rejected. Other controls provide for inhibiting the automatic rejection of selected channels.

Two averaging amplifiers are redundant upon each other and their outputs are auctioneered. Circuitry in the average and reject chassis senses when an averager is malfunctioning high and rejects this average amplifier, however, only one of the two average amplifiers will be rejected by this circuitry.

The average signal is fed to additional circuitry in the chassis which generates an output signal proportional to the rate of change, or period, of the average signal.

The four major functional circuits in the chassis are as follows: the averaging circuits, the automatic and manual rejection circuits, the averaging amplifier rejection circuits, and the period circuit. The operation of each of these functional circuits are described individually in the following sections.

5.1 The Averaging Circuits

The averaging amplifiers including the field effect switches used for rejection, are shown on schematic drawing 936J150 as modules A1 and A2. The following description is with respect to A1. Amplifier AR1 is a high gain operational amplifier. Resistors R_3 , R_5 , and R_7 are the input resistors and R_4 , R_6 , and R_8 the feedback resistors. These are paired: R_3 and R_4 , R_5 and R_6 , and R_7 and R_8 . When all of the rejection circuits are in the not rejected state, the input resistance is the parallel combination of all 3 input resistors, 33.3K and the feedback resistance likewise the parallel combination of all 3 feedback resistors, 33.3K. This makes the gain of the averager unity with the output equal to the average of the

three input signals.

When one of the reject field effect switches opens, the input and feedback resistors associated with that reject switch, R_3 and R_4 with Q_1 , R_5 and R_6 with Q_2 , and R_7 and R_8 with Q_3 are both disconnected. If Q_1 opens, R_3 and R_4 are disconnected from the operational amplifier input. The input resistance is 50K and the feedback resistance is the parallel combination of the two remaining resistors, R_6 and R_8 , 50K keeping the gain of the overall circuit at unity while making the output the average of the remaining two inputs. The circuitry into the amplifier negative input including resistor R_3 and potentiometer R_2 provides amplifier current offset adjustment while voltage offset adjustment is accomplished via potentiometer R_1 . A capacitor around the operational amplifier provides an upper frequency cutoff, limiting the response of the circuit at high frequencies. Diode CR4 along with resistors R_6 and R_7 are used to eliminate the voltage drop of the auctioneering diode CR4 on Module A4. The voltage drop across diode CR4, which is in the feedback loop causes the averager output at TP6 to be approximately 0.6 volts high. This same voltage drop across diode CR5 then makes the average output a true average of the inputs.

5.2 Automatic and Manual Rejection Circuits

5.2.1 Automatic Rejection

There are three automatic and manual rejection channels in the averaging and rejection chassis, one for each of the three log input signals. With reference to Schematic Drawing 936J150, each channel is comprised of a comparator such as Module A9, a trigger pulse amplifier as shown on Module A14, a flip-flop as shown on Module A18, an auto-manual reject circuit as shown on Module A20, and a relay driver as shown on Module A23. Each channel operates as follows: The input log signal (log sig. no. 1) is compared with the averager amplifier output (AVE LOG) in the comparator amplifier. The output of the comparator (Module A9)

at TP11 is a signal which is proportional to the difference between the two inputs but always negative. This is accomplished by means of an operational amplifier AR1 connected to produce the absolute value of the input.

Whenever the difference between the log signal and the averager output is positive, the amplifier AR1 reference is grounded through diode CR4 on Module A9 and the circuit becomes essentially a conventional inverting amplifier with the feedback tapped off of a voltage divider made up of resistors R_{10} and R_{11} . This provides a stage gain of 11. When the difference between the log input signal and the Averager output goes negative, the reference is connected directly to the input and the circuit now has the form of a voltage follower, which is non-inverting. The feedback is taken across the output voltage divider made up of R_{10} and R_{11} providing the gain of 11 in this mode the same as in the before-mentioned mode. The diode drop across diodes CR1 and CR2 are compensated for by the offset through the offset adjust potentiometer R_1 . The output of the absolute value comparator versus the difference input is shown on Figure 4.

The output of the absolute value comparator is fed to the trigger pulse amplifier. If the absolute output becomes greater than the trip set (Reject Adjust, R_1 on Module A14), the trigger pulse amplifier trips and the output of the trigger pulse amplifier at J16 pin 8 goes to zero volts from its normal 15 volt level. If any other channel (Channel 2 or 3) is rejected, a signal inhibiting automatic rejection of Channel No. 1 is fed into the trigger pulse amplifier. This is a normally 15VDC signal and is fed into the trigger pulse amplifier at Pin 6 of J16. This plus 15 volt signal overrides the absolute output and prohibits the trigger pulse amplifier from being switched on by the absolute value comparator. This input, therefore, prohibits the automatic rejection of the channel if any other of the channels has already been rejected.

FIGURE 4
ABSOLUTER OUTPUT VS
DIFFERENCE INPUT

SK0917CEH1570A

Relay K1, with normally closed contacts K1A, is the inhibit relay (Module A12). When this relay is operated the output of the absolute comparator is disconnected from the input to the trigger pulse amplifier and no automatic rejection can be made.

The output of the trigger pulse amplifier feeds the flip-flop amplifier. When the trigger pulse amplifier is tripped, the flip-flop goes to the reject state, Q_2 off and Q_1 on. As long as the trigger pulse amplifier is tripped, the flip-flop will stay clamped in this state. Operation of the Active/Reject Relay, K2A will not cause a change in the flip-flop state. If the trigger pulse amplifier is not tripped, no automatic rejection condition exists, then operation of the Active/Reject Relay will cause the flip-flop to change state every time the relay is operated, and the circuit will be rejected and activated on alternate operations of the momentary action Active/Reject Relay.

If the channel was rejected by a trip of the trigger pulse amplifier and subsequently the absolute amplifier output returns to normal, operation of the active/reject switch will cause the flip-flop to change states back to the active condition.

The output of the flip-flop which is normally 0 when the circuit is active (Pin 8 of J20) is fed to the auto-manual reject circuit (Pin 12 of J22). When the flip-flop goes to the reject state this signal is plus 12 volts which turns on transistor Q_1 in the auto-manual reject module. This in turn turns off transistor Q_2 which causes a +15 volt output at pin 14 of J22 and turns off the field effect switch at the input of the averaging circuit (see Figure 1) if transistor Q_3 is off. Transistor Q_3 is normally off. It is turned on only if the alternate two channels are rejected. This provides protection against all three channels being rejected at the same time.

The output of the reject circuit is also fed through a relay driver, Module A23, to relay K_1 which provides contact closures on reject of the channel for use in indication of a reject state of the channel.

5.2.2 Manual Rejection

The manual rejection of a channel is accomplished by operation of the Active/Reject Relay K2A, Module A16, on the input of the flip-flop. When the flip-flop is in the active state (its output at J20 Pin 8 at zero volts) then operating the Active/Reject switch will cause the flip-flop to change to the reject state. A second operation of the switch will cause the channel to be reactivated.

When two channels are rejected, regardless of the manner in which they were rejected then transistor Q_3 in the auto-manual reject circuit is turned "on". When this occurs, the condition of the reject transistor Q_2 no longer makes any difference since it is in parallel with Q_3 . Transistor Q_3 is biased to be "off", or open circuit for all rejections up to one and to go "on" on the second rejection.

The manual rejection is direct, that is it does not pass through the inhibit switch and is, therefore, not affected by the state of the channel, inhibited or not.

5.3 The Averaging Amplifier Rejection Circuit

The Averaging Amplifier Rejection Circuit is comprised of the following modules:

1. High Signal Selector, Module A3
2. Reject Circuit, Module A4
3. Trigger Pulse Amplifier, Module A5

5.3 The Averaging Amplifier Rejection Circuit (Continued)

This circuit senses when either of the averager amplifiers output is above the highest input and when this occurs, rejects that averager amplifier. If an averager fails low this output is eliminated by virtue of the auctioneering of diodes CR4 and CR5 in Unit A4. This auctioneering action provides an output which is the highest of the two redundant averaging amplifiers.

The active log input signals are auctioneered by diodes CR1, CR3, and CR5 if any channels are in a reject state, field effect transistors Q_1 through Q_3 , as required, are open circuited. The highest of the active inputs is fed as one input to trigger pulse amplifier A5. The other input to the trigger pulse amplifier is the output of the averager amplifier. Each averager feeds one of the trigger pulse amplifiers. The trip adjusts are set such that if the output of an average amplifier is higher than the highest active channel input, the trigger pulse amplifier trips. The -15V output of the trigger pulse amplifier is fed to the rejection transistor Q_2 or Q_3 , as applicable, causing the transistor to go off, or open circuit, thereby removing this averager output from the auctioneering diodes. In this state only the alternate average amplifier is connected to the output. In addition to opening the reject transistor, operation of the reject trigger pulse amplifier operates the auto reject inhibit field effect switch on the alternate averager reject circuit, Q_1 or Q_4 of A4, prohibiting the possibility of a rejection of both averagers.

5.4 Period Circuit

The period circuit generates an output signal, proportional to the rate of change (period) of the input signal. This input is the average log output. Module A7 is the average period circuit. Module A6 is the buffer amplifier which is interposed between the average log output and the period input. This buffer is a unity gain, non-inverting operational amplifier circuit used to isolate the period circuit.

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FIGURE 5 PERIOD CIRCUIT OUTPUT VOLTS AND IND. VS INVERSE PERIOD

606241A

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There is an output from the buffer amplifier taken to the external connector so that this signal can be utilized where a buffered log output is required.

The output of the buffer is fed to the input of the period circuit (connector J9 Pin 9). The average period circuit is an operational amplifier differentiation circuit. The output vs input characteristic is as shown on Figure 5. For periods between -10 seconds to +1 seconds the differentiation is accomplished by input capacitor C_1 on the operational amplifier and feedback resistors R_6 and R_7 . The noise amplification of the circuit is limited by including a second breakpoint in the response of the circuit. This is done by means of resistor R_3 on the input and capacitor C_2 in the feedback circuit. For periods longer than 1 second, the feedback loop through R_5 is not effective since the diode, CR_3 in this circuit is back biased. The input-output relationship of the circuit is determined by the following equation:

$$\text{Volts out} = 7/T$$

where T is the period of the input signal in seconds. The response of the circuit is as shown on Figure 6. Above approximately 62 radians (10 cps) the gain of the circuit drops at 12 db/octave due to the double breakpoint.

For input periods between 0.1 second and 1.0 second, the diode CR_3 becomes forward biased, the output of the circuit is at plus 7 volts, and the drop across the zener diode CR_4 and CR_5 is approximately 7 volts. Once the diode is forward biased the feedback resistance becomes the series pair R_6 and R_7 in parallel with R_5 and, since R_5 is very small with respect to R_6 , the resistance of R_5 is the effective resistance of the feedback in this mode.

FIGURE 6 APP. DESIGN RESPONSE OF PERIOD CIRCUIT

606356A

The output is related to the input according to the following equation:

$$\text{Volts out} = 0.2/T$$

where T is the period of the input signal in seconds. The entire characteristic is shown on Figure 5 over the input inverse period range -0.2 to +10 seconds.

The output of the average period circuit is displayed on a meter on the LRE Console and CTE Console and is available as a 0 to 10 volt output signal at the external connector J₂ Pin FF. Also available is a buffered average period signal at connector J2 Pin EE for use where a buffered output is required.

6.0 OPERATING INSTRUCTIONS

Once the Average and Reject Circuit has been installed, a series of adjustments and operational checkouts must be made.

However, after these adjustments have been completed, no further manipulation is necessary except for routine calibration checks and preventive maintenance (see Maintenance Instructions). Controls, adjustments and operational test procedures follow here.

7.0 CONTROL-OPERATIONAL AND SEMI-PERMANENT

To limit the access to alignment controls, all operating controls have, except for the power fuses, been placed on a component panel inside the Average and Reject Chassis or top mounted on the various component cards.

8.0 FRONT PANEL

8.1 Fuses

Six 1/2 ampere fuses are located on the front panel in their fuse-holders. The holders are marked from left to right:

+15VDC	
-15VDC	Log Ckts & Utility
+15VDC	
-15VDC	Averager "A"
+15VDC	
-15VDC	Averager "B"

9.0 COMPONENT PANEL (SEE FIGURE 11)

Nineteen test points are located on the component panel on the top and at the front of the instrument. These are clearly identified and are for the following services:

9.1 Test Points

TP1	LOG POWER NO. 1	(INPUT NO. 1)
TP2	LOG POWER NO. 2	(INPUT NO. 2)
TP3	LOG POWER NO. 3	(INPUT NO. 3)
TP4	HIGH LOG POWER	(AUCTIONEERED INPUT)
TP5	AVERAGE "A"	
TP6	AVERAGE "B"	
TP7	AVERAGE	
TP8	BUFF. AVERAGER	
TP9	AVERAGE PERIOD	
TP10	BUFF. AVG. PERIOD	
TP11	COMPARATOR OUTPUT NO. 1	
TP12	COMPARATOR OUTPUT NO. 2	
TP13	COMPARATOR OUTPUT NO. 3	
TP14	REJECT ADJUST CHAN. NO. 1	

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TP15	REJECT ADJUST CHAN. NO. 2
TP16	REJECT ADJUST CHAN. NO. 3
TP17	-15VDC
TP18	COMMON
TP19	+15VDC

10.0 OPERATIONAL CHECKOUT

After installing the NRX Average and Reject Chassis according to the procedures detailed under Installation Instructions, certain calibration and alignment checks should be performed.

10.1 Alignment and Test Equipment Needed

Multimeter - Simpson 269 or equivalent
Digital Voltmeter - EAI Model 6001 or equal
4 - 10VDC Adjustable Power Supplies

10.2 Mechanical Checkout

Before application of primary power for the electrical checkout, examine gear carefully for mechanical rigidity of all mounted components connectors, knobs, and the like. Remove the meter shorting strap if not already removed, and mechanically zero the meter. Use a small screwdriver to rotate the zeroing mechanism while lightly tapping the meter face with the finger tips until the needle indicates infinity on the meter.

10.3 Electrical Checkout

Operating voltages are readily accessible (for measuring) at clearly marked test points. Refer nameplates on Test Panel.

10.3.1 Assembly Connection Points

The checkout procedures delineated below should be made after the main power has been turned on and the equipment has warmed up for a minimum of 30 minutes. Before turning on main power, connect actual loads and, if required, remote meters.

10.3.2 Average and Reject (Neutronics) Alignment Procedure

10.3.2.1 Steps involving Simpson 269 voltmeter

check the plus and minus 15 volt power mains into the average and reject chassis at test points 17 through 19 to insure the proper 15VDC input voltages. The voltage inputs to the chassis should be adjusted to obtain $+15 \pm 0.15$ V between TP19 and TP18 and for minus 15 ± 0.15 V between TP17 and TP18. TP18 is the common for both measurements.

10.3.2.2 Steps involving digital voltmeters

10.3.2.2.1 Adjustment of channel rejection levels

1. Turn on the equipment and allow the unit to warm up for a minimum of 30 minutes.
2. Operate all three inhibit switches (inhibited indicator lamps for all three channels should come on).
3. Operate the ACTIVE/REJECT switches on all three channels until all channels are in the active mode (ACTIVE indicators on all three channels should be on).

4. Set the inputs at Pins A, B, and C of connector J2 (TP1, TP2, and TP3 to TP18) to $5 \pm .005$ VDC.

NOTE: The inputs can be from the individual log amplifiers by use of the range calibrator or from adjustable voltage sources connected into TP1, TP2, and TP3 to TP18. If adjustable voltage sources are used, the cable to connector J2 should be removed prior to the introduction of the voltage sources.

5. Alignment of Channel 1 reject level

5.1 Operate inhibit switch of channel

1. The channel 1 inhibit indicator lamp should go off.

5.2 Adjust the trip circuit trip set

adjust, R_1 on Unit A14 until the voltage at TP1 on Unit A14 is a maximum positive value (approximately +15VDC).

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- 5.3 Adjust the input signal to channel 1 to 5.250 volts. (TP1 to TP18).
- 5.4 Adjust the trip circuit trip set adjust, R_1 on Unit A14 until the reject lamp of channel 1 goes on.
- 5.5 Set the channel 1 input voltage at TP1 to 5.000 volts DC and operate the ACTIVE/REJECT switch for channel 1. The reject lamp will go out and the active lamp on.
- 5.6 Slowly increase the input voltage to channel 1 (TP1 to TP18) until the reject lamp comes on. Note the voltage at which this occurs. This voltage should be about 5.250 volts DC.
- 5.7 Repeat steps 5.5 and 5.6 while slowly adjusting R_1 of A14 until the channel rejects at $5.250 \pm .025$ VDC.
- 5.8 Repeat steps 5.5 and 5.6 except slowly decrease the input voltage. The reject lamp should come on at $4.750 \pm .040$ VDC.
- 5.9 Set the input to channel 1 to $5 \pm .005$ VDC, reset the reject by operating the channel 1 ACTIVE/REJECT switch, and inhibit channel 1 by operating the channel 1 inhibit switch.

6. Alignment of Channel 2 reject level
 - 6.1 Operate the inhibit switch of channel 2. The channel 2 inhibit indicator lamp should go off.
 - 6.2 Adjust the trip circuit trip set adjust, R_{13} on Unit A14 until the voltage at TP2 on Unit A14 is a maximum positive value (approximately +15VDC).
 - 6.3 Adjust the input signal to channel 2 to 5.250 volts (TP2 to TP18).
 - 6.4 Adjust the trip circuit trip set adjust, R_{13} on Unit A14 until the reject lamp of channel 2 goes on.
 - 6.5 Set the channel 2 input voltage at TP2 to 5.000 volts DC and operate the ACTIVE/REJECT switch for channel 2. The reject lamp will go out and the active lamp on.
 - 6.6 Slowly increase the input voltage to channel 2 (TP2 to TP18) until the reject lamp comes on. Note the voltage at which this occurs. This voltage should be about 5.250 volts DC.
 - 6.7 Repeat steps 6.5 and 6.6 while slowly adjusting R_{13} of A14 until the channel rejects at $5.250 \pm .025$ VDC.
 - 6.8 Repeat steps 6.5 and 6.6 except slowly decrease the input voltage. The reject lamp should come on at $4.750 \pm .040$ VDC.

- 6.9 Set the input to channel 2 to $5 \pm .005$ VDC, reset the reject by operating the channel 2 active/reject switch, and inhibit channel 2 by operating the channel 2 inhibit switch.
7. Alignment of channel 3 reject level
 - 7.1 Operate the inhibit switch of channel 3. The channel 3 inhibit indicator lamp should go off.
 - 7.2 Adjust the trip circuit trip set adjust, R_1 on unit A15 until the voltage at TP1 on unit A15 is a maximum positive value (approximately +15VDC).
 - 7.3 Adjust the input signal to channel 3 to 5.250 volts (TP3 to TP18).
 - 7.4 Adjust the trip circuit trip set adjust, R_1 on unit A15 until the reject lamp of channel 3 goes on.
 - 7.5 Set the channel 3 input voltage at TP3 to 5.000 volts DC and operate the ACTIVE/REJECT switch for channel 3. The reject lamp will go out and the active lamp on.
 - 7.6 Slowly increase the input voltage to channel 3 (TP3 to TP18) until the reject lamp comes on. Note the voltage at which this occurs. This voltage should be about 5.250 volts DC.

- 7.7 Repeat steps 7.5 and 7.6 while slowly adjusting R_1 of A15 until the channel rejects at $5.250 \pm .025$ VDC.
 - 7.8 Repeat steps 7.5 and 7.6 except slowly decrease the input voltage. The reject lamp should come on at $4.750 \pm .040$ VDC.
 - 7.9 Set the input to channel 3 to $5 \pm .005$ VDC, reset the reject switch, and operate the inhibit switches on channels 1 and 2. All inhibit lamps should be off. This completes the alignment of the channel reject levels.
8. Adjustment of Average Circuit A and Average Circuit B Reject Circuits
 - 8.1 Rotate the trip set adjusts R_1 and R_{13} on the average circuit reject trip circuits card A5 until the voltages at TP1 and TP3 are their maximum positive values (approximately +15VDC).
 - 8.2 Connect a digital voltmeter to the output test jack on Average A trigger circuit (TP2 on unit A5). The voltage should be less than -1 VDC.

- 8.3 Adjust the average A trip adjust, R_1 on card A5 until the voltage at TP2 on card A5 goes above -14VDC. The average A reject lamp should come on. Depress the average A reject/act switch and adjust R_1 until the lamp comes on at exactly this point. Hold the active/rej. switch depressed while making this adjustment.
- 8.4 Connect the digital voltmeter to TP1 on unit A5. Note the voltage at this test point. Adjust the average A trip set adjust, R_1 on card A5 until the voltage is 1.0 volt higher than it was.
- 8.5 Connect a digital voltmeter to the output test jack on average B trigger circuit (TP4 on unit A5). The voltage should be less than -1VDC.
- 8.6 Adjust the average B trip adjust, R_{13} on card A5 until the voltage at TP4 on card A5 goes above -14VDC. The average B reject lamp should come on. Depress the average B reject/act switch and adjust R_{13} until the lamp comes on at exactly this point. Hold the active/rej. switch depressed while making this adjustment.

8.7 Connect the digital voltmeter to TP3 on unit A5. Note the voltage at this test point. Adjust the average B trip set adjust, R_{13} on card A5 until the voltage is 1.0 volt higher than it was.

8.8 This completes the Average A & B reject alignment.

9. Alignment of Averaging Amplifiers

9.1 Set all three inputs at 5VDC.

9.2 Reject Average B by placing a 5000 ohm resistor between TP1 on card A5 and +15VDC. Once the Average B rejects remove the resistor.

9.3 Adjust the Voltage Offset potentiometer, R_1 on the amplifier card, A_1 until the average output at TP7 reads $5 \pm .005$ VDC.

9.4 Reset Average B by operating the Active/Reject switch for Average B.

9.5 Reject Average A by placing the 5000 ohm resistor between TP3 on card A5 and +15VDC. Once the Average A rejects remove the resistor.

9.6 Adjust the Voltage Offset potentiometer, R_{13} on the average output at TP7 reads $5 \pm .005$ VDC.

9.7 Reset Average A by operating the Active/Reject switch for Average A.

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- 9.8 The average output at TP7 should read $5 \pm .007 \text{VDC}$.
- 9.9 This completes the alignment of the average amplifiers.

11.0 MAINTENANCE INSTRUCTIONS

11.1 Preventive Maintenance

Under normal conditions, no routine replacement of parts should be necessary. Good housekeeping practices include periodic dusting, cleaning, inspection and the like. Since the circuitry is low voltage, leakage is a lesser problem, however, dust and moisture always make this a potential problem. Consequently, it is advisable to be sure the components in the chassis are free of dust and moisture at all times.

11.2 Corrective Maintenance

Corrective maintenance, in depth, is performed at the factory, or by the Westinghouse field representative. Local corrective measures, however, may if necessary be performed at the skilled technician level. Standard isolation procedures and techniques are applicable. The alignment and test equipment specified earlier in this brochure suffice to determine a faulty component or circuit. Initial symptoms of malfunction and correction action are:

<u>Symptom</u>	<u>Action</u>
Blown Fuses	Replace
Loose Controls	Tighten
Off-Voltages at Test Points	Check Mains
Faulty Meter Readings	Realign
Overheating Smoke and Odors	Examine for shorts in load or output cables.
Intermittents	High resistance joints or loose connections.

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If any of the preceeding symptoms persist, it is an indication of deepseated malfunction and should be attended to at the using facility or rectified by the factory field representative. Minor items (non-critical capacitors and the like) may be replaced by local parts of edential value and tolerance.

12.0 DRAWING LIST

- 938J166 - Assembly, Average and Reject Chassis
- 936J150 - Schematic, Average and Reject Chassis
- 937J901 - Wiring, Average and Reject Chassis
- 978D758 - Assembly, Average Amplifier Module
- 979D500 - Assembly, High Signal Select Module
- 979D629 - Assembly, Average Log Power Reject Module
- 978D760 - Assembly, Buffer Amplifier Module
- 978D761 - Assembly, Period Amplifier Module
- 978D762 - Assembly, Comparator Module
- 978D763 - Assembly, Relay Module
- 978D704 - Assembly, Trigger Pulse Amplifier Module
- 978D742 - Assembly, Flip-Flop Module
- 979D501 - Assembly, Auto-Manual Reject Module
- 978D764 - Assembly, Relay Driver Module
- 978D866 - Assembly, Relay Module
- 978D196 - Assembly, Grounding Module

13.0 ACCEPTANCE TEST PROCEDURE FOR ETS-1 LOG NEUTRONICS AVERAGE AND REJECT CHASSIS

Each unit has been tested and must comply with the limits of WANL Specification Number T-711861, which follows.

TEST SPECIFICATION NUMBER 711861
Revision A - 5/17/66

ACCEPTANCE TEST SPECIFICATION
FOR
ETS-1 LOG NEUTRONIC AVERAGE AND REJECT CHASSIS

March 16, 1966

Prepared By: Charles E. Hardies 3/16/66
(C. E. Hardies) (Date)

Approved By: R. A. Singer 4/12/66
Control Systems Engineering Date

E. J. ... 5-23-66
Quality Engineering Date

INFORMATION CATEGORY

Unclassified
R. A. Singer 5/1/66
AUTHORIZED CLASSIFIER DATE

1.0 ACCEPTANCE TEST PROCEDURES FOR THE ETS-1 AVERAGING AND REJECTION
CIRCUIT

1.1 Introduction

This document contains the setup, alignment, and acceptance
test procedures for the ETS-1 Averaging and Rejection Circuit.

1.2 Applicable Documents

1.2.1 Drawings

936J150 Rev -	ETS-1 AVE. & REJ. Schematic
938J166 Rev -	ETS-1 AVE. & REJ. Assembly Drawing
937J901 Rev -	ETS-1 AVE. & REJ. Wiring Diagram

1.2.2 Documents

TME 1272	Operational Manual ETS-1 AVE. & REJ. CIRCUIT
----------	--

1.3 Equipment Required

1 Multimeter	(Simpson 269 or equal)
1 Oscilloscope	(Tektronix 585 or equal)
1 Digital Voltmeter	(EAI or equal)
1 Megger	(General Radio megohmmeter 1862-B or equal)
1 Input Simulator	(3 separate 0-10 volt adjustable voltage sources)

1.4 Acceptance Tests

1.4.1 General

The acceptance tests on the ETS-1 AVE. & REJ. Circuit shall
be performed in the order of and as specified in the following
sections of this procedure. Each instrument tested shall be
aligned, according to the alignment section of the ETS-1 AVE. &
REJ. Circuit Operational Manual, the unit allowed to operate for
a minimum of 30 minutes, and then the alignment checked and

adjustments in the alignment made prior to starting the operating portions of the acceptance tests. Any gross changes in alignment settings shall be recorded and reviewed by the engineer in charge prior to the start of the acceptance tests. In the event of an instrument failure during acceptance testing, the failure shall be recorded and reviewed by the Engr. Review Board to ensure that the failure is not due to a design deficiency, the equipment shall be repaired and the acceptance testing repeated from the start except that the visual shall be confined to that area where repairs were made. The acceptance tests shall consist of the following:

- (1) Visual Examination
 - (a) Workmanship, assembly, and fit
 - (b) Materials, parts, and finishes
 - (c) Treatment for prevention of corrosion
 - (d) Safety requirements
 - (e) Marking
- (2) Insulation Resistance
- (3) Operating Test

The equipment shall be energized and subject to an operating test to ensure the proper functioning of the equipment including all controls and adjustments. It shall be demonstrated that the alignment procedure is adequate for aligning the equipment, and that the equipment meets the operational design specifications. In addition, the unit shall be operated continuously for a period of at least 100 hours to ensure that all infant failures have been eliminated.

1.4.2 Visual Examination

The equipment under test shall be presented in its final form together with the applicable schematic, wiring diagram, and assembly drawing. The visual examination shall consist of the following parts:

1.4.2.1 Workmanship, Assembly, and Fit

The inspector shall inspect the equipment for workmanship to WANL requirements and to assure that the overall chassis is of the proper dimensions per the assembly drawing, Westinghouse Drawing No. 938J166. Any deviations from the drawing dimensions shall be recorded in the acceptance test data sheets.

1.4.2.2 Weight

The instrument shall be weighed and the weight recorded in the acceptance test data sheets.

1.4.2.3 Materials, Parts, and Finishes

The equipment shall be inspected to assure that the materials, parts, and finishes are in accordance with the applicable assembly drawings. Incoming inspection records on materials, parts, and finishes shall be utilized to determine conformance to the assembly drawings where possible. Any deviations from drawing specifications shall be recorded in the acceptance test data sheets.

1.4.2.4 Treatment for Prevention of Corrosion

The equipment shall be inspected to assure that the coatings for prevention of corrosion have not been impaired during the manufacturing cycle. Any deficiencies shall be noted in the acceptance test data sheets.

1.4.2.5 Safety Requirements

The equipment shall be inspected to insure that no safety hazard, such as sharp edges etc. exist on the equipment which are potential hazards to personnel operating or maintaining the equipment. Deviations shall be noted in the acceptance test data sheets.

1.4.2.6 Marking

The markings on the equipment shall be inspected to ensure conformance to the applicable drawings and to assure that they are acceptable as to permanance and readability. Deviations shall be noted in the acceptance test data sheets.

1.4.2.7 Visual Examination Review

After the visual examination of the equipment has been completed, the data sheets shall be reviewed by WANL Engineering and Quality Control and all deficiencies corrected by one of the following methods:

- (1) Drawing changes where drawing deficiencies are noted.
- (2) Design changes if necessitated.
- (3) Rework of the parts affected if required.
- (4) In cases where the deficiencies will not affect reliability of operation, safety, or a high level of workmanship, these deficiencies may not be corrected on the specific piece but manufacturing methods changed to eliminate the re-occurrence of the deficiency on future parts by the concurrence of WANL Engineering, Quality Control, and/or Reliability or Safeguards Engineering.

A record of the resolution to visual examination deficiencies shall be made in the acceptance test log book along with the signatures of the personnel agreeing to these resolutions.

1.4.3 Acceptance Operating Tests

1.4.3.1 Operating Tests--ETS-1 AVE. & REJ. CIRCUIT

The operating tests of the ETS-1 Ave. and Rej. Circuit perform the following evaluations:

- (1) Alignment Stability and Functional Check
 - (1a) Averaging Circuit
 - (1b) Period Circuit
- (2) Linearity
 - (2a) Averaging Circuit
 - (2b) Period Circuit

- (3) Accuracy and Drift
 - (3a) Averaging Circuit
 - (3b) Period Circuit
- (4) Output Noise
 - (4a) Averaging Circuit
 - (4b) Period Circuit
- (5) Transients
 - (5a) Input Transients
 - (5b) Power Supply
- (6) Response Time
 - (6a) Averaging Circuit
 - (6b) Rejection Circuit
 - (6c) Period Circuit
- (7) Loss of Phase Power
- (8) 100 Hour Operation

1.4.3.2 Alignment Stability and Functional Check

- 1.4.3.2.1 Connect the ETS-1 Ave. and Ref. Circuit
in the test setup of Figure 1. Apply
power and allow the equipment to warm
up for a minimum of 30 minutes.
- 1.4.3.2.2 Align the equipment per the alignment
procedure in the ETS-1 Ave. and Ref.
Circuit Operational Manual. The
rejection limits shall be set at
 ± 0.2 of a decade on the input.

1.4.3.3 Alignment Stability

- 1.4.3.3.1 Turn the input switch to "ON" and the
DVM switch SW₂, to Position 8. Record

TABLE 1

LINE NO.	Input Voltage at J2			Average Output Output DVM Pos. 8	Channels Rejected		
	1	2	3		1	2	3
1	0	0	0	0 $\pm$.01	No	No	No
2	2	2	2	2 $\pm$.01	No	No	No
3	4	4	4	4 $\pm$.01	No	No	No
4	6	6	6	6 $\pm$.01	No	No	No
5	8	8	8	8 $\pm$.01	No	No	No
6	10	10	10	10 $\pm$.01	No	No	No
7	2	0	0	0.66 $\pm$.01	No	No	No
8	0	0	4	1.33 $\pm$.01	No	No	No
9	0	6	0	2.0 $\pm$.01	No	No	No
10	8	0	0	2.66 $\pm$.01	No	No	No
11	0	10	0	3.33 $\pm$.01	No	No	No
12	2.275	2	2	2.090 $\pm$.01	No	No	No
13	2.475	2	2	2.00 $\pm$.01	Yes	No	No
14	4	4.275	4	4.090 $\pm$.01	No	No	No
15	4	4.475	4	4.00 $\pm$.01	No	No	No
16	6	6	6.275	6.090 $\pm$.01	No	No	No
17	6	6	6.475	6.00 $\pm$.01	No	No	Yes
18	8.275	8	8	8.090 $\pm$.01	No	No	No

Inhibit *
all
Channels

* This is accomplished by operating the inhibit switches on the channels, SW4, SW6, and SW8 on the test panel.

TABLE 1 CONT'D.

LINE NO.	Input Voltage at J2			Average Output Output DVM Pos. 1	Channels Rejected		
	1	2	3		1	2	3
19	8.475	8	8	8.00 $\pm$.01	Yes	No	No
20	1.725	2	2	1.908 $\pm$.01	No	No	No
21	1.525	2	2	2.00 $\pm$.01	Yes	No	No
22	4	3.725	4	3.908 $\pm$.01	No	No	No
23	4	3.525	4	4.00 $\pm$.01	No	Yes	No
24	6	6	5.725	5.908 $\pm$.01	No	No	No
25	6	6	5.525	6.00 $\pm$.01	No	No	Yes
26	7.725	8	8	7.908 $\pm$.01	No	No	No
27	7.525	8	8	8.00 $\pm$.01	Yes	No	No

in the acceptance test data sheets the output voltage from the averaging circuit on the output digital voltmeter for the combination of inputs shown on Table 1. Record which channels reject on each test. Once the signal levels are set, operate the ACT/REJ Switches, SW3, SW5, and SW7 to activate all channels. The average output shall be as listed on Table 1 and the state of the channels as shown on that table. Record the data in the acceptance test data sheets.

1.4.3.3.2 Repeat the test of Paragraph 1.4.3.3.1 after one hour of operation. The average output shall be within the tolerances listed on Table 1. The state of each channel, rejected or not rejected shall be as shown on the table. Record the data in the acceptance test data sheets.

1.4.3.4 Manual Rejection Functional Checks

1.4.3.4.1 Set inputs 1, 2, and 3 to 5 volts $\pm .1$ volt. Manually reject Channel 1, Channel 1 should reject, Channels 2 and 3 shall not.

- 1.4.3.4.2 Manually activate Channel 1 and manually reject Channel 2. Channels 1 and 3 shall not reject and Channel 2 shall.
- 1.4.3.4.3 Manually activate Channel 2 and reject Channel 3. Channel 3 shall reject, Channels 1 and 3 not.
- 1.4.3.4.4 Record in the acceptance data sheets the results of tests 1.4.3.4.1 through 1.4.3.4.3.
- 1.4.3.4.5 Manually reject Channel 1. Increase the inputs to Channels 2 and 3, one at a time to 10 volts. Neither channel 2 or 3 shall automatically reject.
- 1.4.3.4.6 Activate all channels and repeat the test of 1.4.3.4.5 for Channels 2 and 3 manually rejected. Record the results of these tests in the acceptance test data sheets.
- 1.4.3.4.7 Manually reject Channels 1 and 2. Increase the signal on Channel 3 to 10 VDC. Channel 3 shall not reject. Repeat the test for Channels 2 and 3 and 1 and 3 manually rejected. Record the results of the test in the acceptance test data sheets.

1.4.3.4.8 Avg "A" & "B" Reset Check

Reject Avg "A". Operate the active reject switch for Avg "A" to activate the channel. Record in the test data sheets the proper reset of the Averager. Repeat for Average "B".

1.4.3.4.9 Close the Simulate Command, SIM COM., SW1.

Switch on the test setup panel. Measure the resistance between connector pins J2R and J2S. The resistance shall be less than 2 ohms. Measure the resistance between connector pins J2T and J2S. The resistance shall be greater than 10 megohms. Open the SIM COM. switch. Measure the resistance between connector pins J2R and J2S. The resistance shall be greater than 10 megohms. Measure the resistance between connector pins J2T and J2S. The resistance shall be less than 2 ohms.

1.4.3.4.10 Set inputs 1, 2, and 3 on the test panel to 5 volts. Measure the average log output, DVM Switch SW2 in Position 8. The output shall be $5 \text{ VDC} \pm .01 \text{ VDC}$.

Measure the buffered average log output, DVM SW2 in Position 7. The output shall be $-5.0 \pm .02$ VDC.

Measure the non inverted buffered log output, DVM SW2 in Position 9.

The output shall be $5 \text{ VDC} \pm .02 \text{ VDC}$.

Close the SIM. COM. Switch. The Average log output as read on the DVM should drop to zero volts. Introduce a 5.000 VDC signal between connector pins J2K and J2L, positive at J2K. The average shall be $5 \pm .01$ VDC. Remove the signal from J2K and J2L and open the SIM. COM. switch.

1.4.3.5 Period Circuit Linearity and Accuracy

1.4.3.5.1 Set Switch 1 to the "ON" position.

Adjust the inputs to the Ave. and Ref. Circuit at J2 to 10 volts. Switch the input switch to the ramp position and adjust the ramp to the rates as shown on Table 2. Record the period output, Switch 2 on Position 6 on the output DVM at the tested ramp rate. Also record the buffered period output, SW2 on Position 5. The output voltage shall be within the tolerances listed. Record the data in the acceptance test data sheets.

1.4.3.5.2 Repeat the test of Paragraph 1.4.3.5.1 after one hour. The meter indications and output voltages of the period circuit shall be within the tolerances as specified on Table 2.

1.4.3.6 Output Noise

1.4.3.6.1 Average Log Power Output Noise

1.4.3.6.1.1 Set all of the inputs to the averaging and rejection circuit to 0 volts at J2.

TABLE 2

<u>Input Ramp</u>	<u>Period Output Voltage</u>
0	0 ± 0.5 VDC
0.087 Volts/sec.	0.7 ± 0.5 VDC
0.143 Volts/sec.	5 ± 0.5 VDC
0.87 Volts/sec.	7 ± 0.5 VDC
8.7 Volts/sec.	9 ± 0.5 VDC

Set the input switch to "OFF". Take a polaroid picture of the average log power output and paste this picture in the acceptance test data sheet. The noise on the average log power output with the inputs grounded shall not be greater than 0.020 volts peak.

1.4.3.6.2 Average Period Circuit Noise

1.4.3.6.2.1 Set all of the inputs to the averaging and rejection circuit to 0 volts at J2. Set the input switch to "OFF". Take a polaroid picture of the avg. period output. Paste this picture in the acceptance test data sheets. Record the scope settings. The noise at the output of the period circuit shall be less than 0.02 volts peak.

1.4.3.7 Transients

1.4.3.7.1 Input Transients

1.4.3.7.1.1 Set all inputs to 5 volts at J2. Insert a voltage transient at the

input of Channel 1 with a pulse generator. Use a Pulse Amp. of 0.5 volts. Vary the pulse width to cause an automatic rejection. Decrease the pulse height to .275 volts the channel should not automatically reject regardless of pulse width. Record the pulse widths to cause an automatic rejection at the specified pulse heights in the acceptance test data sheets.

1.4.3.7.1.2 Repeat 1.4.3.7.1.1 for each of the other two channels.

1.4.3.7.1.3 Set the inputs to the following Channel 1 5.275 volts, Channels 2 and 3 to 5 volts. Insert a pulse into the input of Channel 1 of .2 volts. Determine the pulse width required in order to cause Channel 1 to automatically reject. Increase the pulse height to 0.5 volts. Determine the pulse width to cause the channel to automatically reject. Reduce the

pulse height to 0.05 volts. The channel should not reject regardless of pulse width. Record the results in the acceptance test data sheets.

1.4.3.7.1.4 Repeat the test of 1.4.3.7.1.3 for the other inputs, 2 and 3.

1.4.3.7.1.5 Set the input to Channel 1 at 5.275 volts and the inputs to Channels 2 and 3 at 5 volts. Insert a pulse of .6 volts into all 3 inputs. Increase the pulse height to 3.0 volts. Increase the pulse height to 5.0 volts. No channel should reject. Record the results in the acceptance test data sheets.

1.4.3.7.2 Line Voltage Transients

1.4.3.7.2.1 Set the inputs to the average and reject circuit of J2 as follows:
Channel 1 = 5.275, 2 = 5.00, 3 = 4.725.
Insert a line transient of + 10% on the excitation input to the AVG & REJ. chassis. The transient shall have a rise time of less than 50 mins.

No rejections should occur. Record the results in the acceptance test data sheets.

1.4.3.7.2.2 Repeat Paragraph 1.4.3.7.2.1 for a -10% line transient.

1.4.3.7.2.3 Set the inputs to the average and rejection circuit as follows:

1 = 5.475, 2 = 5.275, 3 = 4.725.

Insert a line transient of +10% on the excitation input to the unit.

Channel 1 should be rejected and 2 and 3 not rejected before the re-transient, and no change in state should occur as a result of the transient. Record the results in acceptance test data sheets.

1.4.3.7.2.4 Repeat the test 1.4.3.7.2.3 for a -10% line transient.

1.4.3.8 Response Time

1.4.3.8.1 Set the inputs to the averaging and rejection chassis to the following values: Channel 1 = 7, 2 = 7, 3 = 7. Increase the input to Channel 1 to

9.2 volts instantaneously and measure

the time for the channel to reject.

Take a polaroid photo of the measurement

and put it together with the scope

settings into the acceptance test data

sheets.

1.4.3.8.2 Repeat 1.4.3.8.1 for Channels 2 and 3.

1.4.3.8.3 With the inputs set at 7 volts on all channels, increase the input to all channels to 8 volts (step change) by increasing the output voltage of the power supply, psi. Measure the time required for the average output to reach 80% of its new value. Place the polaroid picture of average response in the acceptance test data sheets.

1.4.3.8.4 Repeat 1.4.3.8.3 with the inputs all channels at 2 volts and the step value to 3 volts.

1.4.3.9 100-Hour Operation

1.4.3.9.1 The unit shall be operated for a minimum of 100 hours including checkout and acceptance testing, prior to shipment.

If the unit has not been operated for this amount of time at the end of the acceptance tests, allow it to run for the remainder of time, and then check it operationally, using the test of Para. 1.4.3.3.1.

1.4.4 Additional Test Requirements by Q.C.

1.4.4.1 Fuse Indicator Test

1. Remove all $\pm$ 15 volt fuses from front panel.
2. Apply + 15 VEC to J1-L, - 15 VDC to J1-M and their common connection to J1-F.
3. All plus and minus 15 volts fuse indicators on the front panel should light.
4. Replace all $\pm$ 15 volt fuses.
5. All fuse indicators should be "OFF".

1.4.4.2 Insulation resistance between Safety Ground J1-E and Signal Ground J1-F.

1. With all connector plug terminals tied together except safety ground (J1-E), measure >10 MEG ohms at 500 VDC between J1-E and J1-F.

1.4.4.3 Continuity checks. Remove all power and connections from the chassis under test. Measure continuity as indicated below:

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<u>From</u>	<u>To</u>	<u>Resistance</u> Ω	<u>Check</u>
TP1	J2-A	< 2	_____
TP2	J2-B	< 2	_____
TP3	J2-C	< 2	_____
Chassis	J1-E	< 2	_____
TP19	J1-L	< 2	_____
TP17	J1-M	< 2	_____
TP18	J1-F	< 2	_____
J2 <u>d</u>	J2- <u>y</u>	< 2	_____
J2 <u>d</u>	J2- <u>z</u>	> 10 MEG	_____
J2 <u>j</u>	J2AA	< 2	_____
J2 <u>j</u>	J2BB	> 10 MEG	_____
J2 <u>n</u>	J2CC	< 2	_____
J2 <u>h</u>	J2DD	> 10 MEG	_____
TP4	J5-3	< 2	_____
TP5	J3-11	< 2	_____
TP6	J4-11	< 2	_____
TP7	J8-9	< 2	_____
TP7	J2-HH	< 2	_____
TP8	J8-11	< 2	_____
TP8	J2-GG	< 2	_____
TP9	J9-11	< 2	_____
TP9	J2-FF	< 2	_____

<u>From</u>	<u>To</u>	<u>Resistance</u>	<u>Check</u>
TP10	J10-11	< 2	_____
TP10	J2-EE	< 2	_____
TP11	J11-11	< 2	_____
TP12	J12-11	< 2	_____
TP13	J13-11	< 2	_____
TP14	J22-14	< 2	_____
TP15	J23-14	< 2	_____
TP16	J24-14	< 2	_____
TP18	J2- <u>e</u>	< 2	_____
TP18	J2- <u>f</u>	< 2	_____
TP18	J2- <u>g</u>	< 2	_____
TP18	J2- <u>h</u>	< 2	_____
TP18	J2-U	< 2	_____
TP18	J2-V	< 2	_____
TP18	J2-W	< 2	_____
TP18	J2-L	< 2	_____

ETS-1 Log Neutronic Average and Reject Acceptance Test Setup

FIGURE 1
ETS-1 Log Neutronic Average and Reject
Acceptance Test Setup

1.5 Data Sheets for WANL Average and Reject Chassis

(P/N 938J901 Rev _ , S/N _____)

1.5.1 Visual Examination _____

1.5.1.1 Workmanship, Assembly, and Fit. (Para. 1.4.2.1)

Comments: _____

1.5.1.2 Weight (Para. 1.4.2.2) _____ lb.

1.5.1.3 Materials, Parts and Finishes (Para. 1.4.2.3)

Comments: _____

1.5.1.4 Treatment for Prevention of Corrosion

(Para. 1.4.2.4) Comments: _____

1.5.1.5 Safety Requirements (Para. 1.4.2.5)

Comments: _____

1.5.1.6 Marking (Para. 1.4.2.6)

Comments: _____

1.5.1.7 Visual Examination Review (Paragraph 1.4.2.7)

Comments: _____

1.5.2 Alignment Stability and Functional Checks

1.5.2.1 Alignment Check (Par. 1.4.3.3.1)

Line no.	INPUT VOLTS AT J2			Channels Rejected		
				Avg. Output (DVM Sw in Pos 1)		
	A	B	C	Ideal & Tol.	Actual	Check if Correct
1	0	0	0	0 $\pm$.01		No No No
2	2	2	2	2 $\pm$.01		No No No
3	4	4	4	4 $\pm$.01		No No No
4	6	6	6	6 $\pm$.01		No No No
5	8	8	8	8 $\pm$.01		No No No
6	10	10	10	10 $\pm$.01		No No No
7	2	0	0	0.66 $\pm$.01		No No No
8	0	0	4	1.33 $\pm$.01		No No No
9	0	6	0	2.00 $\pm$.01		No No No
10	8	0	0	2.66 $\pm$.01		No No No
11	0	10	0	3.33 $\pm$.01		No No No
12	2.275	2	2	2.090 $\pm$.01		No No No
13	2.475	2	2	2.00 $\pm$.01		Yes No No
14	4	4.275	4	4.090 $\pm$.01		No No No
15	4	4.475	4	4.00 $\pm$.01		No No No
16	6	6	6.275	6.090 $\pm$.01		No No No
17	6	6	6.475	6.00 $\pm$.01		No No Yes
18	8.275	8	8	8.090 $\pm$.01		No No No
19	8.475	8	8	8.00 $\pm$.01		Yes No No
20	1.725	2	2	1.908 $\pm$.01		No No No
21	1.525	2	2	2.00 $\pm$.01		Yes No No
22	4	3.725	4	3.908 $\pm$.01		No No No
23	4	3.525	4	4.00 $\pm$.01		No Yes No
24	6	6	5.725	5.908 $\pm$.01		No No No
25	6	6	5.525	6.00 $\pm$.01		No No Yes
26	7.725	8	8	7.908 $\pm$.01		No No No
27	7.525	8	8	8.00 $\pm$.01		Yes No No

Inhibit
All
Channels

1.5.2.2 Stability Check (Par. 1.4.3.3.2)

Line No.	INPUT VOLTS AT J2			Avg Output (dvm Sw in Pos 1)		Channels Rejected		
	A	B	C	Ideal & Tol.	Actual	A	B	C
	Check if Correct							
1	0	0	0	0 $\pm$.01		No	No	No
2	2	2	2	2 $\pm$.01		No	No	No
3	4	4	4	4 $\pm$.01		No	No	No
4	6	6	6	6 $\pm$.01		No	No	No
5	8	8	8	8 $\pm$.01		No	No	No
6	10	10	10	10 $\pm$.01		No	No	No
7	2	0	0	0.66 $\pm$.01		No	No	No
8	0	0	4	1.33 $\pm$.01		No	No	No
9	0	6	0	2.0 $\pm$.01		No	No	No
10	8	0	0	2.66 $\pm$.01		No	No	No
11	0	10	0	3.33 $\pm$.01		No	No	No
12	2.275	2	2	2.090 $\pm$.01		No	No	No
13	2.475	2	2	2.00 $\pm$.01		Yes	No	No
14	4	4.275	4	4.090 $\pm$.01		No	No	No
15	4	4.475	4	4.00 $\pm$.01		No	No	No
16	6	6	6.275	6.090 $\pm$.01		No	No	No
17	6	6	6.475	6.00 $\pm$.01		No	No	Yes
18	8.275	8	8	8.090 $\pm$.01		No	No	No
19	8.475	8	8	8.00 $\pm$.01		Yes	No	No
20	1.725	2	2	1.908 $\pm$.01		No	No	No
21	1.525	2	2	2.00 $\pm$.01		Yes	No	No
22	4	3.725	4	3.908 $\pm$.01		No	No	No
23	4	3.525	4	4.00 $\pm$.01		No	Yes	No
24	6	6	5.725	5.908 $\pm$.01		No	No	No
25	6	6	5.525	6.00 $\pm$.01		No	No	Yes
26	7.725	8	8	7.908 $\pm$.01		No	No	No
27	7.525	8	8	8.00 $\pm$.01		Yes	No	No

Inhibit
All
Channels

1.5.3 Manual Rejection Checks (Par 1.4.3.4.)

1.5.3.1 Results of Tests of 1.4.3.4.1 through
1.4.3.4.3 per 1.4.3.4.4

(1.4.3.4.1) Channel "1" Rejected_____

Channel "2" Not Rejected_____

Channel "3" Not Rejected_____

(1.4.3.4.2) Channel "1" Reset_____

Channel "2" Rejected_____

Channel "1" Not Rejected_____

Channel "3" Not Rejected_____

(1.4.3.4.3) Channel "2" Reset_____

Channel "3" Rejected_____

Channel "1" Not Rejected_____

Channel "2" Not Rejected_____

1.5.3.2 Results of Tests of Par 1.4.3.4.5 and
1.4.3.4.6 per 1.4.3.4.6

(1.4.3.4.5) Channel "1" Rejected_____

No Automatic Rejector on Channel "2" due
to increase in input signal_____

No Automatic Rejection on Channel "3" due
to increase in input signal_____

(1.4.3.4.6a) Channel "2" Rejected_____

No Automatic rejection on Channel "1" due

to increase in input signal _____

No automatic rejection on Channel "3" due

to increase in input signal _____

(1.4.3.4.6b) Channel "3" Rejected _____

No automatic rejection on Channel "1" due

to increase in input signal _____

No automatic rejection on Channel "2" due

to increase in input signal _____

1.5.3.3

Results of Test of Para. 1.4.3.4.7

(1.4.3.4.7a) Channel "1" Rejected _____

Channel "2" Rejected _____

Channel "3" Not Rejected Due

To Signal Increase _____

(1.4.3.4.7b) Channel "2" Rejected _____

Channel "3" Rejected _____

Channel "1" Not Rejected Due

To Signal Increase _____

(1.4.3.4.7c) Channel "3" Rejected _____

Channel "1" Rejected _____

Channel "2" Not Rejected Due

To Signal Increase _____

1.5.3.4

Results of Tests of Para. 1.4.3.4.8

(1.4.3.4.8) Avg "A" Resets (Ret. to Act.)

Properly _____

Avg. "B" Resets (Ret. to Act.)

Properly _____

1.5.3.5 Result of Tests of Para. 1.4.3.4.9

(1.4.3.4.9a) Resistance J2R to J2S

(2 ohms max) _____ ohms

Resistance J2T to J2S

(10 meg min) _____ ohms

(1.4.3.4.9b) Resistance J2R to J2S

(10 meg min) _____ ohms

Resistance J2T to J2S

(2 ohms max) _____ ohms

1.5.3.6 Result of Tests of Para. 1.4.3.4.10

Inputs 1, 2, and 3 at 5 VPC

Avg. Log Output (DVM Pos. 8)

(5 ± 0.01 VDC) _____ VDC

Buffered Log Output (DVM Pos. 7)

(-5 ± 0.02 VDC) _____ VDC

Non Inverted Buf. Log Output (DVM Pos. 9)

(5 ± 0.02 VDC) _____ VDC

Sim. Com. SW Closed _____

Avg. Log Output (DVM Pos. 8)

(0.00 ± 0.01 VDC) _____

5.000 VDC Applied Between

J2K and J2L _____ VDC

1.5.3.7 Results of Tests of Para. 1.4.3.5

(Para. 1.4.3.5.1)

Input Ramp	Buf. Period Output Volts		Period Output Volts	
	Ideal	Actual	Ideal	Actual
0	0 ± 0.5 VDC		0 ± 0.5 VDC	
0.087 volts/sec.	-0.7 ± 0.5 VDC		0.7 ± 0.5 VDC	
0.143 volts/sec.	-5.0 ± 0.5 VDC		5 ± 0.5 VDC	
0.87 volts/sec.	-7.0 ± 0.5 VDC		7 ± 0.5 VDC	
8.7 volts/sec.	-9.0 ± 0.5 VDC		9 ± 0.5 VDC	

(Para. 1.4.3.5.2)

Input Ramp	Buf. Period Output Volts		Period Output Volts	
	Ideal	Actual	Ideal	Actual
0	0 ± 0.5 VDC		0 ± 0.5 VDC	
0.087	-0.7 ± 0.5 VDC		0.7 ± 0.5 VDC	
0.143	-5.0 ± 0.5 VDC		5 ± 0.5 VDC	
0.87	-7.0 ± 0.5 VDC		7 ± 0.5 VDC	
8.7	-9.0 ± 0.5 VDC		9 ± 0.5 VDC	

1.5.3.8 Results of Test of Par 1.4.3.6.1

Scope Settings

Vertical_____

Horizontal_____

Comments_____

_____.

1.5.3.9 Results of Test of Par 1.4.3.6.2

Scope Settings

Vertical_____

Horizontal_____

Comments_____

_____.

1.5.4 Transient Test Results

- 1.5.4.1 Results of Test of Par 1.4.3.7.1.1 and
1.4.3.7.1.2 Channel "1"
(0.5 Pulse)Pulse Width to cause rejection____
(0.275Pulse)Channel will not reject_____
Channel "2"
(0.5Pulse)Pulse width to cause rejection____
(0.275Pulse)Channel will not reject_____
- 1.5.4.2 Results of Test of Par 1.4.3.7.1.3
Channel 1 input at 5.275_____
Channel 2 input at 5.000_____
Channel 3 input at 5.000_____
Pulse width of 0.2V Pulse into "1" to cause
Channel 1 to automatically reject_____
No rejection as a result of a 0.05V Pulse
regardless of width_____
- 1.5.4.3 Results of Test of Par 1.4.3.7.1.4a (pulse
into Channel 2)
Channel 1 input at 5.000V_____
Channel 2 input at 5.275V_____
Channel 3 input at 5.000V_____
Pulse width of 0.2V Pulse into "2" to cause
Channel 2 to automatically reject_____

Pulse width of 0.5V Pulse into "2" to cause
Channel to automatically reject_____
No rejection as a result of a 0.05V pulse
into 2 regardless of width_____

1.5.4.4 Results of Test of Par 1.4.3.7.1.4b (pulses
into Channel 3)

Channel 1 input at 5.000V_____

Channel 2 input at 5.000V_____

Channel 3 input at 5.275V_____

Pulse width of 0.2V Pulse into "3" to cause
Channel 3 to automatically reject_____

Pulse width of 0.5V Pulse into "3" to cause
Channel 3 to automatically reject_____

No rejection as a result of a 0.05 V

Pulse into 3 regardless of width_____

1.5.4.5 Results of Test of Par 1.4.3.7.1.5

Input to Channel 1 at 5.275V_____

Input to Channel 2 at 5.000V_____

Input to Channel 3 at 5.000V_____

No rejection (0.6VPulse into all channels)___

No rejection(3.0VPulse into all channels)___

No rejection (5.0VPulse into all channels)___

- 1.5.4.6 Results of Test of Para. 1.4.3.7.2.1 & 2
Channel 1 input at 5.275 VDC _____
Channel 2 input at 5.00 VDC _____
Channel 3 input at 4.725 VDC _____
No rejections as a result of +10% line
transient _____
No rejections as a result of a -10% line
transient _____
- 1.5.4.7 Results of Test of Para. 1.4.3.7.2.3 & 4
Channel 1 input at 5.475 VDC _____
Channel 2 input at 5.275 VDC _____
Channel 3 input at 4.725 VDC _____
No rejections as a result of +10% line
transient _____
No rejections as a result of a -10% line
transient _____
- 1.5.4.8 Results of Test of Para. 1.4.3.8
(1.4.3.8.1) All inputs at 7 VDC _____
Time required for Channel "1" to reject as
a result of input step to 9.2V _____

Scope Settings

Vertical _____

Horizontal _____

(1.4.3.8.2a) Time required for Channel "2"
to reject as a result of input step to
9.2 VDC _____

Scope Settings

Vertical _____

Horizontal _____

(1.4.3.8.2b) Time required for Channel "3"
to reject as a result of input step to
9.2 VDC _____

Scope Settings

Vertical _____

Horizontal _____

(1.4.3.8.3) Time required for average
output to reach 80% of its final value
as a result of step input to 8 VDC on all
channels _____

Scope Settings

Vertical _____

Horizontal _____

(1.4.3.8.4a) Inputs set at 2 VDC _____

Time required for average output to reach
80% of its final value as a result of step
input to 3 VDC on all channels _____

Scope Settings

Vertical _____

Horizontal _____

1.5.5 Additional Tests Requirements by Q.C.

1.5.5.1 Fuse Indicator Test (Para. 1.4.4.1)

All Indicators Light _____

1.5.5.2 Insulation Resistance (Para. 1.4.4.2)

Insulation Resistance Between

J1-E and J1-F _____

1.5.5.3 Continuity Checks (Para. 1.4.4.3)

<u>From</u>	<u>To</u>	<u>Resistance</u>	<u>Check If OK ()</u>
TP1	J2-A	< 2	_____
TP2	J2-B	< 2	_____
TP3	J2-C	< 2	_____
Chassis	J1-E	< 2	_____
TP19	J1-L	< 2	_____
TP17	J1-M	< 2	_____
TP18	J1-F	< 2	_____
J2 <u>d</u>	J2 <u>y</u>	< 2	_____

<u>From</u>	<u>To</u>	<u>Resistance</u>	<u>Check if OK ()</u>
J2 <u>d</u>	J2 <u>z</u>	> 10MEG	_____
J2 <u>i</u>	J2AA	< 2	_____
J2 <u>i</u>	J2BB	> 10MEG Ω	_____
J2 <u>n</u>	J2CC	< 2	_____
J2 <u>n</u>	J2DD	> 10MEG Ω	_____
TP4	J5-3	< 2 Ω	_____
TP5	J3-11	< 2 Ω	_____
TP6	J4-11	< 2 Ω	_____
TP7	J8-9	< 2 Ω	_____
TP7	J2HH	< 2 Ω	_____
TP8	J8-11	< 2 Ω	_____
TP8	J2GG	< 2 Ω	_____
TP9	J9-11	< 2 Ω	_____
TP9	J2-FF	< 2 Ω	_____
TP10	J10-11	< 2 Ω	_____
TP10	J2-EE	< 2 Ω	_____
TP11	J11-11	< 2 Ω	_____
TP12	J12-11	< 2 Ω	_____
TP13	J13-11	< 2 Ω	_____
TP14	J22-14	< 2 Ω	_____
TP15	J23-14	< 2 Ω	_____
TP16	J24-14	< 2 Ω	_____
TP18	J2- <u>e</u>	< 2 Ω	_____
TP18	J2- <u>f</u>	< 2 Ω	_____

<u>From</u>	<u>To</u>	<u>Resistance</u>	<u>Check if OK ()</u>
TP18	J2-g	< 2 Ω	_____
TP18	J2-h	< 2 Ω	_____
TP18	J2-U	< 2 Ω	_____
TP18	J2-V	< 2 Ω	_____
TP18	J2-W	< 2 Ω	_____
TP18	J2-L	< 2 Ω	_____

WANL-TME-1272

1.5.6

100 Hours Operation Certification Unit has operated
for a minimum of 100 hours. _____

Comments _____