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TRANSISTORS

Counters

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ABSTRACT

Two transistor plug-in decade counters are described, one of which operates over the SCS-7 temperature range. A transistor digital scanner with storage and parallel readout is described. It utilizes one of the plug-in decades. A simple design procedure for flip-flops is presented.

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TRANSISTORS

Counters

A 100-KC TRANSISTOR PLUG-IN DECADE COUNTER

Photographs of the 100-kc decade are shown in Fig. 1. The package dimensions are roughly $1\frac{1}{2} \times 2 \times 5$ inches. The schematic diagram is shown in Fig. 2. The circuit consists of four stages of bistable multivibrators (flip-flops) and two feedback circuits which artificially add six counts, thus changing the scale-of-16 to scale-of-10. The input and coupling circuits each consist of two AC gates connected in parallel to provide proper pulse routing.

The counting sequence is as follows:

Positive input pulses having a minimum size of 1 volt versus 1 microsecond are counted in binary fashion through the 7th pulse. The 8th pulse sets a "1" in the 4th binary which then sets the 2nd and 3rd binary to "1", thereby adding a 2 and a 4 so that 8 counts look like 14. The 9th count looks like 15, and the 10th count resets all binaries to "0", causing a positive step to appear at the output. The counting sequence is shown in Fig. 3.

To reset, the bases on the right-hand transistor of each flip-flop are momentarily grounded, turning on those transistors. This condition is defined as "0" condition. Of course, it is possible to use a negative supply also. In this case, those points marked "+" are returned to ground and those marked "ground" to B-. Reset would then be accomplished by returning the bases to B- rather than ground during reset.

The decade will operate over a supply voltage range of 2 to 35 volts and a temperature range of -90 to $+170^{\circ}\text{F}$.

A 1.4-MC TRANSISTOR PLUG-IN DECADE COUNTER

Figure 4 shows external and internal views and Fig. 5, a schematic diagram of a decade counter which will respond to pulses having a repetition rate up to 1.4 mc.

The Sylvania 2N94A has an alpha cutoff frequency of 6 mc and a common emitter gain of approximately 10. Therefore its common emitter cutoff is about 600 kc. The flip-flop operation is pushed to twice this amount by employing emitter followers in the cross-coupling circuits from collector to opposite base. A better impedance match is obtained with a resultant unloading of the collectors and much faster switching times. The maximum resolution frequency of the counter is then determined as the point beyond which the loop gain is less than 1.

1a external

1b internal

Fig. 1 -- External and internal views of a 100-kc transistor plug-in decade counter

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Fig. 2 -- Schematic diagram of a 100-kc transistor plug-in decade counter

497 005

Fig. 3 -- Counting sequence

4a external

4b internal

Fig. 4 -- External and internal views of a 1.4-mc transistor plug-in decade counter

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Fig. 5 -- Schematic diagram of a 1.3-mc transistor plug-in decade counter

Negative pulses are required to trigger the decade. The power supply requirements are +10 volts ± 2 and -10 volts ± 2 .

The same feedback scheme is used as described for the 100-kc counter.

A TRANSISTOR DIGITAL SCANNER

Figure 6 shows top, front, and bottom views and Fig. 7, a schematic diagram of a counter and storage device. The device will count for a period of time governed by the "start" and "stop" commands and store a five-decade number (through 99,999).

It will count pulses greater than 0.2 volt in amplitude which have a repetition rate below 3.5 kc. (The repetition rate is limited by stepping switches which constitute the last three decades.)

The first two decades are the 100-kc, plug-in counters described previously. There is no visual readout from these decades, but there is a relay sampling matrix connected to each.

The last three decades are stepping switches which provide their own storage and also drive Inditron numerical indicators which provide visual readout of the three most significant figures.

The specific application for which the scanner was developed is to count output pulses from a Geiger-Muller (g-m) tube for 1-minute periods and to provide contact closures so that the number stored can be punched automatically on IBM cards. The scanner was connected in parallel with a commercial digital scanner for 10,000 operations and showed exact agreement.

A block diagram of the transistor scanner is shown in Fig. 8.

The pulse standardizer shapes pulses generated by the g-m tube. Both the pulse width and pulse amplitude are determined by the pulse standardizer for all pulses generated by the g-m tube that have an amplitude greater than a preset threshold.

The amplitude of the pulses generated by the g-m tube depends on two things:

1. The time between impinging beta particles and
2. The size of the capacitance from the anode of the g-m tube to ground.

The time between impinging beta particles determines the amplitude of the g-m tube output pulses when the tube does not have a long enough time to recover between impinging beta particles. Therefore, an amplitude threshold is set so that there will be no difference between counts from one digitizer to the other.

top view

front view

bottom view

Fig. 6 -- Views of a transistor digital scanner

Fig. 8 -- Transistor digital scanner block diagram

The coaxial cable that connects the g-m tube output to the pulse standardizer must have a particular length since coaxial cables have capacity and will attenuate the g-m output pulse. In order to standardize the count between units, one defined coaxial-cable length must be chosen.

The negative-going output pulse from the g-m tube is applied to the base of Q_1 through the differentiating network C_1 and R_1 . Q_1 is an emitter-follower whose input impedance is approximately 2.5 megohms. The biasing network, R_1 and R_2 , holds Q_1 near cutoff.

The negative-going pulse drives the base negative which causes the emitter to follow the base within 0.2 volt of the base driving pulse. The negative-going pulse at the top of R_2 is applied to the base of Q_2 through the coupling network, C_2 and R_3 . Q_3 is a pulse amplifier

whose gain is set approximately by the ratio of the collector-to-emitter circuit resistors. The inverted and amplified pulse is coupled from the collector of Q_2 to the base of Q_3 through the differentiating network, C_3 and R_6 . Q_3 is a high-gain amplifier and also sets the threshold level by means of the emitter-base biasing arrangement. When a count is desired, relay contacts connect the base of Q_2 to ground through R_6 . The emitter bias is set by R_8 and R_9 so that Q_3 is in the off condition. R_8 and R_9 are adjusted so that a 250-millivolt pulse at the input of Q_1 from the g-m tube will cause Q_3 to conduct. The 250-millivolt threshold sensitivity is chosen so that vacuum tube and transistor digitizers may be compared.

When the positive pulse applied to the base of Q_3 exceeds the bias voltage applied to the emitter, Q_3 conducts. The pulse at the collector of Q_3 is amplified and inverted. This negative-going pulse is applied to the base of Q_4 , turning Q_4 on. The collector of Q_4 rises to +11.4 volts. The right-hand side of capacitor C_6 which was initially at +11.6 volts rises with the collector of Q_4 to 23 volts. This action turns off the base-to-emitter diode of Q_5 by 11.4 volts. Capacitor C_6 charges through R_{11} , Q_4 , and R_{15} until the base of Q_5 reaches +11.6 volts. Q_5 starts to turn on. The collector of Q_5 rises toward +11.6 volts turning the base of Q_4 off. The collector of Q_4 returns to ground potential. Capacitor C_6 discharges through a low-impedance path, consisting of R_{10} , base-emitter diode of Q_5 , and R_{15} , to its initial condition. The positive-going output pulse is taken from the collector of Q_4 and routed to the input of the first decade counter. This output pulse is of fixed size and shape, independent of input, for a wide variation in input pulse shape.

Details of the relay sampling matrix are apparent from the schematic diagram, Fig. 8. The output from each binary of the decade is necessary to drive the matrix. An emitter follower, Q_6 , for example, is used to isolate each matrix relay from the decade.

The main virtue of the transistor scanner over the vacuum tube version is the reduction of power required and a resultant reduction in heat dissipation. The vacuum tube scanner has serial readout and requires external circuitry to switch its storage matrix from one decade to the next, greatly increasing readout time. The external circuitry also requires an additional power supply.

DESIGN PHILOSOPHY FOR TRANSISTOR COUNTERS

Typical Design for a Flip-Flop

The general circuit is shown in Fig. 9.

The object here is to have the "on" transistor held in conduction by bias voltages provided by the "off" transistor. Likewise, the "off" side is held off by biases provided from the "on" side. If the "off" side is turned on, the opposite condition will prevail.

Fig. 9 -- Flip-flop circuit configuration

Consider a flip-flop built around PNP transistors having a collector voltage rating of -45 volts, a common emitter gain of 50 at 5 ma, and a leakage current, I_{COB} , of 10 micro-amperes.

To hold a transistor in the nonconducting state, the base-emitter diode must be back-biased; i. e., base-positive with respect to emitter for a PNP. If only one supply voltage is to be used, it is then necessary to have the emitter potential below the most positive point in the circuit. This is done by inserting a resistor in series with the emitters. It is then possible to drive the bases positive with respect to their emitters.

Since one or the other of the transistors is always conducting, a DC potential will exist across the resistor, R_e , in common with both emitters and can be held reasonably constant by connecting a bypass capacitor, C_e , in parallel with it. A crude criterion for C_e is that the $R_e C_e$ product be long compared to a trigger-pulse length.

A design center of 1-volt back bias insures adequate margin for wide variation in transistors. Therefore, we shall design conservatively for a 2-volt drop across the emitter resistor at 5 ma. (One uses 5 ma because this is well within the rating of the transistor in question.)

$$R_e = \frac{2}{5} = 400 \text{ ohms}$$

Since the collector voltage swing is approximately equal to the supply voltage less the emitter voltage, and a large swing is desirable, the emitter voltage should be kept reasonably low.

If we assume that the "on" transistor is saturated (collector positive with respect to base), then the emitter-to-collector voltage is less than 1/2 volt. The saturation voltage can be read directly from the transistor static curves (see Fig. 10).

Fig. 10 -- Transistor static curves

Therefore, using a negative supply, the collector of the "on" transistor is at $V_{Re} + V_{SAT}$ below ground, or about -2.5 volts. For a 15-volt supply, the drop across the "on" collector resistor is $15 - 2.5 = 12.5$ volts. For $I_C = 5$ mils,

$$I_b = \frac{I_c}{\beta} = \frac{5}{50} = 0.1 \text{ mil}.$$

Insert a large safety factor here to insure sufficient base drive for saturation, say, 0.5 mil. Then, neglecting the forward drop across the emitter-base junction, V_b for the "on" transistor equals $V_e = -2$ volts.

Choose R_b large with respect to the emitter-base resistance, say, 10 k. Then $I_{R_b} = \frac{2.0}{10 \text{ k}} = 0.2 \text{ mil}$ and $I_{R_n} = I_b + I_{R_b} = 0.7 \text{ mil}$.

Now determine R_c . Considering the "on" transistor

$$R_c = \frac{V_{SUPPLY} - V_c}{I_c + I_{R_{bOFF}}} = \frac{15 - 2.5}{5.10} = 2.4 \text{ K}.$$

Now determine R_n .

$$V_{c"OFF"} = V_{SUPPLY} - R_c I_{R_n}$$

$$= 15 - 2.4 \times 0.70 = 13.3 \text{ volts}$$

$$R_n = \frac{V_{c"OFF"} - V_{b"ON"}}{I_{R_n}} = \frac{13.3 - 2.5}{0.7} = 15 \text{ K}$$

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The final circuit then appears as in Fig. 11.

Fig. 11 -- Flip-flop circuit

Check the cross-coupling circuit for the off base; $I_{RN} = \frac{2.5}{25K} = 0.1 \text{ mil}$ ($I_{b"OFF"} = 0$). $V_{bOFF} = 0.1 \text{ mil} \times 10K = -1 \text{ volt}$. Since the off emitter is at -2 volts, $V_{be} = 1 \text{ volt}$, and the transistor is turned solidly off.

This flip-flop is bistable. That is, the side which is turned on will continue to conduct until the other side is turned on.

The safety factor built into the base driving current should receive some comment here. One reason for a large safety factor is that the common-emitter current gain, B , is greatly reduced at saturation. It is not unusual for a transistor to have B reduced by a factor of 5 for saturation versus nonsaturation for the same collector current. The actual B can be exactly determined experimentally for a particular transistor. It is only necessary to obtain a set of static output characteristics and read off the ratio I_c to I_b .

If the flip-flop is to operate over some temperature range, then the most straightforward design approach is the following. Consider the two conditions illustrated in Fig. 12: condition 1 for a collector resistance R_{L1} and condition 2 for a collector resistance R_{L2} . The two sets of common-emitter output characteristics are to the same scale and for the same transistor at the two extremes of the operating temperature range. Notice how the curves move away from the voltage axis as temperature increases. The implication is that the transistor gain increases as the temperature increases. Generally this is true. Also, the leakage current increases with temperatures (doubles every 10°C , approximately), which helps to bias the transistor on. As a result of these effects, the same base drive, I_{b2} , for example, yields considerably more collector current at high temperature than at low temperature.

Fig. 12 -- Flip-flop circuit for two conditions of collector resistance

If the "on" and "off" base currents are I_{b3} and I_{b1} , respectively, the flip-flop will not have two stable states for R_{L1} at high temperature, A_1' and B_1' . Note that I_{b1} , the base current for the "off" condition, is sufficient to saturate the transistor so the "off" condition, point B_1' , is the same as the "on" condition, point A_1' .

However, if the load is decreased to some value, R_{L2} , two stable states, A_2' and B_2' , will exist for I_{b3} and I_{b1} , respectively.

A simple summary of the above: choose the "on" collector current larger than the "off" collector leakage current at the upper temperature limit. The ratio, of course, will determine the output voltage swing, $V_{CON} - V_{COFF}$.

It is recommended that the output characteristics be obtained at the temperature limits as the first step in the design procedure. If the two sets of curves are superimposed on the same axes, Fig. 13, then the allowable range for the value of load, i.e., collector, resistance will be apparent.

Fig. 13 -- Composite characteristics for two temperatures

From Fig. 13, R_{L1} is the limit for the maximum value of R_L because at high temperatures, the "off" intercept is the same as the "on" intercept, point A. The minimum value of R_L is limited by the low temperature "on" condition, point B. An allowable range for R_L is between R_{L1} and R_{L2} . The required output voltage swing will then determine whether or not the transistor in question will meet the application requirements.

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Frequency Response Considerations

If the flip-flop is to be used at high frequency the first consideration is, of course, a good high-frequency transistor.

The 3-db frequency in a common emitter configuration is f_{α}/B . An SB-100 transistor having an f_{α} of 30 megacycles and a B of 20 could not be expected to operate above 1.5 megacycles in a standard flip-flop configuration.

Certain circuit modifications will result in improved high-frequency operation. These are:

1. Connecting capacitors in parallel with each cross-coupling resistor, R_N . These capacitors allow large driving currents to flow during the initial stages of switching, which shortens the response time.
2. Reducing the tolerances for "on" and "off" conditions. For example, set the "off" base at a few tenths of a volt rather than at 1 volt.
3. Couple from collector to opposite base through emitter followers. This provides a better impedance match and greatly decreases switching time.
4. Limit the collector swing with clipping and clamping diodes. The clamping diodes limit the lower swing of V_C so that saturation does not occur and t_1 , the hole-storage time, equals zero. The clipping diodes permit the use of a higher supply voltage than the transistor rating and thus shorten switching time.

The circuit of Fig. 14 includes all of these refinements.

Triggering

If the binary is to be used to divide by two from a single source, it is necessary to provide a routing scheme for the trigger pulses so that successive pulses will appear on alternate bases. The trigger is usually applied to the base for that is the most sensitive point.

Two AC gates connected together provide a simple pulse-routing scheme. Such a scheme is shown in Fig. 15. The diode bias resistors, R_1 , cause the diodes to alternately block, then pass the trigger pulses, depending on the collector voltage state.

For PNP's, a positive pulse applied to the base of the "on" transistor will turn it off. Likewise, a negative pulse applied to the base of the "off" transistor will tend to turn it on. The reverse is true for NPN's.

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A REFINED FLIP-FLOP

Fig. 14b

COMMON-EMITTER
OUTPUT CHARACTERISTIC

Fig. 14a

Fig. 14

Fig. 15 -- Pulse-routing diagrams

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If both positive and negative pulses are available from the source, then the decision as to which to use will be based on whether one wants sensitivity or speed.

For maximum trigger sensitivity turn the "on" transistor off. This requires that the least trigger pulse amplitude for the "on" bias be only the forward voltage drop across the emitter-base diode, nominally 0.1 to 0.2 volt.

For maximum switching speed, the "off" transistor should be turned on. This drives the transistor into an active condition, i.e., a gain greater than 1. The other transistor is already active so that both transistors assist in switching.

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